Introduction

Electrical overstress (EOS) has historically been one of the leading causes of integrated circuit failures, regardless of the semiconductor manufacturer. In general terms, electrical overstress can be defined as any condition where one or more pins on an IC are subjected to current and/or voltage levels that exceed the Absolute Maximum Ratings per the IC data sheet. The result of an EOS event can range from no damage or degradation to the IC up to catastrophic damage where the IC is permanently non-functional. EOS covers a broad spectrum of events, including electrostatic discharge (ESD), latch-up, power-up/power-down transients, and excessive DC current/voltage levels. ESD is typically the most common form of EOS, and consequently it is the focus of much of this chapter.

ADI recognizes the need to design ICs that are robust to all forms of EOS in order to maximize manufacturability and minimize customer failures. Over the past three decades, ADI has developed extensive expertise in designing ICs that are robust to EOS. In the 1970s, ICs were designed on relatively large geometry fabrication processes that inherently provided good robustness. Since the 1980s, as process geometries have shrunken, ADI has developed design rules and proprietary design techniques for providing adequate on-chip EOS protection. ADI holds many patents for novel on-chip EOS protection circuits for products on bipolar, bipolar-CMOS, and CMOS processes.

ESD Definitions

Electrostatic Discharge

Electrostatic Discharge (ESD) is a single fast, high current transfer of electrostatic charge between two objects at different electrostatic potentials.

ESD Pass Voltage

The ESD Pass Voltage of a particular device type is the highest voltage level at which all pins can be subjected to ESD events to a given ESD model without the device failing any data sheet test limits during subsequent electrical testing.

ESD MODELS / TEST METHODS

Overview

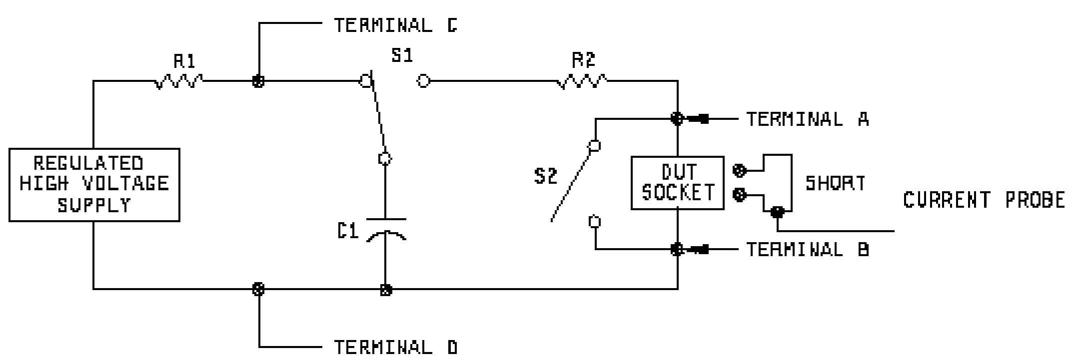
Failure Analysis (FA) at ADI on both in-house and customer-returned ICs with ESD failure signatures has shown that the vast majority can be simulated by either the Human Body Model (HBM) or the Charged Device Model (CDM). All ADI products (including major product revisions) are tested to the HBM and the CDM prior to release. Another ESD model sometimes referenced in the semiconductor industry is the Machine Model (MM), which is basically a worst-case Human Body Model. Since ADI and industry studies have shown that real-world ESD events rarely fit the MM, ADI does not place significant emphasis on this model. However, limited in-house MM testing and subsequent FA's have shown that the failure mechanisms for HBM and MM simulations are generally consistent. Therefore, ADI's design rules and proprietary design techniques for achieving adequate HBM ESD robustness also result in adequate MM ESD robustness.

Human Body Model (HBM) and Machine Model (MM)

The Human Body Model is the oldest and best-known ESD model. The HBM dates back to the 1800s. This model first gained acceptance in the semiconductor industry in the late 1960s as a method for simulating failures of Junction Field Effect Transistors (JFETs) used in the Flight Control Computer for the United States Titan III Space Program. The model consists of a simple series RC circuit with the values of R and C selected to simulate the discharge from the fingertip of a standing person that touches an IC. Although the HBM was used extensively during the 1970s, lack of consensus on a standard for test systems (in particular, what values of R and C to use) resulted in poor correlation between HBM thresholds measured using different ESD test systems.

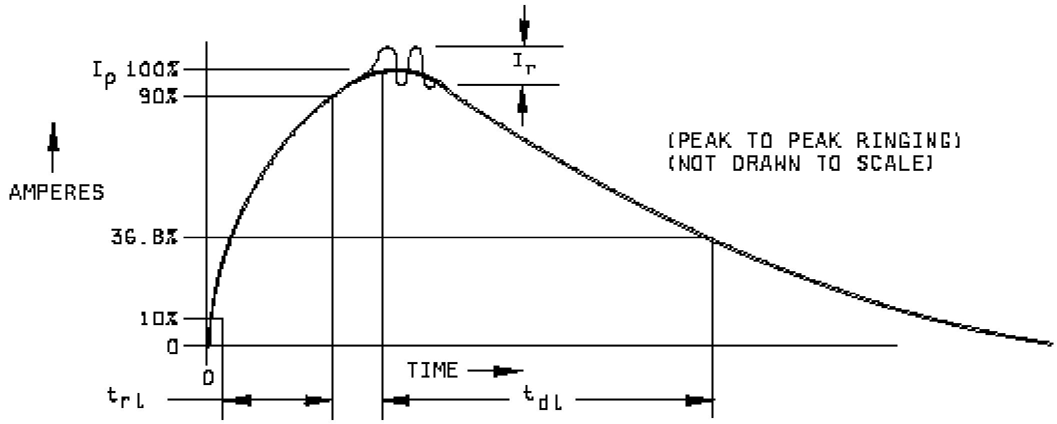
Correlation between testers greatly improved after MIL-STD-883 Method 3015 *Electrostatic Discharge Sensitivity Classification* was released in 1979[1]. This HBM test method specifies an RC network of $R_2 = 1500\Omega$ and $C_1 = 100pF$, as shown in Figure 1. Real-world RC values vary considerably from person-to-person and are a function of many variables, including the person's clothing/shoes, position, and surroundings. Consequently, the 1500Ω, 100pF model should be considered more of a benchmark than a true model for discharges from people's fingers. Per Figure 1, capacitor C1 is charged via a high voltage generator in series with a charge resistor R1. When high voltage relay S1 is thrown, the voltage V_{ESD} on C1 is discharged as current I_{ESD} through the series combination of discharge resistor R2 and the Device Under Test (DUT). The peak value of I_{ESD} is given by:

$$I_P = V_{ESD}/(R_2 + R_{DUT}). \quad (1)$$



R1 = 10^6 ohms to 10^7 ohms
C1 = 100 picoFarads ±10 percent (Insulation resistance 10^{12} ohms minimum)
R2 = 1,500 ohms ±1 percent
S1 = High voltage relay (Bounceless, mercury wetted, or equivalent)
S2 = Normally closed switch (Open during discharge pulse and capacitance measurement)

Figure 1: HBM ESD Test Circuit
(Excerpted from MIL-STD-883 Method 3015.7)



The current pulse shall have the following characteristics:

Tri (rise time) ---------------------	Less than 10 nanoseconds.
Tdi (delay time) -------------------	150 ±20 nanoseconds.
Ip (peak current) ------------------	Within ±10 percent of the Ip value shown in Table 1 for the voltage step selected.
Ir (ringing) --------------------------	The decay shall be smooth, with ringing, break points, double time constants or discontinuities less than 15 percent Ip maximum, but not observable 100 nanoseconds after start of the pulse.

Figure 2: HBM ESD Short-Circuit Current Waveform (Excerpted from MIL-STD-883 Method 3015.7)

The HBM ESD test circuit in Figure 1 essentially acts as an ideal current source that injects current into the DUT. Figure 2 shows the ESD current, I_{ESD}, vs. time when the DUT is a short-circuit ($R_{DUT} = 0\Omega$). This HBM ESD waveform has a characteristic double exponential shape, with a rise time typically in the 6-8ns range and a fall-time of $\tau = (R_2)(C_1) = (1500\Omega)(100pF) = 150ns$.

Table 1 shows the peak HBM ESD current, I_P, into a short-circuit ($R_{DUT} = 0\Omega$) for the typical minimum set of stress voltages used to classify the HBM ESD robustness of ADI products. Substituting $R_{DUT} = 0\Omega$ into equation (1), $I_{P(0\Omega)} = V_{ESD}/R_2$, or $I_{P(0\Omega)} = V_{ESD}/1500\Omega$. Thus, for a 1000V HBM event into a short-circuit, $I_{P(0\Omega)} = 1000V/1500\Omega$ or 0.67 Amp.

Table 1: ADI HBM ESDS Testing Stress Levels and Associated Classifications

Stress Voltage	Peak Current, I_P (±10%)	Sample Size	Corresponding HBM ESDS Classification for any electrical failures at this stress voltage
±500V	±0.33A	3	Class 1
±1000V	±0.67A	3	Class 1
±1500V	±1.00A	3	Class 1
±2000V	±1.33A	3	Class 1
±2500V	±1.67A	3	Class 2
±3000V	±2.00A	3	Class 2
±3500V	±2.33A	3	Class 2
±4000V*	±2.67A	3	Class 2

* If all samples pass following stress testing through ±4000V, the HBM ESDS classification is Class 3.

MIL-STD-883 Method 3015 has not been updated since 1989. Subsequently, two very similar test methods were released that more thoroughly specify HBM ESD Sensitivity testing:

- ESD-STM5.1-1998, *ESD Association Standard Test Method for Electrostatic Discharge (ESD) Sensitivity Testing: Human Body Model (HBM) – Component Level*[2]
- EIA/JEDEC Test Method A114-A, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM).*[3]

ESD-STM5.1-1998, which is the basis of ADI's HBM ESD classification program, is the strictest of these three industry specifications for HBM ESD Sensitivity classification testing. Consequently, ADI's HBM ESD results for a given product may be lower than those that would be obtained using MIL-STD-883 Method 3015.7 or EIA/JEDEC Test Method A114-A.

Unlike Method 3015.7, ESD-STM5.1-1998 and Test Method A114-A also provide waveform specifications for a 500Ω load. This provides for a more realistic evaluation of the ESD test system since DUTs obviously have finite (non-zero) resistance during stress testing. Substituting $R_{DUT} = 500\Omega$ into equation (1), $I_{P(500\Omega)} = V_{ESD}/(R_2 + R_{DUT})$. Thus, for a 1000V HBM event into a 500Ω load, $I_{P(500\Omega)} = 1000V/(1500\Omega + 500\Omega)$ or 0.50 Amp. As shown in Table 2, the rise time of the ESD current waveform is slower when $R_{DUT} = 500\Omega$ than when $R_{DUT} = 0\Omega$.

Table 2: Significant Differences Between Industry HBM ESD Specifications

Test Parameter	MIL-STD-883 Method 3015.7	EIA/JEDEC Test Method A114-A	ESD Association Std. Test Method STM5.1-1998 and ADI0082
Rise Time into a Short-Circuit	<10ns	2-10ns	2-10ns
Rise Time into a 500Ω Load	Not specified	5-25ns (for V_{ESD} = 4000V)	5-20ns (for V_{ESD} = 500V)
Number of pulses per pin combination in Table 2	3 positive + 3 negative	1 positive + 1 negative	1 positive + 1 negative
Failure criteria	Testing to room temperature DC parameters and functional tests	Testing to data sheet limits (both functional and parametric)	Testing to data sheet limits (both functional and parametric)

The Machine Model, or Zero-Ohm Model

The Machine Model uses the same basic test circuit as in Figure 1, except $R_2 = 0\Omega$ and $C_1 = 200pF$. ADI conducts MM testing based on customer requests/requirements, with most testing conducted per ESD-STM5.2-1999, *ESD Association Standard Test Method for Electrostatic Discharge Sensitivity Testing: Machine Model (MM) – Component Level*[4] . This is the most stringent MM test method in the industry, and it is very similar to the corresponding HBM test method, ESD-STM5.1-1998. Due to the high peak current of this 0Ω model, the MM ESD pass voltage for a given product is typically $1/5^{th}$ to $1/20^{th}$ of the HBM pass voltage. However, correlation is less predictable on low input impedance pins since the value of the series resistor (R_2) has a greater effect on the results.

Importance of Understanding Pin Combinations Zapped

ADI conducts HBM ESD classification testing on all new or redesigned products per internal corporate specification ADI0082. During this testing, one positive and one negative discharge (“zap”), each 0.3 to 1.0 second apart, is applied to all the pin combinations specified in Table 3. (These same pin combinations are used for MM ESD classification testing per MM test method ESD-STM5.2-1999.) HBM testing is typically conducted at ±500V, ±1000V, ±1500V, …±4000V, with three new samples used at each stress voltage level.

Table 3: Pin Combination Groups for HBM and MM ESD Testing at ADI

Group	Connection to Terminal A in Figure 1	Connection to Terminal B in Figure 1
1	Each pin one-at-a-time (other pins floating)	Power Supply 1
2	Each pin one-at-a-time (other pins floating)	Power Supply 2
n	Each pin one-at-a-time (other pins floating)	Power Supply n
n+1	Each non-supply pin one-at-a-time	All other non-supply pins as a group

In Table 3, each Power Supply (1, 2, …n) is the pin or group of pins that are shorted-together by metal either on-chip or in the IC package to form a unique power supply group. For example, if two Vdd pins are not shorted-together by metal, then these two pins are treated as separate power supply pins. To illustrate the application of Table 3, consider the AD724 RGB to NTSC/PAL Encoder. As indicated by the pin-out in Figure 3, this product has n=4 distinct power supplies: APOS, DPOS, AGND, & DGND. During HBM ESD classification testing per ADI0082, the AD724 is subjected to a total of 144 zaps (72 positive zaps, 72 negative zaps) using the 72 pin combinations shown in Figure 3. Note that all pins not connected to Terminal A or Terminal B are left floating.

Semiconductor companies other than ADI may not be as stringent about the pin combinations zapped during HBM ESD testing. Using the AD724 example, some companies might treat the APOS and DPOS supplies as a single positive supply pin group, and likewise treat the AGND and DGND supplies as a single GND pin group. (It can be argued that this is allowable per MIL-STD-883 Method 3015.7, but this is not allowable per ESD Association Standard Test Method STM5.1-1998 or EIA/JEDEC Test Method A114-A.) By grouping the supplies together in this manner, the AD724 would only be subjected to a total of 84 zaps (42 positive zaps, 42 negative zaps). Moreover, if the APOS pin had effective on-chip ESD protection and the DPOS pin did not, grouping these two pins together during zapping would “hide” the weakness of the DPOS pin. Thus, such testing could potentially result in a significantly higher HBM ESD pass voltage than would be obtained with ADI’s more stringent testing. This “higher” pass voltage could provide the user with a false sense of security when using the product in an environment with static problems.

	Term. A	Term. B
1	STND	APOS
2	AGND	APOS
3	FIN	APOS
4	ENCD	APOS
5	RIN	APOS
6	GIN	APOS
7	BIN	APOS
8	CRMA	APOS
9	COMP	APOS
10	LUMA	APOS
11	SELCT	APOS
12	DGND	APOS
13	DPOS	APOS
14	VSYNC	APOS
15	HSYNC	APOS

	Term. A	Term. B
16	STND	DPOS
17	AGND	DPOS
18	FIN	DPOS
19	APOS	DPOS
20	ENCD	DPOS
21	RIN	DPOS
22	GIN	DPOS
23	BIN	DPOS
24	CRMA	DPOS
25	COMP	DPOS
26	LUMA	DPOS
27	SELCT	DPOS
28	DGND	DPOS
29	VSYNC	DPOS
30	HSYNC	DPOS

	Term. A	Term. B
31	STND	AGND
32	FIN	AGND
33	APOS	AGND
34	ENCD	AGND
35	RIN	AGND
36	GIN	AGND
37	BIN	AGND
38	CRMA	AGND
39	COMP	AGND
40	LUMA	AGND
41	SELCT	AGND
42	DGND	AGND
43	DPOS	AGND
44	VSYNC	AGND
45	HSYNC	AGND

	Term. A	Term. B
46	STND	DGND
47	AGND	DGND
48	FIN	DGND
49	APOS	DGND
50	ENCD	DGND
51	RIN	DGND
52	GIN	DGND
53	BIN	DGND
54	CRMA	DGND
55	COMP	DGND
56	LUMA	DGND
57	SELCT	DGND
58	DPOS	DGND
59	VSYNC	DGND
60	HSYNC	DGND

	Term. A	Term. B
61	STND	All other I/Os
62	FIN	All other I/Os
63	ENCD	All other I/Os
64	RIN	All other I/Os
65	GIN	All other I/Os
66	BIN	All other I/Os
67	CRMA	All other I/Os
68	COMP	All other I/Os
69	LUMA	All other I/Os
70	SELCT	All other I/Os
71	VSYNC	All other I/Os
72	HSYNC	All other I/Os

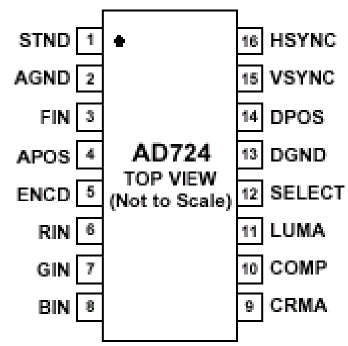


Figure 3: AD724 Pin-Out and 72 Pin Combinations Zapped During AD724 HBM ESD Testing

Charged Device Model (CDM)

The Charged Device Model originated at AT&T in 1974 as a new model to simulate field failure damage that could not be simulated by HBM testing[5]. Conceptually, the CDM is easy to understand. This model assumes the IC package is charged either directly via the triboelectric effect (i.e., via frictional contact with some material) or indirectly due to an external electric field. One or more package pins (e.g., leads, solder balls) subsequently contact a conductive surface at or near ground potential. This causes the charge stored on the die and associated conductive materials in the package (e.g., the bond wires and lead frame) to be dissipated in an ultra fast “spark discharge.” The discharge is almost instantaneous due to the low resistance (generally ~1Ω) and low inductance (typically only a few nH) of these conductive materials in the package.

Typical examples of triboelectric charging followed by a CDM discharge include:

- ICs become charged by sliding down an Automatic Test Equipment (ATE) handler chute and then corner pins discharge to a grounded stop pin.
- ICs become charged by sliding down a plastic shipping tube and then corner pins discharge to a grounded bench mat.

Typical examples of external-field-induced charging followed by a CDM discharge include:

- Rubber rollers in laser marking equipment generate a high electric field that induces charge on ICs. Corner pins then contact and discharge to a grounded stop pin.
- Cover tape is quickly removed from Tape-and-Reeled ICs during automated Printed Circuit Board (PCB) assembly operations, thus creating a high electric field that induces charge on ICs. Pin(s) on each IC are then discharged when they subsequently contact conductive traces on the PCB.

The Charged Device Model is highly effective at simulating ESD damage induced by automated equipment and automated shipping/handling. Automated equipment and IC packing materials can be designed to minimize charging, such as by using grounded conductive rubber rollers, antistatic shipping tubes, and antistatic Tape-and-Reel cover tape in the above examples. The amount of charging is also a function of numerous environmental variables. For example, charging decreases rapidly with increasing humidity and air ionization levels. However, no matter what precautions are taken, some degree of charging will always occur when an IC package contacts and moves over a dissimilar material. In fact, due to the automation of IC and PCB manufacturing operations, CDM ESD damage is now more prevalent than HBM ESD damage in the semiconductor industry.[6] Thus, ADI places heavy emphasis on designing ICs that are robust to CDM events as well as HBM events.

CDM testing can be conducted either with the Device Under Test (DUT) in a test socket (the Socketed Discharge Model, SDM) or “free-standing” (Non-Socketed or Robotic Charged Device Model, RCDM). ADI has extensive experience with both these test methods.[7] Although SDM testing is relatively easy to conduct, it does not always replicate real-world CDM failures as well as RCDM testing. Consequently, ADI has recently standardized on RCDM testing for classifying all new products and major die revisions. During RCDM testing, the charge is stored in the device capacitance, C_D, between the DUT and an adjacent ground plane with the DUT placed pins-up ("dead bug") on a thin dielectric layer over the ground plane (see Figure 4). The value of C_D is a function of the package, ranging from ~1pF for a very small package to ~20pF for a very large package. This device capacitance can be charged either directly using a charging probe or indirectly using a field-charging electrode. The latter option, referred to as Field-Induced Charged Device Model (FICDM) testing, is the basis for ADI’s CDM classification program, which is documented in ADI internal corporate specification ADI0429. As indicated in Figure 4, after the DUT is charged to the desired stress voltage (positive or negative) using the field charging electrode, the robotic pogo probe is used to discharge each pin through the 1Ω resistor to ground.

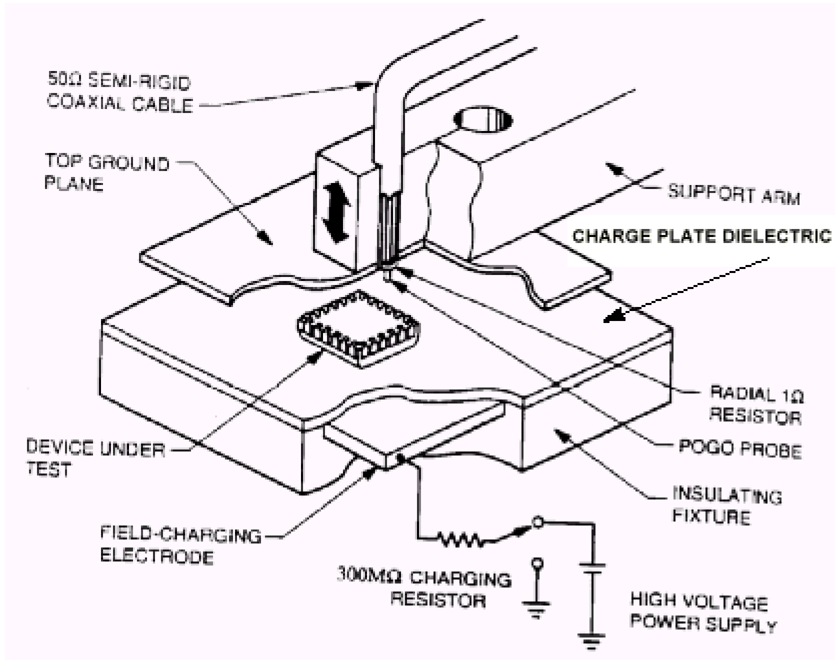


Figure 4: Field-Induced CDM ESD Test Circuit
(Excerpted from EIA/JEDEC Test Method C101)

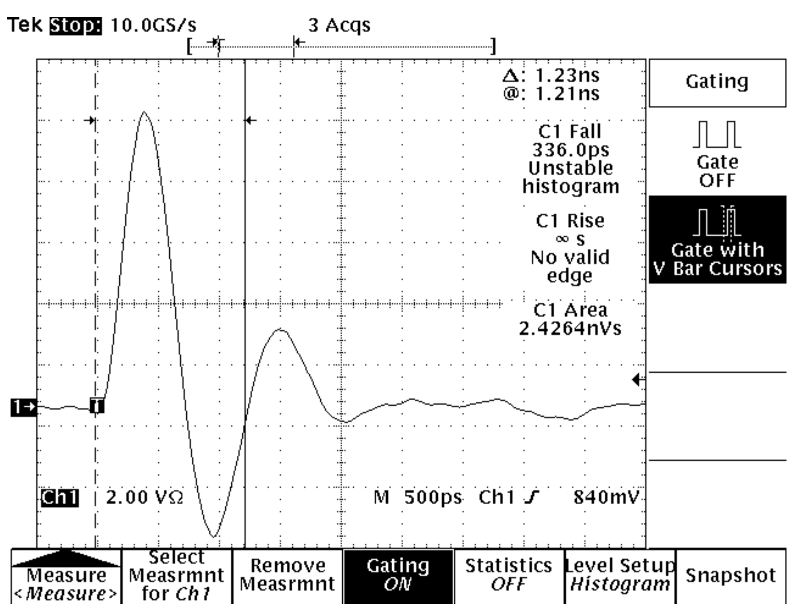


Figure 5: Field-Induced CDM ESD Current Waveform for a +250V Discharge using a 30pF Test Module and 10GHz oscilloscope.
Vertical Scale: 2V/div. through a 1Ω resistor = 2A/div.; $I_{PEAK} \approx 9.6A$.
Horizontal Scale: 500ps/div.; T_{RISE} (10% to 90% I_{PEAK}) $\approx$ 200ps.

For a 4pF Test Module (C_D = 4pF) and a 1GHz oscilloscope, Table 4 shows the peak FICDM ESD current, I_P, through the 1Ω discharge resistor for the typical minimum set of ESD stress voltages used to classify the FICDM robustness of ADI products.

Table 4: ADI FICDM ESDS Testing Stress Levels and Associated Classifications

Stress Voltage	Peak Current, I_P* (±20%)	Minimum Sample Size	Corresponding RCDM ESDS Classification for any electrical failures at this stress voltage
±125V	±1.13A	3	Class C1
±250V	±2.25A	3	Class C2
±500V	±4.5A	3	Class C3
±1000V	±9.0A	3	Class C4
±1500V**	±13.5A	3	Class C5

* This peak current is measured using a 4pF Test Module and a 1GHz bandwidth measuring system.
** If all samples pass following stress testing through ±1500V, the FICDM ESDS classification is Class C6.

The CDM waveform replicates the fastest known real-world ESD event. Figure 5 shows the ESD current, I_{ESD}, vs. time when a 30pF calibration module charged to +250V is discharged through R=1Ω to GND. Note the extremely fast rise time and very short total duration of the CDM ESD event. The measured rise time using a 10GHz oscilloscope is ≈200ps, and the entire discharge event is over in ≈2ns. In comparison, the duration of an HBM event is ≈100x longer, as shown in Table 5. The true rise time of a CDM ESD event is unknown; faster oscilloscopes than those currently available are needed to determine this. Unfortunately, the difficulty in measuring CDM waveforms and the availability of various "competing" test method options has impeded the widespread deployment of CDM testing. However, ADI recognizes the growing importance of this model and thus ADI now classifies all new products and major die revisions to the CDM prior to product release.

No MIL-STD-883 test method exists for conducting CDM testing. The two CDM standards most commonly used in the semiconductor industry are:

- ESD-DS5.3.1-1996, *ESD Association Draft Standard for Electrostatic Discharge Sensitivity Testing: Charged Device Model (CDM) Non-Socketed Mode - Component Level.*[8]
- EIA/JEDEC Test Method C101, *Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components.*[9]

ESD-DS5.3.1-1996, which is the basis of ADI's CDM ESD classification program, is slightly stricter than Test Method C101.

Unlike the relatively complicated pin combinations used during HBM testing, FICDM stressing is very straightforward. Each pin on the DUT is discharged a total of six times, with discharges occurring 0.3 to 1.0 seconds apart, as detailed below:

1. The DUT is charged positively to the desired voltage level and then pin 1 is discharged. This same sequence is repeated two more times.
2. The DUT is charged negatively to this same voltage level and then pin 1 is discharged. This same sequence is repeated two more times.
3. Steps 1 and 2 are repeated for each and every other pin on the DUT.

Unlike Human Body Model pass voltages, CDM pass voltages depend significantly on the package type. For a given product offered in multiple packages, smaller packages are typically less susceptible to CDM damage than larger packages. This is primarily because smaller packages have less lead frame area to store charge than do larger packages. Consequently, when ADI conducts FICDM testing on a new or revised product offered in multiple package styles, testing is either conducted on all available package styles or the worst-case package (typically the largest one) based on previous CDM test results.

Exercise Caution When Comparing Competitors' ESD Results

When comparing competitors' ESD data on a given part type, it is essential to understand exactly how the data was generated and what failure criteria were used. ADI follows stringent ESD test requirements based on ESD Association specifications. However, some semiconductor companies still follow less stringent test methods. One major cause of inconsistent ESD data from different semiconductor companies is differences in the failure criteria used when testing samples after ESD stressing. Consistent with ESD Association and JEDEC standards, ADI uses electrical testing to data sheet limits (including all functionality tests and all DC and AC parametric tests) as the post-stress failure criteria. Any sample that does not meet **all** data sheet limits after zapping is considered a failure. For instance, on an operational amplifier with a maximum bias current (I_B) specification of 1.0pA, if ESD stressing results in I_B = 1.1pA, the sample is considered a failure. Other semiconductor companies may consider this a "marginal" failure and discount it, whereas ADI treats it as a legitimate failure. In addition, other companies may simply use curve tracer testing or opens/shorts testing as their failure criteria, resulting in artificially high ESD pass voltages.

In summary, when comparing ESD results provided by different suppliers, it is essential to find-out:

- What test method was used
- What pin combinations were zapped, and
- What failure criteria were used.

Otherwise, you may be drawing improper conclusions due to an "apples to oranges" comparison.

Summary of HBM & FICDM Test Methods

Table 5 provides a summary comparison of the Human Body Model and the Field-Induced Charged Device Model as deployed at ADI. As this table indicates, these two models represent fundamentally different ESD events. Consequently, correlation between the test results for these models is minimal.

Table 5: Summary of HBM & FICDM Test Methods

	Human Body Model	**Field-Induced Charged Device Model**
Simulates:	Discharge from finger of a standing person	Discharge when a charged IC contacts a grounded surface
1st Used for ICs:	Late 1960s	1974
Basis for ADI Test Methods:	ESD Association ESD-STM5.1-1998	ESD Association ESD-DS5.3.1-1996
RC	1500Ω, 100pF	1Ω, typically 1-20pF
Rise Time	<10ns (typically 6-8ns)	<400ps (with a 1GHz scope)
I_{PEAK} at +1500V	1.0A	13.5A (with a 1GHz scope)
Energy for V_{PEAK} = +1500V	~1.5µJ	~2.0µJ
Total Duration:	~500ns	~2ns
Number of Discharges Per Pin	Variable; function of pin-out	6 (3 positive & 3 negative)
Failure Criteria	Testing to data sheet limits (both functional and parametric)	
Package Dependency:	No	Yes
Relevance to Real-World:	Moderate but decreasing	High and increasing

ADI TARGETS FOR ESD ROBUSTNESS

Based on reviews of customer General Semiconductor Specifications, discussions with customers, and our internal failure analysis results, ADI has established the following targets for ESD robustness for new products and major die revisions:

- Human Body Model: ≥2000V
- Field-Induced Charged Device Model: ≥1000V for corner/outside pins; ≥500V for other pins.

The targets for FICDM robustness on corner/outside pins are higher than for other pins since the majority of real-world CDM events occur on corner/outside pins. This is because a corner/outside pin on a charged IC is more likely than other pins to contact a hard or virtual ground, thus resulting in a CDM discharge. For example, on a 16-pin SOIC, corner pins 1, 7, 8, and 16 are the most likely to be subjected to a CDM discharge. On a 44-pin Quad Flat Package, corner pins 1, 11, 12, 22, 23, 33, 34, and 44 are particularly susceptible to a CDM discharge. As a final example, on a 225-ball Plastic Ball Grid Array (PBGA) package in a 15x15 configuration, the 56 balls along the outside rows are the most likely to be subjected to a CDM discharge.

Not all ADI products can meet the above HBM and FICDM robustness targets. Some older ADI products were released before design and layout rules were developed for achieving these levels of ESD performance. In addition, some products have electrical performance characteristics that preclude the use of standard on-chip ESD protection cells. Examples include:

- ICs with extremely low bias/leakage current specifications (pA to fA range)
- ICs with one or more pins that have operating/test voltages beyond the supply rails
- ICs with one or more high frequency pins (typically >300 MHz).

In cases such as these, most pins on the IC will meet ADI's targets for ESD robustness. However, the pins with special electrical performance requirements may not meet these targets. Whenever possible, these pins are not assigned as corner/outside package pins. This minimizes the probability that they will be subjected to real-world ESD events.

Some ADI products, such as RS-232 and RS-485 transceivers, are intended for use in environments that are particularly vulnerable to high-voltage ESD events. For such products, proprietary or patented design/layout techniques are used to achieve robustness levels far above the target ESD levels shown above. In addition, ESD/EOS testing is conducted using additional models/test methods. For example, the Input/Output pins on the latest versions of the ADM2209E and ADM3311E RS-232 transceivers pass all the following tests:

- ±15kV ESD testing per the IEC 61000-4-2 Air Discharge HBM (RC = 330Ω,150pF)[10]
- ±15kV ESD testing per the MIL-STD-883 Method 3015 HBM (RC = 1.5kΩ,100pF)
- ±8kV ESD testing per the IEC 61000-4-2 Contact Discharge Model (RC = 330Ω,150pF)
- At least ±2kV Electrical Fast Transient (EFT) testing per IEC 61000-4-4[11].

For further details on this testing as well as the ESD/EFT protection schemes, please see the ADM2209E and ADM3311E data sheets, which are available on the ADI Web Site at http://www.analog.com/.

ESD FAILURE MODES & FAILURE MECHANISMS

Overview

ICs subjected to ESD usually have distinct failure signatures. The most common ESD-induced failure mode is leakage or resistive shorts at I/O pins. Other failure modes include excessive supply current, open pins, or functional failures. The pins causing these failures can sometimes be identified via pin-to-pin current-voltage (I-V) curve tracer testing. However, particularly in the case of the CDM, the damage may be well past the on-chip I/O circuitry, and thus not detectable via I-V testing. In such cases, advanced Failure Analysis (FA) techniques may be required to locate the ESD damage.

Most ESD-induced failures occur due to one of more of the following three failure mechanisms:

- Conductor/resistor melting
- Dielectric damage
- Junction damage/contact spiking

Any of these failure mechanisms can potentially occur on any IC. However, dependent on the key features of the corresponding wafer fabrication process (e.g., very thin gate oxides, submicron line widths, thin-film resistors, etc.), certain failure mechanisms may predominate.

Conductor/Resistor Melting

Conductor or resistor melting can occur in thin metal interconnects, thin-film or thick-film resistors, and polysilicon resistors/interconnects. This is the easiest ESD failure mechanism to understand. The ESD event causes excessive localized Joule heating that melts the conductor or resistor material.

Conductor/resistor melting is most commonly seen on ICs subjected to HBM ESD since real-world HBM events typically have higher energy than real-world CDM events. In most cases, the ESD event completely fuses-open the conductor/resistor, thus resulting in a functional failure of the IC. However, in the case of thin-film and thick-film resistors, partial melting of the resistor material is possible, resulting in only a shift in the resistance and a corresponding parametric failure of the IC.

Figure 6 shows an example of a fused-open aluminum MET1 interconnect on an advanced bipolar IC that was non-functional after being subjected to ±2000V HBM stressing.

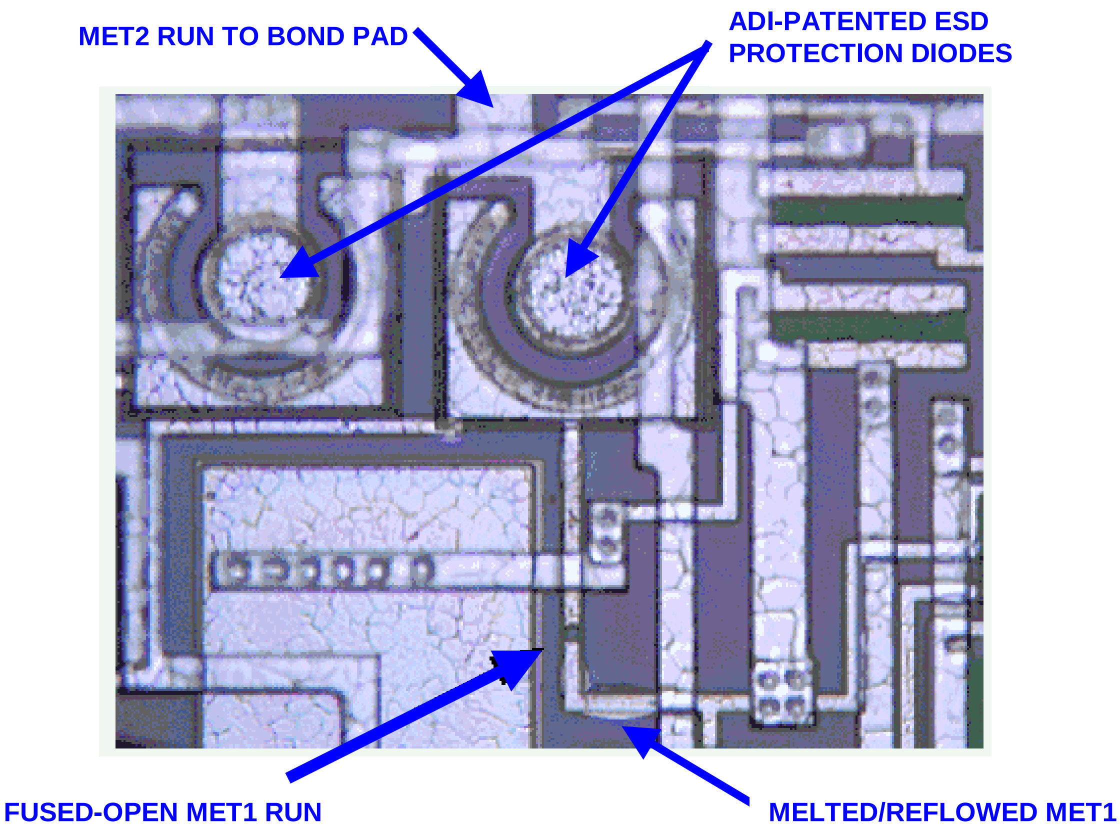


Figure 6: Optical microscope image of a 4µm wide MET1 interconnect on a sample stressed at ±2000V HBM. Note that this damage was visible without deprocessing.

In the case of the above IC, the 4µm MET1 run was in the primary path of ESD current flow during ESD stressing. This run was simply widened to 8µm, and this IC now has an HBM ESD pass voltage of ±4000V. Using Failure Analysis (FA) results from project chips and new products that are subjected to ESD stressing, ADI regularly updates IC design and layout rules so that they reflect best practices for achieving excellent ESD robustness.

Dielectric Damage

Dielectric damage can occur when the ESD voltage across a dielectric layer (e.g., silicon dioxide, silicon nitride) exceeds its dielectric strength, resulting in punchthrough. It is the predominant CDM failure mechanism since the extremely fast rise time is the most likely of all ESD models to result in excessive on-chip voltage. The sequence of events that causes dielectric damage is as follows:

1. The dielectric breakdown voltage is exceeded at a high electric field point (typically a submicron site at an edge, corner, or step in the dielectric layer).
2. Very high current flows through the breakdown site, resulting in adiabatic (highly localized) heating of the immediately adjacent area.
3. A melt filament (e.g., amorphous silicon or polysilicon) forms along the conduction site.

Figures 7 and 8 show an example of gate oxide damage sites on a PMOS output driver transistor that exhibited leakage after being subjected to FICDM discharges at the drain/output pin after the sample was charged to ±1500V. In this case, the gate polysilicon was at nearly ±1500V when the drain/output pin was instantaneously grounded. This resulted in dielectric breakdown, high current flow, and the formation of a melt filament, as detailed in 1-3 above.

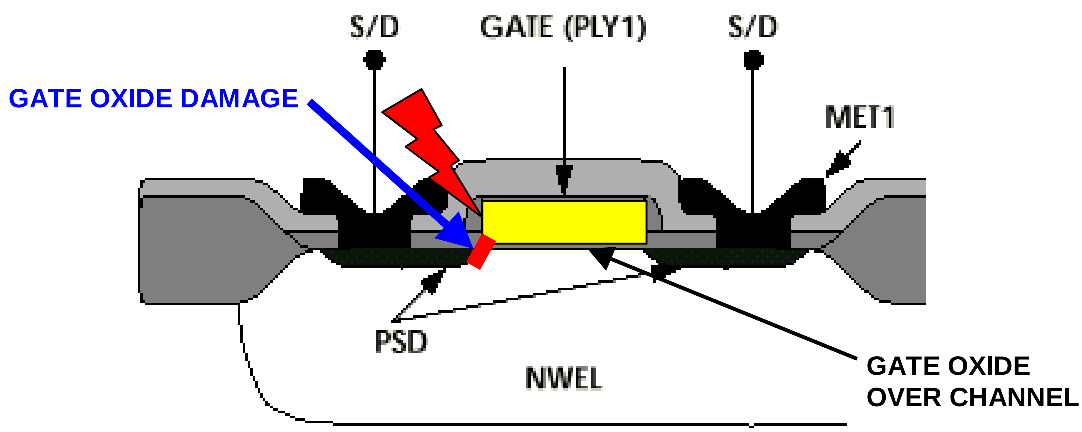


Figure 7: Location of Typical FICDM Gate Oxide Damage

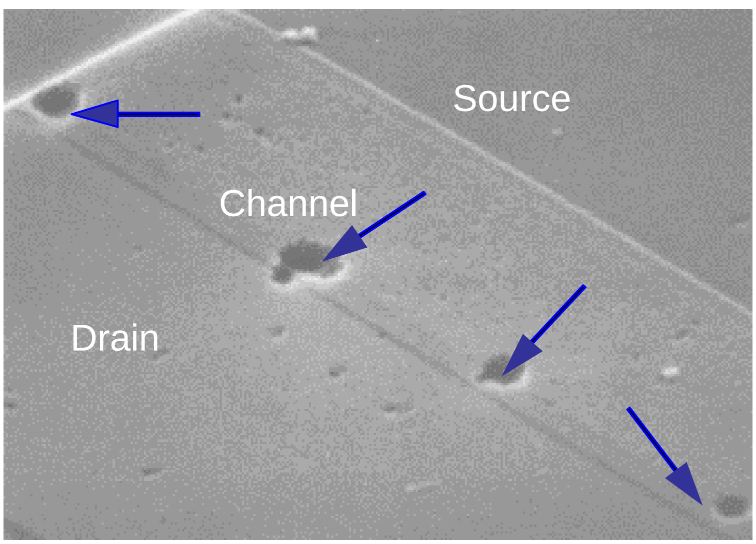


Figure 8: Scanning Electron Microscope (SEM) image post de-processing to the silicon level showing 4 pits on a sample stressed at ±1500V FICDM. These pits are ≈0.2-0.5µm in diameter and correspond to where silicon melted and flowed into the gate oxide.

ADI designs ICs that are relatively immune to dielectric damage by including proprietary ESD protection cells adjacent to bond pads and by including appropriate series resistors between the bond pads and the susceptible dielectric layers. The ESD protection cells are designed to turn-on extremely rapidly in response to an ESD event, thus clamping/limiting the voltage at the bond pad.

Junction Damage/Contact Spiking

Junction damage and/or contact spiking typically occur when a shallow P-N junction (e.g., the emitter-base junction of a bipolar transistor or the drain-substrate junction of an NMOS transistor) goes into avalanche breakdown followed by secondary breakdown and ultimately thermal run-away. The sequence of events that typically results in junction damage that may lead to contact spiking is as follows:

1. The avalanche breakdown voltage of a reverse-biased P-N junction is exceeded.
2. Secondary breakdown can then occur at a point where the P-N junction is sufficiently hot to cause thermal generation of carriers to exceed avalanche generation of carriers.
3. Very high current is “funneled through” the secondary breakdown site, resulting in adiabatic (highly localized) heating of the immediately adjacent area.
4. This highly localized heating accelerates the thermal generation of carriers. This further increases the current flow and results in a thermal run-away condition whereby more and more thermally-generated carriers cause higher and higher current flow. This culminates in melted silicon at the initial breakdown site if the temperature exceeds 1415°C.
5. If the heating is sufficient to melt the metal in an adjacent contact opening, the electric field can cause the melted metal to migrate across the junction, resulting in a resistively-shorted junction.

When the melted silicon at the secondary breakdown site on the P-N junction re-solidifies after the ESD event, the dopant profile is disturbed since the P-type and N-type dopants mixed together when the silicon melted. In addition, the re-solidification process alters the crystal properties of the silicon. The changes in the dopant profile combined with the changes in the silicon crystal properties result in “soft” reverse-breakdown I-V characteristics. Depending on the severity of the junction damage, the effect on the IC can range from an inconsequential increase in leakage current up to a significant increase in leakage current that results in one or more data sheet parameters being out of specification. Failure analysis at ADI has shown that ESD-induced crystal damage at a P-N junction can sometimes be partially "annealed out" by a 24 hour 125°C unpowered bake, but the I-V characteristics will still be softer than usual. This indicates that an IC junction that is damaged by ESD may actually have decreasing leakage current during field use, especially if the junction temperature is well above 25°C.

If the heating associated with the thermal run-away condition causes the metal in an adjacent contact opening to melt and migrate across the junction, the resulting resistive short typically causes the corresponding pin on the IC to exhibit a “hard” failure. High temperature baking of the IC will have little or no effect on this resistive short.

To reduce the susceptibility to contact spiking, transistor layout rules typically specify increased contact-to-junction spacings for contacts connected to external pins. Special design techniques and layout rules are also used to reduce the susceptibility of a junction to secondary breakdown and thermal run-away. As with conductor/resistor fusing, junction damage and contact spiking occur most commonly on ICs subjected to HBM ESD since HBM events typically have higher energy than CDM events.

Figures 9 and 10 show an example of drain-channel junction damage and drain contact spiking on an NMOS output transistor that exhibited a resistive short after being subjected to ±2000V HBM stressing at the drain/output pin.

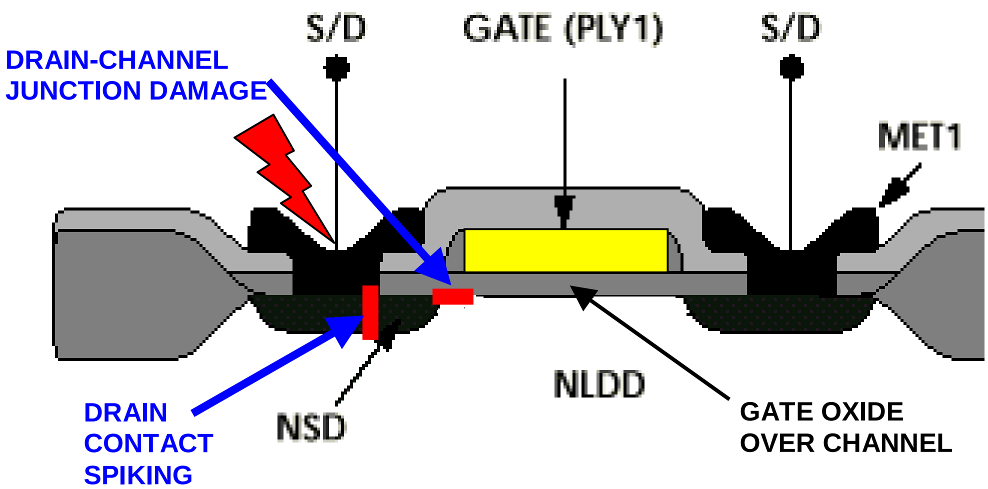


Figure 9: Locations of Typical HBM Contact Spiking and Junction Damage

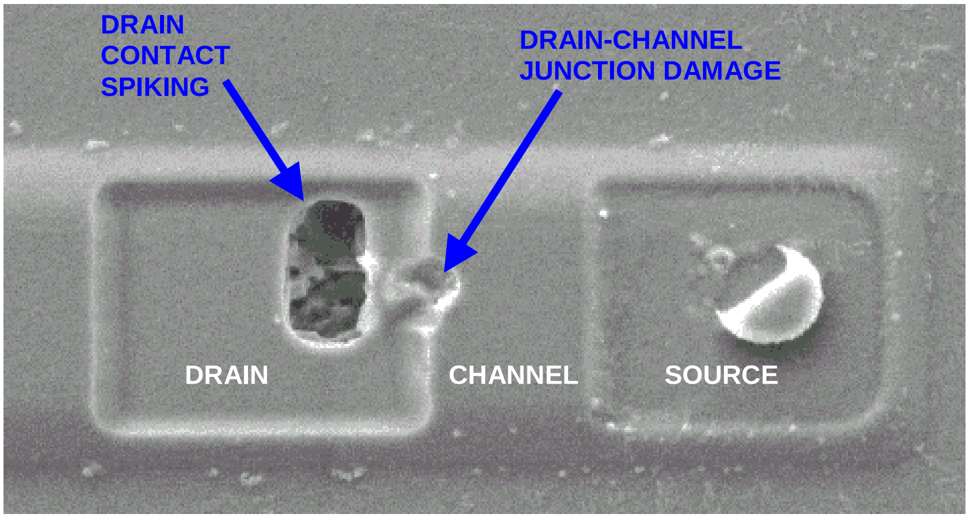


Figure 10: Scanning Electron Microscope (SEM) image post deprocessing to the silicon level showing drain-to-channel junction damage and drain contact spiking on a sample stressed at ±2000V HBM.

In the case of the above IC, the NMOS output transistor was made larger and a series resistor was added between the drain and the output pin. This transistor is now immune to ESD damage during HBM stressing up to at least ±4000V.

Summary of HBM & FICDM Test Methods

Table 6 provides a summary comparison of the three predominant failure mechanisms caused by ESD.

Table 6: Summary of ESD Failure Mechanisms

	Conductor/Resistor Melting	**Dielectric Damage**	**Junction Damage / Contact Spiking**
Failures occur at:	Thin Film, Thick Film, Polysilicon, Metal	Any dielectric layer, but especially thin layers such as gate oxide	Any junction, but especially emitter-base, drain-channel, & other small junctions
Failure Mode:	Resistance shifts & open-circuits	Leakage & resistive shorts	Junction damage: Leakage; Contact spiking: Resistive shorts
Failure Signature:	Partial or complete conductor/resistor fusing	Submicron conductive melt filament through the dielectric	Junction damage: Crystal damage across junction; Contact spiking: Hole in contact area
Most prevalent on:	Human Body Model (HBM) failures	Charged Device Model (CDM) failures	Human Body Model (HBM) failures
Bake Recoverable:	No	No	Partially, unless resistively shorted
Recoverable at Ambient:	No	No	No

Electrical Overstress

The Human Body Model (HBM) and Field-Induced Charged Device Model (FICDM) represent just two of the infinite number of forms of electrical overstress (EOS). As indicated in Figure 11, EOS covers an entire spectrum of events, with the FICDM and DC over-voltage/over-current on opposite ends of the spectrum. However, a "typical" EOS event has a duration on the order of 50 milliseconds. The much longer duration of a typical EOS event results in much more energy being delivered to the IC. For example, whereas +1500V HBM and CDM discharges have energies of ~1.5 microJoule and ~2.0 microJoule, respectively, typical EOS events can have energies exceeding 1 Joule. Thus, although the failure mechanisms associated with ESD and EOS are similar, the physical damage is generally much more severe with EOS failures. This is shown in Figures 12 & 13, which show typical examples of EOS damage that was readily visible with an optical microscope following decapsulation of the plastic package. Not surprisingly, for a given IC, the higher the energy of the EOS event the more likely permanent damage is to occur.

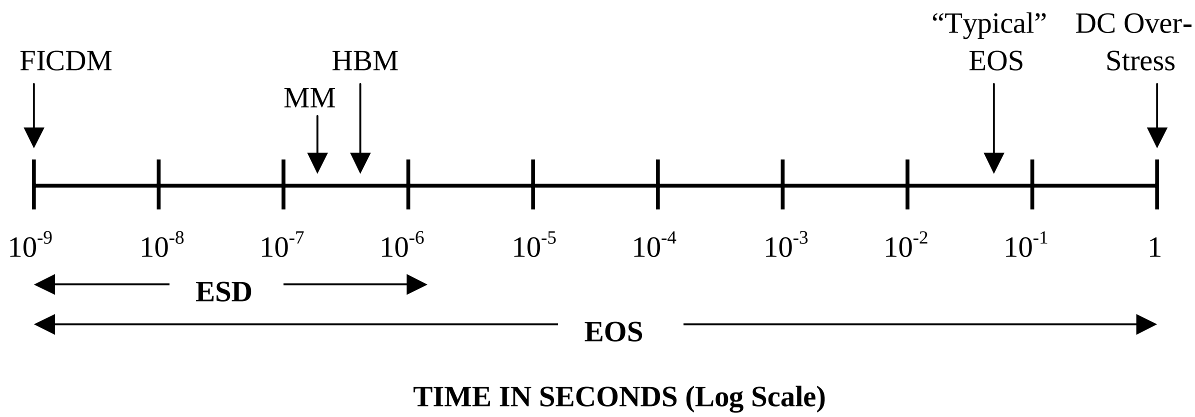


Figure 11: Spectrum Showing the Duration of Common EOS/ESD Events

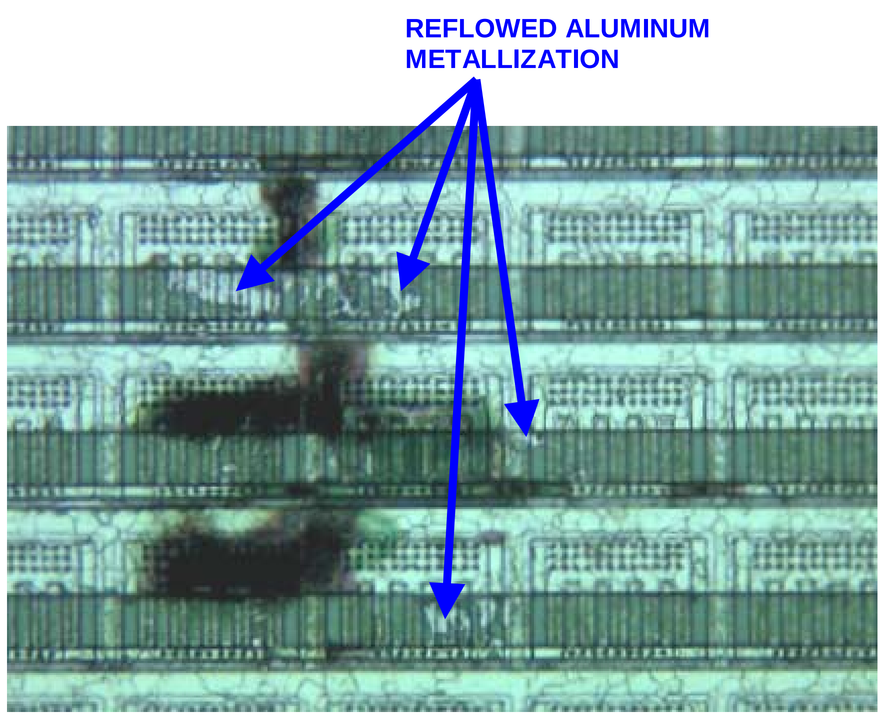


Figure 12: Optical microscope image of severe Electrical Overstress (EOS) damage at a bipolar output transistor. Note the black "burn mark" where the aluminum metallization melted and reflowed.

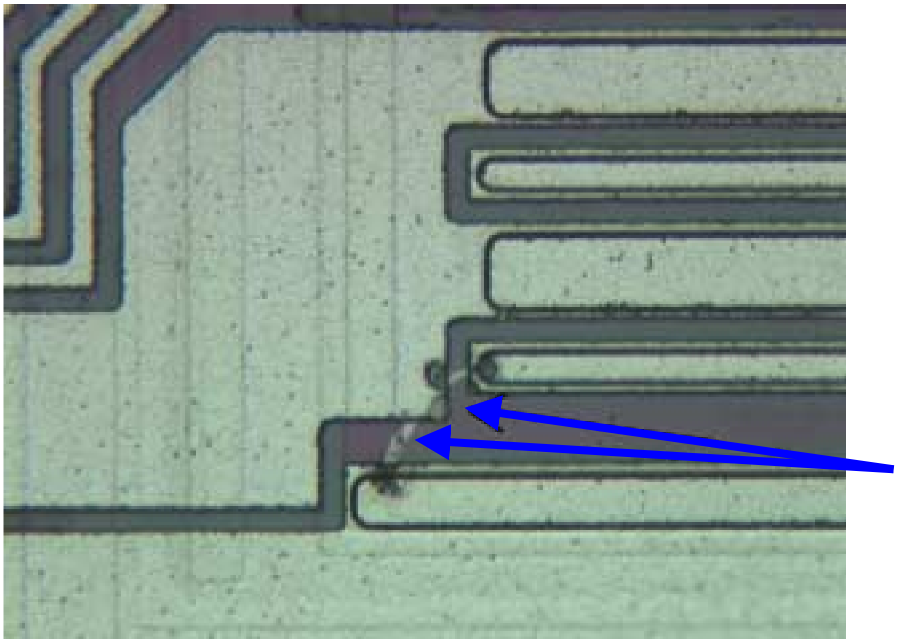


Figure 13: Optical microscope image of EOS damage at a bipolar output transistor. Note the dark "burn marks" where the aluminum metallization melted and reflowed, forming a white "arc track" that shorted-out the transistor.

Design for EOS/ESD Protection

ADI uses proprietary and/or patented on-chip protection circuitry to maximize the robustness of our products to EOS/ESD transients at all pins. ADI products use a broad range of EOS/ESD protection circuitry, depending on the wafer fabrication process and the electrical performance requirements of each pin on the product. ADI's ICs are typically designed with an individual protection circuit immediately adjacent to each non-substrate bond pad. An "ideal" protection circuit functions as a perfect switch that is:

- Always electrically open (i.e., having infinite resistance, zero capacitance, and zero inductance) during normal IC operation
- Instantaneously electrically closed (i.e., having zero resistance, zero capacitance, and zero inductance) in response to an EOS/ESD transient.

However, due to fundamental device physics, no matter how well a protection circuit is designed, it is never a perfect switch. More specifically, a protection circuit is a source of parasitic leakage current, capacitance, and inductance during normal IC operation. In addition, all protection circuits have a finite turn-on time in response to an EOS/ESD transient, and have finite on-resistance. These non-ideal characteristics make the design of protection circuits very challenging, especially for high-performance ICs. ADI has responded to this challenge by using teams of ESD engineers, device engineers, design engineers, layout engineers, failure analysis engineers, and reliability engineers to develop many innovative and effective protection circuits for our products.

As an example, Figure 14 shows a generic "H-network" protection circuit for I/O pins comprised of four Protection Devices (PD1 through PD4) and a series resistor (R). PD1 and PD2 provide primary protection, while PD3 and PD4 provide secondary protection. The function of PD1 and PD2 is to "steer" as much of the EOS/ESD current as possible to one of the supply rails (V+ or GND). Series resistor R slows-down very fast transients that may not have been adequately attenuated ("clamped") by PD1 or PD2, and it also limits the magnitude of the residual current that is not diverted to a supply rail by PD1 or PD2. This residual current is then diverted to a supply rail by one of the secondary protection devices, PD3 or PD4.

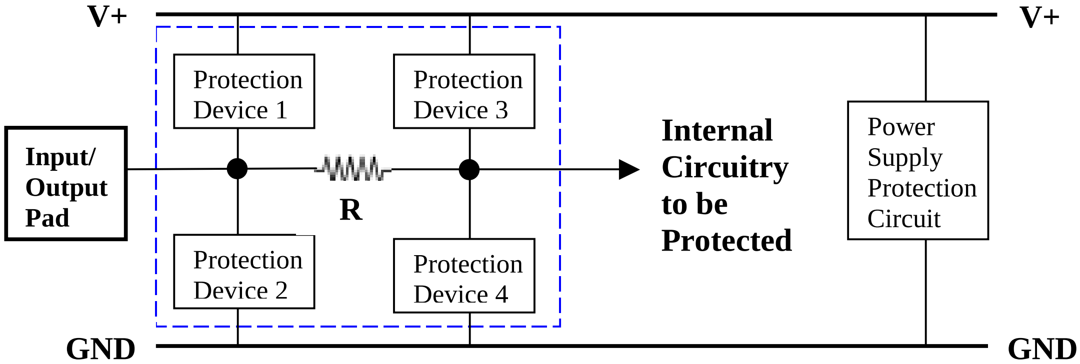


Figure 14: The dashed blue box shows a generic on-chip "H-network" EOS/ESD protection circuit used on Input/Output pins.

To be fully effective, on-chip EOS/ESD protection circuitry must be included for all pin combinations subject to possible transients. For example, the circuitry shown in Figure 14 provides protection to the I/O Pad as follows:

- A positive transient at the I/O Pad with respect to V+ turns-on PD1 and PD3, thus conducting the EOS/ESD current to V+ and protecting the internal circuitry. (Note that most of the current is "steered" through PD1 since resistor R limits the current through PD3.)
- A positive transient at the I/O Pad with respect to GND turns-on the Power Supply Protection Circuit as well as PD1 and PD3. (Again, most of the current is conducted by primary protection device PD1.) EOS/ESD current then safely flows from the I/O Pad to V+ and then to GND, thus protecting the internal circuitry.
- A negative transient at the I/O Pad with respect to GND turns-on PD2 and PD4. (Most of the current is "steered" through PD2 since R limits the current through PD4.) EOS/ESD current then safely flows from the substrate (GND) out the I/O Pad, thus protecting the internal IC circuitry.
- A negative transient at the I/O Pad with respect to V+ turns-on the Power Supply Protection Circuit as well as PD2 and PD4. (Again, most of the current is conducted by primary protection device PD2.) EOS/ESD current then safely flows from V+ to GND and then out the I/O Pad, thus protecting the internal IC circuitry.

Summary

ADI is committed to developing and releasing ICs that have high levels of robustness to electrical overstress (EOS) transients, including electrostatic discharge (ESD). All new products are tested to the Human Body Model (HBM) and the Field Induced Charged Device Model (FICDM). ADI uses stringent methods for this HBM and FICDM testing, consistent with the latest industry standards. Any new product that does not meet ADI's targets for ESD robustness is subjected to failure analysis to identify the failure site and exact failure mechanism. This information is then used to redesign the product and to update IC design and layout rules so that future products will consistently achieve high levels of EOS/ESD robustness. ADI's expertise in on-chip EOS/ESD protection circuitry is demonstrated by our broad portfolio of patents in this area. More importantly, our continuous focus on maximizing the robustness of our products has resulted in a downward trend in the number of customer returns due to EOS/ESD damage.

[1] MIL-STD-833 Method 3015.7, "Electrostatic Discharge Sensitivity Classification."

[2] ESD-STM5.1-1998, "ESD Association Standard Test Method for Electrostatic Discharge Sensitivity

Testing: Human Body Model (HBM) – Component Level," ESD Association, Rome, NY, 1998.
[3] EIA/JEDEC Test Method A114-A, "Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)," Electronic Industries Association, 1997.

[4] ESD-STM5.2-1999, "ESD Association Standard Test Method for Electrostatic Discharge (ESD) Sensitivity Testing: Machine Model (MM) – Component Level," ESD Association, Rome, NY, 1999.

[5] T.S. Speakman, "A Model for Failure of Bipolar Silicon Integrated Circuits Subjected to Electrostatic Discharge," *12th Annual Proceedings, Reliability Physics*, pp. 60-69, April 1974.
[6] L.R. Avery, "Charged Device Model Testing; Trying to Duplicate Reality," *1987 Electrical Overstress/Electrostatic Discharge Symposium Proceedings*, ESD Association, Rome, NY.

[7] A. Olney, "A Combined Socketed and Non-Socketed CDM Test Approach for Eliminating Real-World CDM Failures," *1996 Electrical Overstress/Electrostatic Discharge Symposium Proceedings*, ESD Association, Rome, NY.
[8] ESD-DS5.3.1-1996, "ESD Association Draft Standard for Electrostatic Discharge Sensitivity Testing: Charged Device Model (CDM) Non-Socketed Mode - Component Level," ESD Association, Rome, NY, 1996.

[9] EIA/JEDEC Test Method C101, "Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components," Electronic Industries Association, 1995.

[10] IEC 61000-4-2 (1995-01), "Electromagnetic Compatibility (EMC) – Part 4: Testing and Measurement Techniques – Section 2: Electrostatic Discharge Immunity Test," International Electrotechnical Commission, Geneva, Switzerland, 1995.

[11] IEC 61000-4-4 (1995-01), "Electromagnetic Compatibility (EMC) – Part 4: Testing and Measurement Techniques – Section 4: Electrical Fast Transient/Burst Immunity Test," International Electrotechnical Commission, Geneva, Switzerland, 1995.

[12] EIA/JEDEC Test Method C101, "Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components," Electronic Industries Association, 1995.

[13] ESD ADV-2.0-1994, "ESD Association Advisory for Protection and Sensitivity Testing of Electrostatic Discharge Susceptible Items – Handbook," ESD Association, Rome, NY, 1994.

[14] N. Lyne, "Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Reoccurrence," Analog Devices, Inc. Application Note AN-397, 1995.
Available on the ADI Web Site at http://www.analog.com/techsupt/application_notes/AN-397.pdf.

[15] M. Byrne, "How to Reliably Protect CMOS Circuits Against Power Supply Overvoltaging," Analog Devices, Inc. Application Note AN-311, 1983.
Available on the ADI Web Site at http://www.analog.com/techsupt/application_notes/AN311.pdf.

[16] P.R. Bossard, R.G. Chemelli, and B. Unger, "ESD Damage from Triboelectrically Charged IC Pins," *1980 Electrical Overstress/Electrostatic Discharge Symposium Proceedings*, ESD Association, Rome, NY.