SONY

SONY SEMICONDUCTOR

Quality and Reliability HandBook

Quality and Reliability HandBook

Notes

- This handbook was created for the purpose of introducing Sony's approach toward maintaining and controlling semiconductor quality and reliability to customers who are currently using Sony semiconductor products and to potential customers who are considering their use in the future. It also aims for understanding of general points for caution when using Sony semiconductor products.

  Responsibility for quality assurance, defect warranties and other items relating to individual transactions shall conform to these sales contracts and other adjunct contracts concluded between the Sony Sales Department or Sony agents and customers, and this handbook shall not in any way add to or modify the contents of said contracts.

  Note that "quality assurance" as used in this text refers to the maintenance and control of semiconductor device quality and reliability, and differs from the quality assurance items in contracts.

- Sony makes the utmost efforts to improve the quality and reliability of its products, but semiconductor failure of a certain percentage is unavoidable. Therefore, we request that sufficient care be given to ensuring safe design in customer products such as redundant design, anti-conflagration design and design for preventing misoperation in order to prevent accidents resulting in injury or death, fire or other social damage from occurring as a result of semiconductor failure. In addition, be sure to consult your Sony sales representative beforehand when there is a chance that customer products manufactured using Sony products may pose a life- or injury-threatening risk or are highly likely to cause significant property damage in the event of such a failure.

- Sony reserves the right to change the contents of this handbook without notice. Be sure to check the latest information before using Sony semiconductor products.

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PREFACE

We would like to thank you for your continued patronage of Sony Semiconductor products.

We are pleased to announce the recent completion of this Sony Semiconductor Quality and Reliability Handbook which summarizes Sony's approach and the results of research on semiconductor quality and reliability.

The Sony Semiconductor Network Company offers a collection of the finest technology to customers, and supplies semiconductor products which form the basis of key technologies in various industries. All departments from Product Planning to Design, Manufacturing, Evaluation and Service are united in their efforts to ensure quality and reliability capable of satisfying each and every customer around the world.

This handbook aims to introduce and achieve widespread understanding of Sony's approach toward semiconductor quality and reliability as well as points for caution when using Sony semiconductor products, and it is our sincere hope that it will prove useful as a guidebook for quality and reliability assurance for our customers. As such, it is intended for use together with previously published data books, manuals and other materials.

The greatest care was taken in the compilation of this handbook. However, please contact Sony Corporation if you find any errors, omissions or unclear points. Your comments would be greatly appreciated.

October, 2000

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Semiconductor Network Company
Sony Corporation

Quality and Reliability Hand Book

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CHAPTER 1 - QUALITY ASSURANCE FOR SEMICONDUCTOR DEVICES

1.1 Approach toward Quality Assurance

1.1.1 Basic Policies

The Sony Group is not content simply to improve product and service quality, and is instead deploying company-wide activities to realize the world's top management quality in order to provide the highest level of satisfaction in all aspects to our customers. As a member of the Sony Group, the Semiconductor Network Company is charged with the development, design, manufacture and sale of semiconductor products.

Within the Sony Semiconductor Network Company as well, all divisions, related departments and factories hold the basic policies of "the customer first" and "providing top level quality" with the aim of realizing the "No. 1 customer satisfaction in the world". To achieve this, the Semiconductor Network Company constantly strives to improve the quality of its semiconductor products through activities such as maintaining and improving ISO 9000 Series and QS-9000 quality systems, improving work process performance through Six Sigma activities, and improving product quality through various scientific approaches.

1.1.2 ISO 9000 Series and QS-9000

1.1.2.1 Construction of a Quality System Based on the ISO 9000 Series

As semiconductor product structures become increasingly complex, customer expectations toward quality are becoming even stricter. Customer requirements are generally incorporated into Specifications, but even with perfect Technical Specifications, if the systems of the organization supplying the product contain defects, then the Specifications alone cannot be considered capable of continuously satisfying customer requirements.

The Sony Semiconductor Network Company has promoted the successive acquisition of ISO 9000 Series certification since fiscal 1993. The ISO 9000 Series is an international standard concerning quality assurance and quality control systems, and currently all divisions and factories have acquired either ISO 9001 or ISO 9002 certification.

The following control is carried out through "process management", which is the basic concept for the ISO 9000 Series.

- Work structures (work flow) through which products flow
- Quality of products flowing through these structures (work flow)

This control makes it possible to create and supply products with stable quality to customers, thereby meeting customer demands and firmly establishing trust in Sony Semiconductor products.

The Sony Semiconductor Network Company's quality system document system was constructed based on ISO 9000 Series requirements. This system and our basic approach toward maintaining and improving quality systems are described below.

(1) Quality document system diagram (Fig. 1-1)

The quality system is stratified and compiled into documents with quality manuals at the top supported by regulations, rules, procedures and detailed work standards, etc.

(2) Quality system maintenance and improvement (Fig. 1-2)

Employees are trained and keep records of duties carried out according to prescribed methods based on the latest documents to ensure that the constructed quality system is implemented in the prescribed manner.

The quality system is periodically checked and evaluated though systematic internal quality audits and audits by ISO certification agencies to provide opportunities for improvement.

Fig. 1-1 Quality Document System

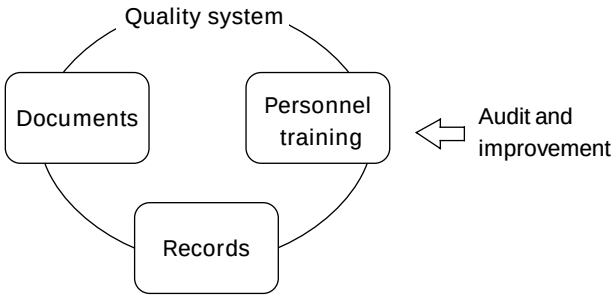


Fig. 1-2 Quality System Maintenance and Improvement

As shown above, the Sony Semiconductor Network Company works to continuously improve processes and performance by reliably implementing and periodically reviewing the constructed quality system.

1.1.2.2 Deployment to QS-9000 Certification Activities

The Sony Semiconductor Network Company is conducting activities with the aim of acquiring QS-9000 certification during fiscal 2000 in order to further increase the effectiveness of the quality system constructed with the ISO 9000 Series.

QS-9000 is the standard required of primary suppliers by America's "Big Three" automotive manufacturers (General Motors, Ford and Chrysler), and this certification must be acquired to supply parts to the Big Three. QS-9000 is based on the ISO 9000 Series, and more clearly delineates the concept of working for both the customer's and one's own benefit to ensure customer satisfaction by carrying out constant improvements which focus on preventing defects in the supply chain and reducing "variance" and "waste". QS-9000's effectiveness is acknowledged and its adoption has begun to spread rapidly to automotive manufacturers other than the Big Three mainly in North America and Europe.

The Sony Semiconductor Network Company is working to improve customer satisfaction and realize the No. 1 customer satisfaction in the world by incorporating and implementing the concepts in this standard.

1.1.3 Six Sigma

Six Sigma activities

The Sony Group is working to improve product and service quality and to continue providing the highest level of satisfaction to our customers. Using the Voice of Customers (VOC) as a starting point, we have systematized conventional QC and TQC activities in a more scientific and logical manner, and are introducing and deploying reconstructed Sony Six Sigma activities on a company-wide basis in order to realize the highest management quality at the 6 σ level.

Within the Sony Semiconductor Network Company as well, all divisions, related departments and factories have introduced and are working to actively utilize Six Sigma activities in an organized manner. We are continuing our efforts to improve the quality of our semiconductor products with the targets of "providing top-level quality and solutions" and "achieving the No. 1 customer satisfaction in the world".

Sony Semiconductor Network Company - Sony Six Sigma basic policy and activity guidelines

Aim:

Sony Six Sigma aims to hold the "maximization of customer satisfaction and creation of customer values" as a shared value, to establish Win-Win relationships with customers, and to make a culture of learning take root in order to further improve management quality.

Basic policy:

Sony Six Sigma will be positioned as a shared management tool, and efforts will be made to firmly establish a culture of learning and to scientifically and rationally achieve Customer Satisfaction through the in-depth application of this culture.

Activity guidelines:

(1) Correctly understanding the Voice of Customers (VOC), setting important themes to be resolved as Critical to Quality (CTQ), appropriately breaking down these CTQ, deploying and reliably executing specific projects in an organized manner, following up in an organized and vigorous manner to achieve targets, and reducing all Costs of Poor Quality (COPQ) in corporate management activities.

(2) Solving Critical to Quality (CTQ) with the Six Sigma Approach (D-MAIC).
- D-MAIC = Define - Measurement - Analysis - Improvement - Control
- D = Define (Correctly recognizing VOC, extracting CTQ and setting themes = projects)
- M = Measurement (Understanding themes)
- A = Analysis (Analyzing themes)
- I = Improvement (Improving themes)
- C = Control (Constructing systems to ensure that improvement effects take root)

(3) Reliably carrying out quality planning, design review, and confirming design validity. Producing and supplying high quality products by reliably executing work according to the quality system.

(4) Working to "Look realistically at real objects in real situations" in all aspects, analyzing data using scientific methods, performing appropriate statistical processing to allow correct judgment of the obtained data, and then using this data to make swift improvements.

1.1.4 Scientific Approach

In order to build in stable quality in the semiconductor device design and manufacturing processes, the Sony Semiconductor Network Company takes a scientific approach and uses various statistical techniques in each process.

In addition, we have introduced Six Sigma to our training curriculum and are working for widespread understanding of these concepts in order to achieve effective improvements.

As examples, the Statistical Process Control (SPC) performed mainly in the manufacturing process and the Failure Mode and Effects Analysis (FMEA) performed in the design and manufacturing processes are described below.

1.1.4.1 Statistical Process Control (SPC)

The manufacturing process is controlled using check sheets, graphs, control diagrams and other control tools. In particular, control diagrams are an effective means for continuously monitoring changes in process quality for each process, and make it possible to take proper action when trouble occurs.

Control diagrams set control limits (average $\pm 3\sigma$) indicating the range of normally occurring data based on the variance σ of process data over a certain range, and enter measurement data onto record charts.

When an abnormal factor enters the process variance, the data exceeds the control limit lines, so control

charts are effective for quickly detecting process changes. In addition to detecting when the data exceeds the control limit lines, process changes such as rising and falling data trends can also be detected.

The use of control diagrams and other statistical techniques helps to quantitatively understand and analyze variance which affects quality, and is useful in improving quality.

Specifically, first the important control items are determined based on the characteristics items demanded by customers, items affecting device quality and reliability, and items which correlate with defect mechanisms, etc.

Capability measures (Cp, Cpk) are calculated for each process based on these items, and process improvements are then carried out for items with low process capability measures levels to achieve higher level values and realize stable quality.

Process capability measures

The process stability with respect to the standards for that process can be obtained from the process data over a certain period and the standard values. These are called process capability measures (Cp, Cpk), and are obtained by the following formulas.

$$Cp = \frac{\text{(Standard upper limit - Standard lower limit)}}{6\sigma}$$

(Process capability measures in consideration of data (average value) bias toward the standard center)

$$Cpk = \frac{|\text{Standard limit closest to the average value - average value}|}{3\sigma}$$

The Semiconductor Network Company works to improve process variance by periodically understanding these process capability measures.

1.1.4.2 Failure Mode and Effects Analysis (FMEA)

Failure Mode and Effects Analysis (FMEA) consists of confirming and evaluating the risks posed by the failure modes which are latent in devices or processes.

Confirming these risks makes it possible to systematically discover what is necessary to eliminate or reduce decisive trouble and achieve an optimum design.

Table 1-1 shows a simplified example of FMEA applied with the purpose of improving quality in a wafer manufacturing process.

In this example, two modes are given as failure modes.

First, a number representing the seriousness of the problem is assigned to the Seriousness column. Next, a number representing the probability of occurrence, that is to say the degree of possibility of that problem occurring, is assigned to the Frequency column. Then, a number representing the degree of possibility of a detection miss is assigned to the Detection level column.

The result of multiplying of these three numbers is entered to the Priority column, and this number can be used to rank the risk of each problem in order from high to low.

The conclusion reached in this example is that measuring the positioning accuracy is the most important matter which should be investigated.

The next step in FMEA is to brainstorm as to the possible causes of these problems and formulate action plans for foolproofing or eliminating the problems.

Then, improvements are carried out based on the formulated action plans.

Table 1-1 FMEA Example

Product or Process	Potential Failure Mode	Potential Effect(s) of Failure	Severity	Potential Cause(s)	Occurrence	Current Design Controls	Detection	Risk Priority Number (RPN)	Recommended Actions - Important Items	Countermeasures and Plans
1PC process	Withstand voltage defect	Isolation deterioration	4	High channel density	2	Channel density control	3	24	4	Increase the EQC frequency of the injector.
										Introduce an annealing activation rate control process.
				Small gate-drain interval	4	Positioning accuracy measurement	3	48	1	Increase the number of measurement points and strengthen the screening.
										Adjust the stepper.
										Review the positioning method and mark structure.
				Short circuit caused by particles	1	Particle control	3	12	5	Review the equipment dust control method.
										Reduce floor dust.
	Large wiring resistance	Insertion loss deterioration	3	Thin wiring metal thickness	3	Thickness measurement	5	45	2	Introduce thickness measurement using a dummy wafer.
				Narrow wiring width	3	Line width measurement	4	36	3	Introduce TEG for line width measurement.
										Review the stepper exposure conditions.
										Introduction of dye-containing photoresist.
	....	....	...	....	...	....	...	...	....	....

1.1.5 Approach toward Quality Certification

As shown in Fig. 1-3, the reliability of prototypes is evaluated mainly through accelerated life tests, and the quality is certified in order assure the quality of semiconductor products.

With recent trends toward small-lot production of multiple items such as ASIC, it is not feasible to perform all evaluations for each individual product.

The approach adopted by the Sony Semiconductor Network Company is to divide semiconductor product reliability into the three areas of wafer process technology, circuit technology and packaging technology, and to evaluate each individually.

Regarding wafer process technology, basic reliability is evaluated for each major technology such as the 0.5 µm or 0.35 µm generations, and the process is certified. This assures the basic reliability of each semiconductor product manufactured using that wafer process technology.

The circuit technology of each individual product is checked from the viewpoint of reliability as to whether new or special circuits are used or whether special operating conditions are required, etc. Then the differences from the basic technology are clarified and only the reliability evaluation which is thought to be necessary is added.

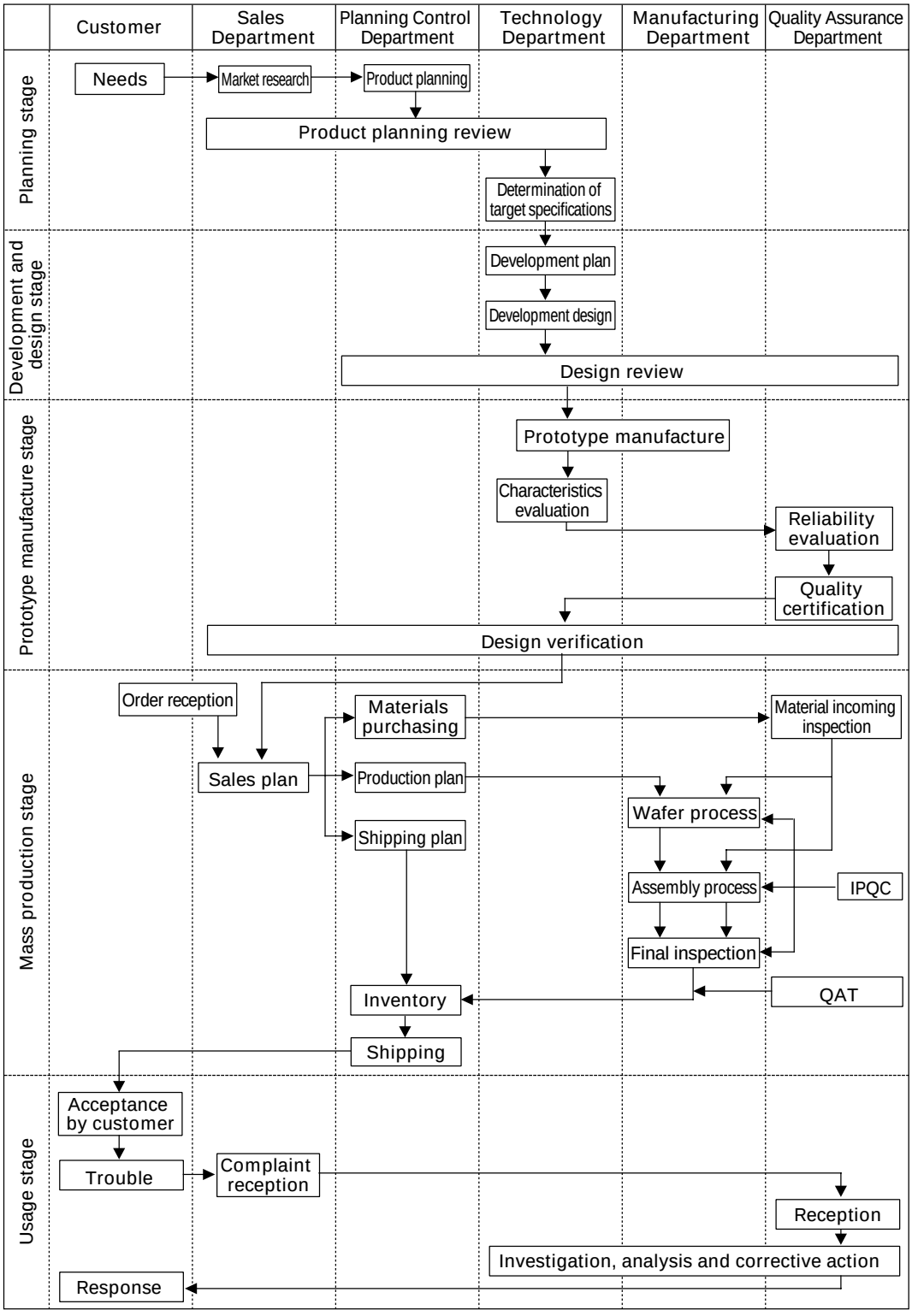
For packaging technology as well, in contrast to general plastic packages such as conventional LQFP and QFP, when developing and manufacturing packages with new structures such as CSP (Chip Size (Scale) Package), the basic reliability is evaluated and the package is certified. This assures the basic reliability of each semiconductor product manufactured using that packaging technology.

In this manner, quality certification of Sony semiconductor products is based on the certification of basic technologies such as process certification and package certification.

1.2 Quality Assurance System for Semiconductor Devices

To ensure quality and reliability and to supply products which meet customer needs in a timely manner, all Sony Semiconductor Network Company departments carry out activities based on a consistent quality assurance system from the product planning stage through development, design, manufacture of prototypes, evaluation, mass production, shipping, market and service.

Fig. 1-3 shows the Sony Semiconductor Network Company's quality assurance system.



IPQC : In Process Quality Control QAT : Quality Assurance Test

Fig. 1-3 Quality Assurance System Diagram

1.2.1 Quality Assurance in the Development Stage

1.2.1.1 Product Planning

Before starting product planning, it is essential to carry out market research activities to ascertain the intended applications and the product quality and reliability demanded by each customer, and also to understand technical trends in the general marketplace, basic specifications, delivery periods, prices, quality, reliability and other demands on products.

Information on demanded quality and reliability acquired through the above activities and various data obtained in-house from accumulated quality and reliability results and fundamental research on reliability technology are used to set target quality and reliability levels which are appropriate for product applications and operating environments and to formulate development plans.

This information is then compiled into product plans, and design specifications are drawn up based on these product plans and summarized as input for design.

1.2.1.2 Product Development and Design

Product design is an extremely important process for ensuring high reliability in semiconductor devices, and it is necessary to build in both quality and reliability.

Product design should incorporate reliability in all aspects based on design specifications which have been thoroughly investigated in the planning stage. For example, circuit and layout designs should have sufficient design leeway to tolerate variance in the manufacturing process.

Product design work proceeds according to the design specifications. These design specifications include design inputs (applicable laws and regulations, customer demands, in-house standards) to ensure that appropriate requirements are selected. Product design passes through the stages of logic/circuit design, layout design, mask design, prototype manufacture and evaluation before reaching completion. In addition, reliability evaluation to assure quality and reliability levels, design review and design verification are carried out at strategic points throughout this process to confirm that the design input requirements are satisfied.

Design review consists of reviewing design results with the aim of improving design quality. Design verification checks that products meet needs and customer requirements using input documents (design specifications), output documents (evaluation data), related reports and other materials. In addition, production drawings and preparations are checked, products are approved as mass production types, and procedures for starting mass production are initiated.

1.2.1.3 Design Review

The product design results and observance of the design specifications used as these inputs are checked as the design review. Design review may also be carried out partway through the design work and these results fed back to the design to improve design quality.

Design review consists of checking whether the design standards which are the rules to be followed during circuit design, layout design and assembly are being observed, and thorough investigation of design data by technical experts. Observance of design standards is checked using various simulation tools during circuit and layout design, and the design results are automatically and manually verified against the design standards to check whether there are any design errors, design standard violations or problems with product performance.

In addition, experts from related departments review designs from various angles using checklists which include design standards, cases of past trouble, etc. These design reviews aim to avoid trouble after prototype manufacture and mass production, and build the target performance, quality and reliability into products in line with demands.

1.2.2 Quality Assurance in the Mass Production Stage

1.2.2.1 Process Quality Control in Manufacturing

In order to supply the high quality and high reliability products demanded by customers, related departments perform capacity verification with respect to production, shipping and material purchasing plans which have been created based on the latest sales plan, and then operations shift to the production stage.

Based on the concept of building in quality in the manufacturing process, the manufacturing conditions (process conditions, facility conditions, manufacturing environment conditions, workmanship criteria, etc.) which have been determined according to the various drawings presented from the Development and Design Departments are prescribed in the work standards, and standard upper and lower limit control is performed as In Process Quality Control (IPQC). Then, SPC control (see 1.1.4) is carried out for important control items which have a significant effect on quality, and efforts are made to stabilize quality and to discover and prevent trouble. (Fig. 1-4)

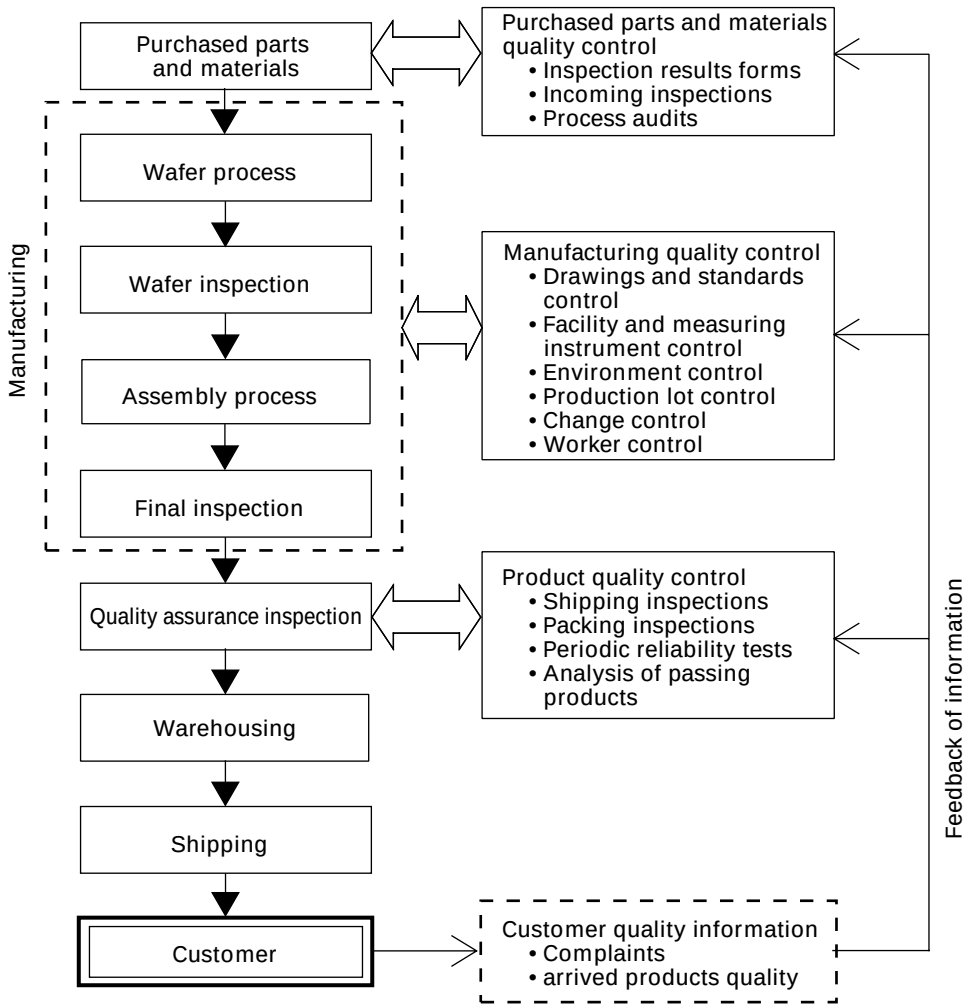


Fig. 1-4 Quality Control Flow in the Mass Production Stage

All necessary information concerning quality, from materials and parts purchasing to quality control, manufacturing process control, inspections, warehousing and quality conditions at the customer's place, is controlled by a data collection system and used to make swift quality improvements. When trouble occurs in the manufacturing process, a trouble report is issued, the Technology Department in charge investigates the matter, and action is taken to correct the problem and prevent recurrence. (Fig. 1-5)

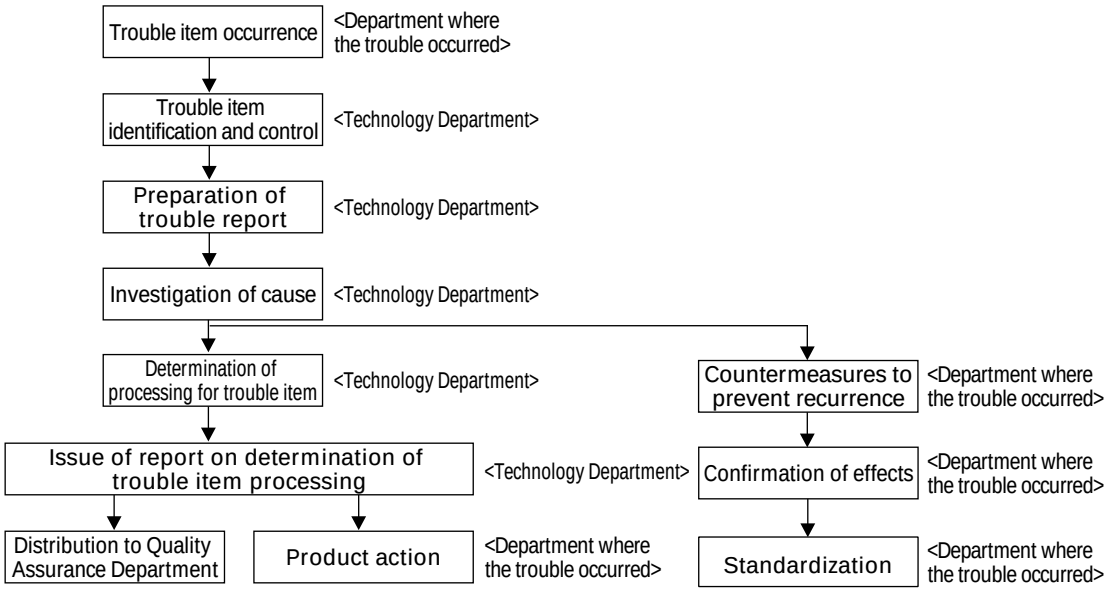


Fig. 1-5 Trouble Item Occurrence and Corrective Action

In this manner, a final inspection is carried out to check whether manufactured products satisfy product specifications and customer demands, and only passing products are shipped to customers.

1.2.2.2 Process Quality Control for Outsourced Items

Even when outsourcing part of the manufacturing process, quality assurance activities are promoted based on the same approach for both in-house production lines and outsourced production lines. These activities include product quality, process control, quality improvement activities and measures when trouble occurs, and efforts are made to maintain and improve product quality and to prevent the occurrence of trouble. (Fig. 1-6)

- **Certification of product quality**

Outsourced production items undergo the same quality and reliability evaluations as in-house production items as "quality certification" to make sure there are no problems.

- **Line audits**

Line audits are conducted by specialists when starting outsourced production to make sure there are no problems, and production starts after this "line certification".

- **Measures when trouble occurs**

When trouble occurs in outsourced production processes, product and corrective actions are carried out according to the decisions of related in-house departments based on information provided from the outsourcing supplier.

- **Periodic quality meetings**

Periodic quality meetings are held with outsourcing suppliers, and quality improvement activities are promoted. These activities include extracting themes such as trend control for process control items and inspection passing rates, and correction and prevention of problems.

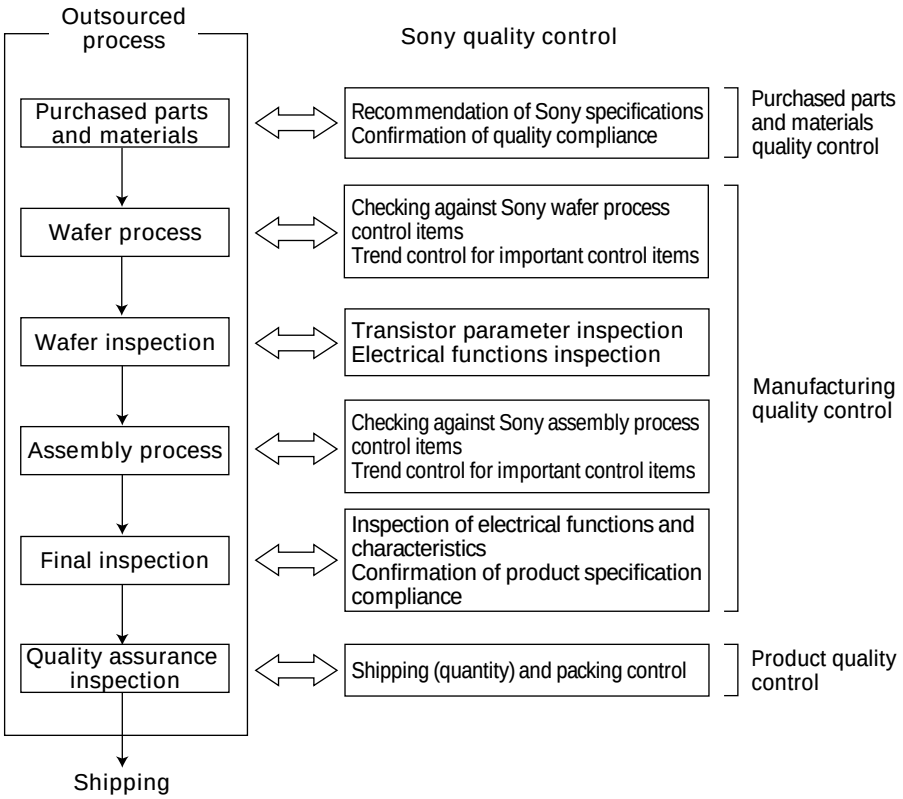


Fig. 1-6 Process Quality Control Flow for Outsourced Items

1.2.3 Quality Assurance for Materials and Parts

As semiconductor devices move toward higher performance and higher density, design demands on materials and parts are also becoming higher level.

On the other hand, it hardly needs mentioning that materials and parts quality is important for assuring the quality of semiconductor devices.

The Sony Group system includes supplier and manufacturer evaluation and registration, certification inspections and evaluation of materials and parts, and overall evaluation as semiconductor devices, etc. Within this system, Sony promotes activities to assure materials and parts quality, and purchases materials and parts which meet high level design demands. These procedures are shown in Fig. 1-7.

Specific activity contents are as follows.

- Selection of manufacturers based on demanded materials and parts specifications.
  Manufacturers are selected mainly by the Development and Purchasing Departments according to materials and parts functions and performance.
- Evaluation and registration of suppliers
  “Management”, “technology”, “quality”, “price” and “delivery period” are evaluated and registered mainly by the Purchasing and Quality Assurance Departments, and this information is shared by the Sony Group.
- Review and certification of manufacturers (factories)
  “Quality systems” and “process quality control” are reviewed and certified mainly by the Purchasing, Quality Assurance and Development Departments, and this information is shared by the Semiconductor Group.
- Certification inspection and evaluation of materials and parts
  Lead frames and other mechanical parts are certified by inspecting the appearance and measuring the dimensions.
- Evaluation and certification of quality and reliability as semiconductor devices
  Items for which evaluation in material and part units is difficult are certified by overall evaluation as completed semiconductor devices.
- Registration and control of materials and parts purchasing data sheets
  These sheets are prepared by the Development Department, then individual numbers are assigned to each material and part and this data is registered and controlled by the Purchasing Department.
- Materials and parts incoming inspections
  These inspections are performed by the Purchasing Department (Quality Assurance Department) based on the purchasing data sheets.
- Materials and parts inventory and control
  This is performed by the Purchasing Department (Quality Assurance Department) based on the purchasing data sheets.
- Ensuring materials and parts lot traceability for semiconductor devices
  This is controlled by the Manufacturing Department as quality records within process control.
- Materials and parts change control
  Materials and parts changes are received by the Purchasing Department and verified by the Development and Quality Assurance Departments. Steps are taken to ensure traceability when making changes.

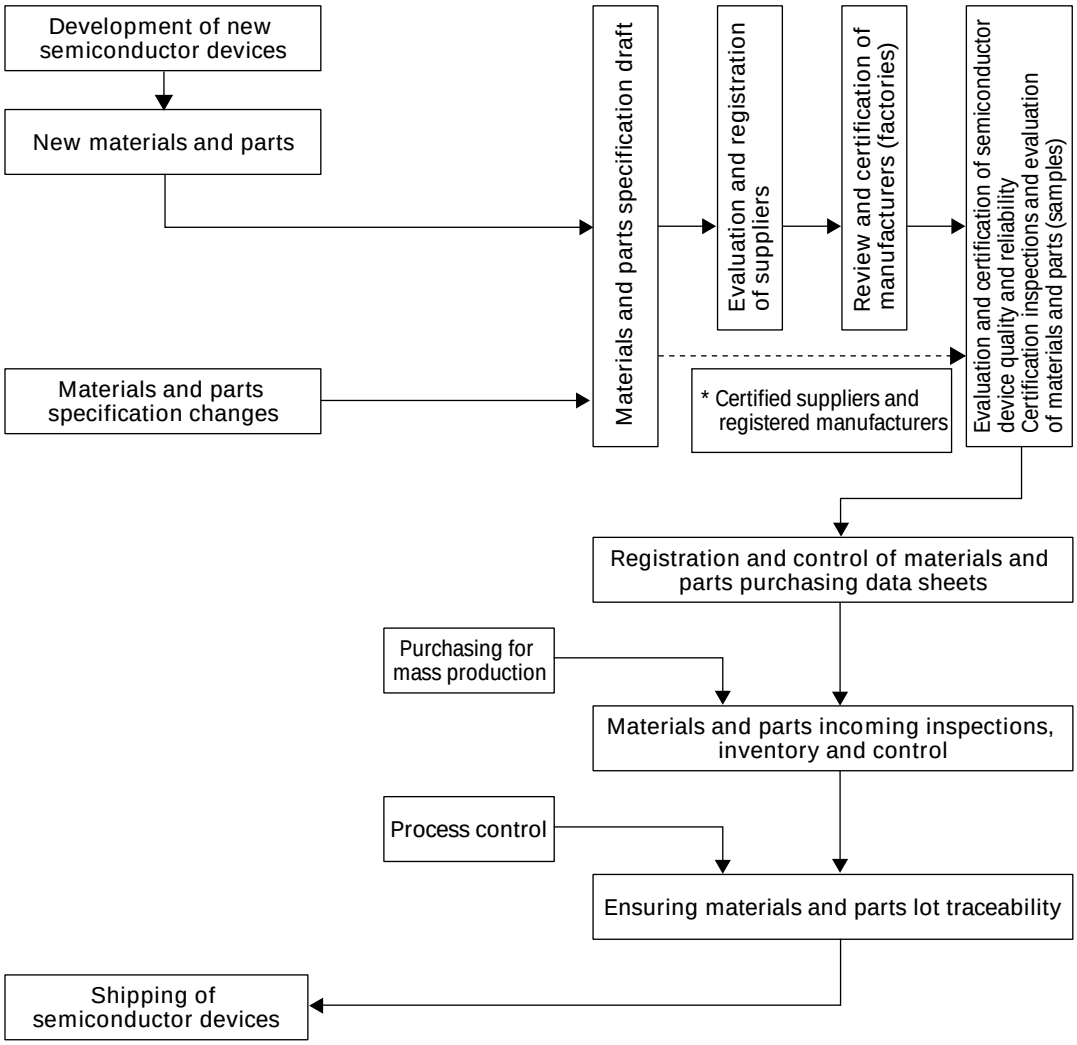


Fig. 1-7 Flow from Materials and Parts Development to Shipping

1.2.4 Facility and Measuring Instrument Control and Environment Control

During the course of semiconductor production, product performance and quality are assured and improved by having measuring instruments constantly operating in the normal condition and within the required accuracy.

Measuring instrument accuracy is controlled by establishing a preventative maintenance system. Incoming inspections are carried out when instruments are purchased and periodic inspections are carried out during use to check accuracy, calibrate instruments, and prevent malfunctions and drops in accuracy. Fig. 1-8 shows the quality control system for measuring equipment.

The environment has a significant effect on semiconductor device quality and reliability. Therefore, control items, control methods and control standards for temperature, humidity, dust and other items are set according to the manufacturing process and micro-machining level, and the environment is maintained and controlled by monitoring systems, etc. In addition, quality is also maintained and controlled by monitoring the specific resistance, purity and other characteristics of the deionized water, gases and chemicals used in manufacturing lines.

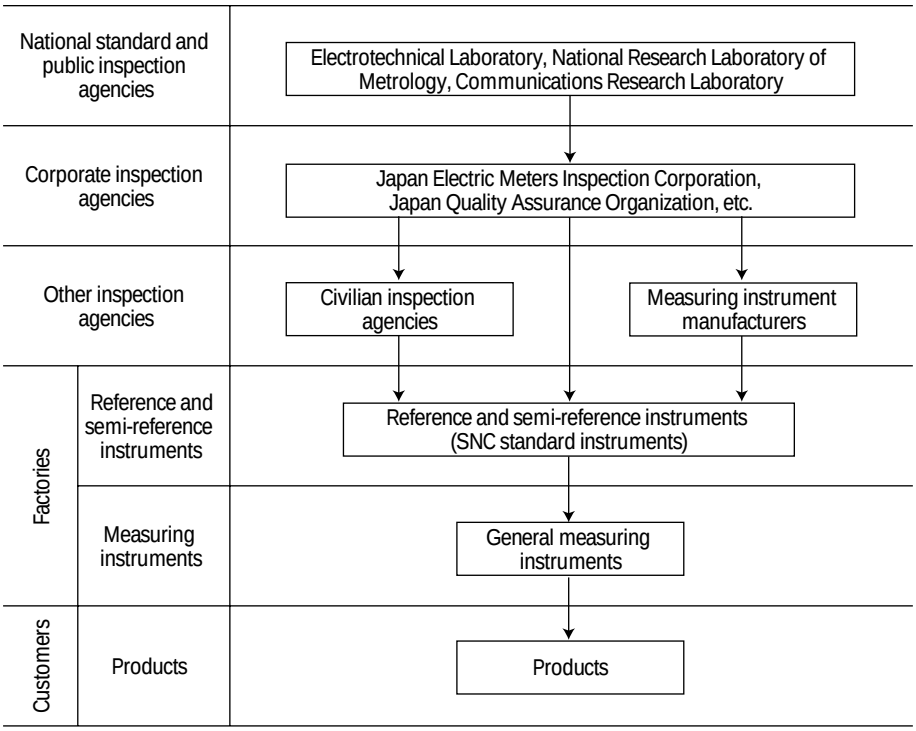


Fig. 1-8 Traceability of Measuring Instruments

1.2.5 Change Control

Changes are made to products or manufacturing process in order to improve semiconductor product functions, quality and reliability and also to improve productivity.

The feasibility of these changes is judged using sufficient data indicating that the change will not produce any negative effects.

When a change is planned, all related departments review the change. The necessary and ideal evaluation of items thought to have a technical effect is planned, and these effects are confirmed by manufacturing prototypes, etc.

In the case of changes which alter the product itself or changes to the manufacturing process which have a significant effect on the product, these results are conveyed in advance to customers to confirm that there is no effect at the customer.

After these judgments are received, if the change is acceptable, instructions are issued and initial control of floating data is performed as necessary for the final check.

This change system is shown in Fig. 1-9.

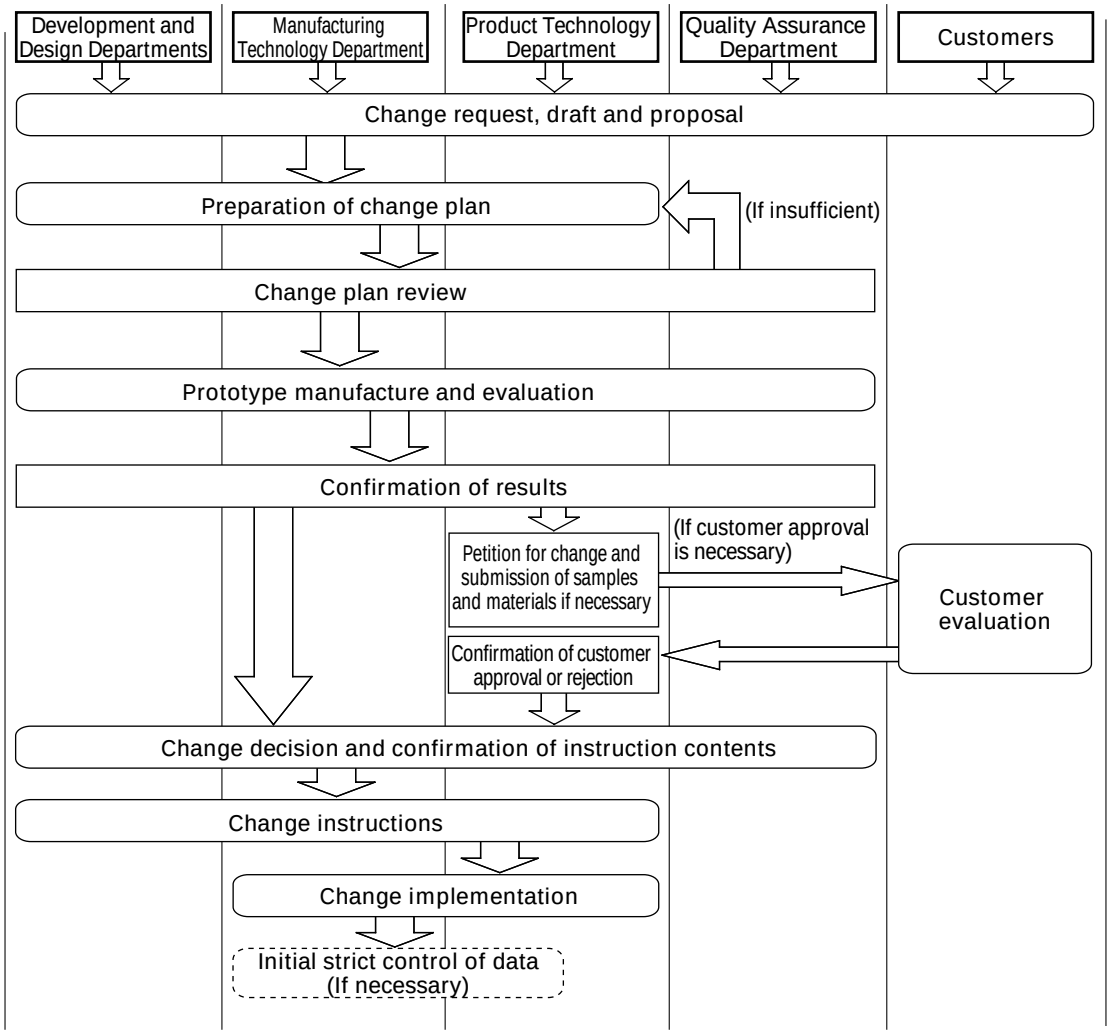


Fig. 1-9 Change System

1.3 Product Shipping Quality Assurance

Checks are carried out to ensure that the quality control established in the development and manufacturing stages is being reliably executed. Then, shipping inspections are carried out to confirm the quality assurance of each lot and periodic reliability tests are conducted in process and package units in order to ensure the quality and reliability of shipped products.

1.3.1 Quality Assurance Test (QAT)

Table 1-2 shows an example quality assurance inspection. The tested items are electrical characteristics, mechanical characteristics, thermal environment, reliability and long-term reliability.

Table 1-2 Example Quality Assurance Inspection

	Shipping inspection (Gp-A)	Mechanical strength test (Gp-B)	Periodic reliability test/other (Gp-C)	Long-term reliability test (Gp-D)
Frequency	Visual check: Lead bending, marking defects, chipping, voids, control defects Characteristics: DC and AC characteristics Packing: [Every lot]	Solderability S-Pd PPF products: each package category Solder plated products: each outsourcing supplier Soldering heat resistance [Once per month]	Representative types for sampling are determined each month from the wafer process family and the package family. Electrostatic strength test [Once per month]	One type from among the Gp-C tested items each month [Once per month]
Conditions	Visual check: IC visual inspection Judgment: AQL0.065 (0-1/200) Characteristics: FC standard Judgment: AQL0.065 (0-1/200) Packing: IC packing standard	Solderability: Sn/Pb : 230°C for 3 s Sn/Ag/Cu: 245°C for 3 s Judgment: Visual Soldering heat resistance: IR reflow Sony recommended temperature profile (Peak 260°C$_{max}$) Judgment: Visual, FC	HTB: 85°C to 125°C Test time max. 1008 h THB: 85°C, 85% RH Test time max. 1008 h TC: -65°C to +150°C Test time max. 100 cycles PCT: 121...C, 100% RH (unsaturated), 2.03 × 10^5 Pa Test time max. 236 h Electrostatic strength test: Machine model only	Same conditions as Gp-C HTB time: 5000 h THB time: 5000 h TC time: 500 cycles PCT time: 500 h
Quantity	Visual check: 200 pcs/lot Characteristics: 200 pcs/lot Packing: Entire lot	Solderability Soldering heat resistance: 96 pcs/lot	HTB 22 pcs, THB 22 pcs, TC 22 pcs, PCT 22 pcs/lot Electrostatic strength test	Continued from Gp-C: 1 lot per month

AQL: According to MIL-STD-105E/JIS Z9015
Sampling standard: According to MIL-S-19500 Sampling Inspection Table
(See Appendix Table A-5.)

S-Pd PPF: Sony specification palladium Pre-Plated lead Frame

1.3.1.1 Shipping Inspection

After the final inspection, sampling inspections are performed for each lot and a lot judgment is made to confirm that the electrical specifications, appearance and packing condition of shipped products satisfy the specifications demanded by customers.

1.3.1.2 Periodic Reliability Tests

Tests are carried out in process and package units to confirm that the reliability levels of shipped semiconductor products satisfy the levels demanded by customers.

1.3.2 Handling Customer Complaints

When a customer experiences trouble, these complaints pass through Sony's sales company and are received by the Quality Assurance Department.

Investigation and analysis of complaint items and feedback of these results are both a duty and a service to customers, and at the same time provide valuable information for improving product quality.

Results of investigations of complaint items and the contents of countermeasures are reported to customers in document form and efforts are made to obtain understanding. However, in some cases customers may be visited to report these results directly.

Fig. 1-10 shows an outline of the customer complaint handling flow.

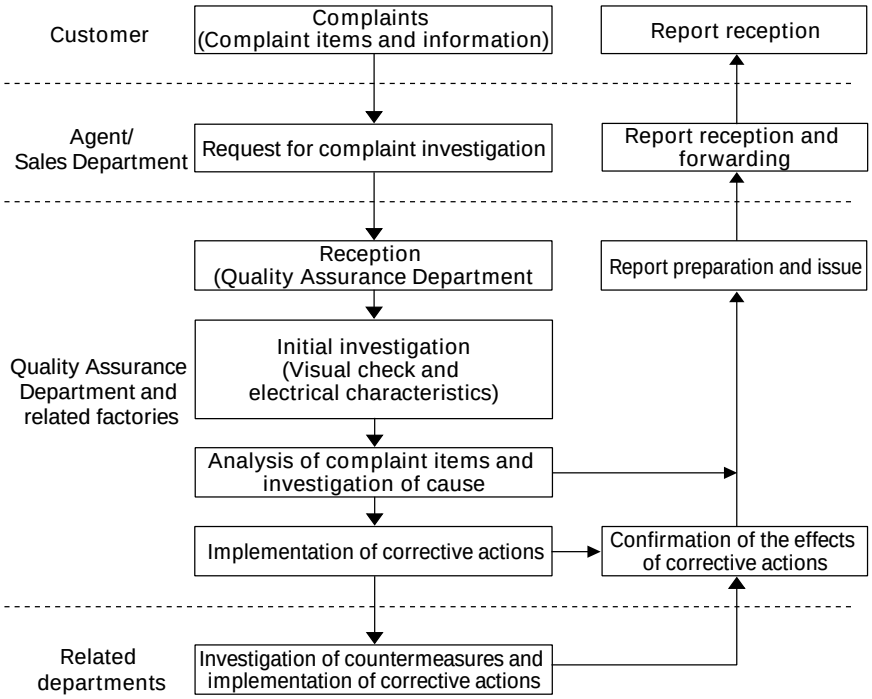


Fig. 1-10 Customer Complaints Handling Flow

1.3.2.1 Complaints Information

Complaints processing requires accurate information concerning the conditions under which the trouble occurred, and the more the information can be obtained from the customer, the easier the investigation and analysis can proceed. Therefore, when requesting investigation of complaint items, customers are requested to present detailed information on the trouble contents, the process in which the trouble occurred, the electrical, mechanical and thermal stress application history, lot dependency, occurrence rate, surrounding circuit conditions, applications, etc.

Particularly with lead bending and packing trouble (incorrect items or mixing of different types), detailed information at the time of occurrence is required.

1.3.2.2 Return of Complaint Samples

Complaint items should be returned as much as possible in the condition in which the trouble occurred.

When returning samples, appropriate measures should be taken to avoid external stress (electrical, thermal and mechanical) so that the effects of stress during handling and transport do not change the trouble conditions.

1.3.2.3 Return of Analyzed Samples

Items judged as acceptable or for which the complaint symptoms cannot be reproduced as a result of analysis by the Sony Semiconductor Network Company are returned to the customer for reconfirmation. If customers can reproduce the complaint symptoms, investigation should be requested again together with detailed information.

1.3.3 Corrective Action

After determining the cause from the complaint item investigation and analysis results, countermeasures are implemented and corrective action is also taken as necessary for the quality systems in each stage to prevent recurrence as shown in the example below.

(1) Evaluation and verification systems in the development and design stage
(2) Quality and reliability evaluation systems
(3) Control system for drawings, specifications and other data transferred from development and design to production
(4) Process internal quality control, trouble processing and facility control systems in the production stage

Taking corrective action for quality systems prevents the same kind of trouble from occurring in products other than the complaint item.

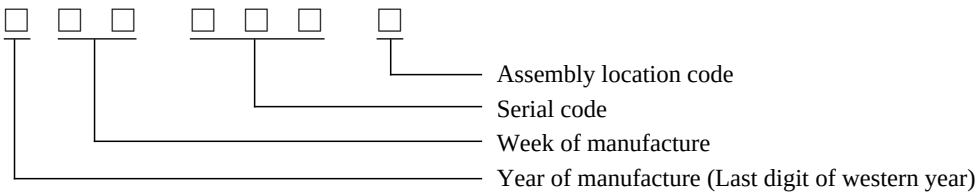
1.3.4 Product Identification and Traceability

Manufacturing history identification is controlled by assigning production lot numbers to allow tracing of the manufacturing history. Lot numbers are comprised of seven digits representing the year and week of manufacture, a serial code and a code indicating the assembly location. For small package items, this lot number is divided or omitted, and the full name is indicated on the shipping label.

(For details, see the item on Sony product name indications.)

1.3.4.1 Product Lot Indication (Traceability)

Full lot number indication



Divided indication

□ □ □ Year and week of manufacture
□ □ □ □ Serial code and assembly location code

1.3.4.2 Product Name Indication

Semiconductor devices are identified by naming and marking each product according to the Sony product name regulations for each category.

In principle the full name should be indicated, but since discrete devices have small packages, this indication is omitted in many cases.

1.4 Product Liability (PL) Act

1.4.1 Purpose of Activities

Sony carries out product liability (PL) activities under the name “Safety and Peace of Mind” activities.

Customer expectations toward safety and peace of mind are “to provide safe products and work together with customers to establish an environment in which products can be used with peace of mind”, and Sony’s mission is to realize customer satisfaction.

To fulfill this mission, Sony has prescribed the following basic guideline and policy for promoting safety and peace of mind, and the Sony Semiconductor Network Company has further established its own basic policy based on these.

Basic guideline

Sony will work to supply safe products and “make Sony the world reference” in the field of safe use by customers.

Basic policy

Sony recognizes that one of its most important management requirements is to conduct business activities aimed at realizing a “society where peopple can live safely and with peace of mind,” and will work to prevent accidents in all corporate activities. Furthermore, in the unfortunate event that accidents do occur, Sony will handle these incidents in a fair and swift manner.

Basic policy of the Sony Semiconductor Network Company

The Sony Semiconductor Network Company recognizes that one of its most important management requirements is to conduct business activities aimed at realizing a “society where people can live safely and with peace of mind,” and will “work through set customers which are direct customers to prevent accidents at the final customer.” Furthermore, in the unfortunate event that accidents do occur, the Sony Semiconductor Network Company will handle these incidents in a fair and swift manner.

1.4.2 Management Structure for Promoting Safety and Peace of Mind

The Sony Semiconductor Network Company promotes safety and peace of mind from the following starting points of PS, CS and PL.

(1) Product Safety (PS)

Supplying safe products

(2) Customer Satisfaction (CS)

Realizing safe use

(3) Product Liability (PL)

Fair and swift redress

1.4.3 Activities for Promoting Safety and Peace of Mind

(1) PS

The possibility of semiconductor products being the direct cause of death, injury or damage to property is extremely rare. However, semiconductor product quality or reliability failure in set products which use semiconductor products may trigger accidents in the final market.

The Sony Semiconductor Network Company feels that improving the quality and reliability of semiconductor products is the most important item for preventing PL accidents in set products, and works constantly to improve quality and reliability.

(2) CS

Product data sheets, catalogs, user manuals and other materials contain clearly marked notes on operation in order to prevent PL accidents resulting from improper use by customers such as use at voltages exceeding the absolute maximum rating.

(3) PL

In the event that quality or reliability failure of a semiconductor product causes a set product PL accident in the final market, efforts are made to respond swiftly to clarify the cause and prevent the damage from spreading.

We have established an emergency contact network in the event of a safety and peace of mind accident, and created an organization which allows responses on a 24-hour basis in order to effect this swift response.

1.4.4 Systems for Promoting Safety and Peace of Mind

The Sony Semiconductor Network Company has appointed Product Liability Authorized Reviewers (PLAR) as the final persons in charge of promoting safety and peace of mind in order to realize PS, CS and PL. In addition, systems for promoting safety and peace of mind have also been established, and implementation of action plans is monitored and corrective action taken.

CHAPTER 2 - FAILURE MECHANISMS 2

CHAPTER 2 - FAILURE MECHANISMS

2.1 Failure Modes and Mechanisms

Memory capacity is increasing steadily, and has reached the point where Giga (G) unit devices will soon be released.

In addition, multi-function system ICs which combine both memory and various logic circuits are replacing conventional single-function ICs as the main type of IC.

Increased capacity and multi-functions are transforming ICs, which were formerly just another component, into the core of system configurations. As such, the importance of ICs themselves is increasing, and the required reliability is also becoming extremely strict.

The keywords in this evolution of semiconductor devices are miniaturization, higher integration, and larger scale chips due to multi-functions.

In addition, the processes for realizing this evolution are also becoming more advanced and complex, and the failure modes could be said to include more complex factors.

Note that failure modes in semiconductor devices indicate symptoms such as open, short and leak defects, and failure mechanisms represent the course and mechanism for arriving at these symptoms. However, some failure modes are caused by compound mechanisms instead of just a single mechanism, so it is essential to investigate one factor at a time to determine the true cause. The Sony Semiconductor Network Company has established a loop by which the obtained failure mechanisms are swiftly analyzed, countermeasures are taken and feedback is provided in a systematic manner to allow mass production and ensure reliability.

Table 2-1 lists examples of mechanisms hypothesized from the failure modes.

2.2 Failure Mechanisms Rooted in Design and the Wafer Process

Table 2-2 shows typical failure mechanisms rooted in design and the wafer process.

As miniaturization of the wafer process advances, the design and process margins are tending to shrink due to the following factors. Therefore, it is thought that defects in the wafer process will increasingly affect device characteristics and reliability in the future.

1. Increased stress electric fields
2. Increased current density
3. Increased internal wiring stress
4. Multilayer wiring

Adequate steps are of course taken to ensure reliability in the prototype manufacture stage before semiconductor devices are shipped. However, semiconductor device quality can also be improved by performing sufficient process control within the wafer process.

Table 2-1 Example Failure Modes and Mechanisms

Failed part	Failure mode	Failure mechanism
Chip	Open	• Aluminum wiring disconnection (corrosion, migration, latch-up) • Bonding pad corrosion • Polysilicon wiring disconnection (melting) • Bond peeling (formation of Au-Al and other intermetallic compounds)
	Shorts or leaks	• Oxide film breakdown or pinhole • Electrostatic breakdown • PN junction degradation • Interlayer insulator breakdown or pinhole • Conductive foreign matter • Contamination within the process • Chip cracking • Entry of moisture
	IC function failure (characteristic fluctuation and function failure)	• Hot electron or hot carrier injection to the oxide film • Surface inversion • Crystal defect • Contamination within the process
	Malfunction	• Soft error • Latch-up • Electromagnetic interference (EMI)
Package	Open	• Bonding wire disconnection or peeling • Lead dirtiness, stress due to oxidation or absorbed moisture + heat stress
	Package cracking, shorts or leaks	• Delamination between the chip or lead frame and mold resin • Wire touching (contact between the wires, chip and lead frame) • Electrochemical migration between leads
	Soldering defect	• Surface contamination or oxidation

Table 2-2 Failure Mechanisms Rooted in Design and the Wafer Process

Failure mechanism	Primary factor	Failure mode
Hot carrier deterioration	Miniaturization of MOS transistor	Vth fluctuation, increased leak current
Time-Dependent Dielectric Breakdown (TDDB)	Reduced oxide film thickness	Increased leak current
Electromigration	Increased current density	Increased resistance value, open
Stress migration	Reduced wiring width	Increased resistance value, open
Soft error	α ray injection	Incorrect data rewriting

2.2.1 Hot Carrier

2.2.1.1 Description

MOS LSI have basically achieved widespread use today due to the establishment of the scaling rule approach.

The scaling rule was proposed by Dennard (IBM)[1)] in 1974, and concerns the proportional reduction of elements. In the 20-some years since its presentation, this rule has become the guiding principle for MOS FET miniaturization.

A typical scaling rule is the so-called “constant electric field scaling rule” shown in Fig. 2-1 by which both the element dimensions and the voltage are reduced by 1/k (k>1). As a result, not only does the element delay time become shorter (higher speed), but the power consumption also drops (low power consumption). In other

words, higher performance can be automatically achieved through miniaturization, making this an extremely superior method.

However, reducing the supply voltage with each generation causes various system problems, so scaling has actually been performed by “constant voltage scaling” which reduces element dimensions while maintaining the same voltage over multiple generations.

As a result, the electric fields inside MOS FET have grown with miniaturization, causing various problems. Typical problems include hot carrier effects described in this section and the time-dependent gate oxide film breakdown phenomenon described in 2.2.2.

Hot carrier effects are a phenomenon where a carrier (hot carrier) which has attained high energy due to acceleration by the electric field inside the MOS FET or other factors is injected to the gate oxide film, causing the MOS FET characteristics to fluctuate and the circuit to eventually stop operating normally. For this reason, hot carrier effects are suppressed by modifying the device structure, etc.

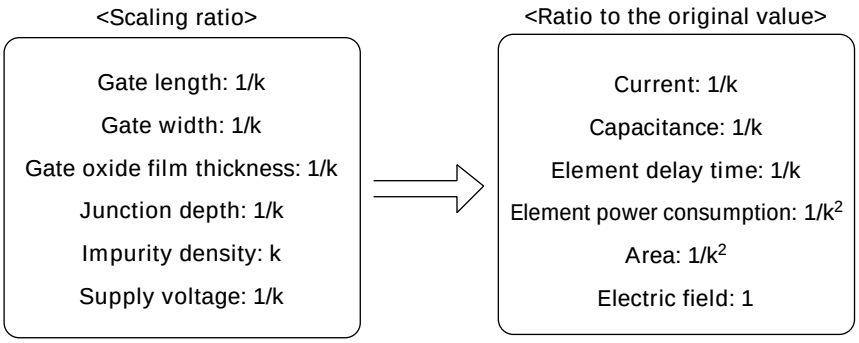


Fig. 2-1 Example of Constant Electric Field Scaling

2.2.1.2 Hot Carrier Generation Mechanism and Injection to the Gate Oxide Film

Hot carriers consist of high energy electrons (hot electrons) or holes (hot holes).

The hot carriers which exceed the energy barrier between the silicon substrate and the silicon oxide film are injected to the gate oxide film.

There are a number of types of generation mechanisms [2) 3)], and the particularly important ones are described below.

(1) Channel Hot Electron (CHE) injection [4)]

Electrons flowing from a source are accelerated by the high electric field near a drain, and of these the “lucky electrons” which do not experience energy-dissipating impacts are injected to the gate oxide film. This mechanism occurs most easily when the gate voltage and the drain voltage are equal ($V_{GS} = V_{DS}$).

(2) Drain Avalanche Hot Carrier (DAHC) [5) 6)]

Electrons flowing from a source undergo impact ionization due to the high electric field near a drain, and generate electron-hole pairs. Of these, the electron or the hole, whichever has the higher energy, is injected to the gate oxide film.

This mechanism occurs most easily when V_{GS} is approximately $\frac{1}{2}$ V_{DS} (the V_{GS} which provides the peak substrate current value). DAHC causes the greatest deterioration in MOS FET characteristics in the normal operating temperature range, and reliability is normally evaluated under this condition.

2.2.1.3 Electrical Characteristics Shift in MOS FET and Countermeasures

Typical electrical characteristics which fluctuate due to hot carriers injected to the gate oxide film include the threshold value Vth, transfer conductance gm and drain current I_{DS}. In the case of NMOS FET, Vth rises and gm and I_{DS} drop.

Reliability is basically evaluated through accelerated life tests, but for hot carrier effects, acceleration is performed with respect to the supply voltage and the time-dependent change in characteristics fluctuation is measured.

For example, the time for Vth to fluctuate 10 mV is determined as the device life τ, and the life at the normal operating voltage is estimated from the supply voltage dependence on τ. (Fig. 2-2)

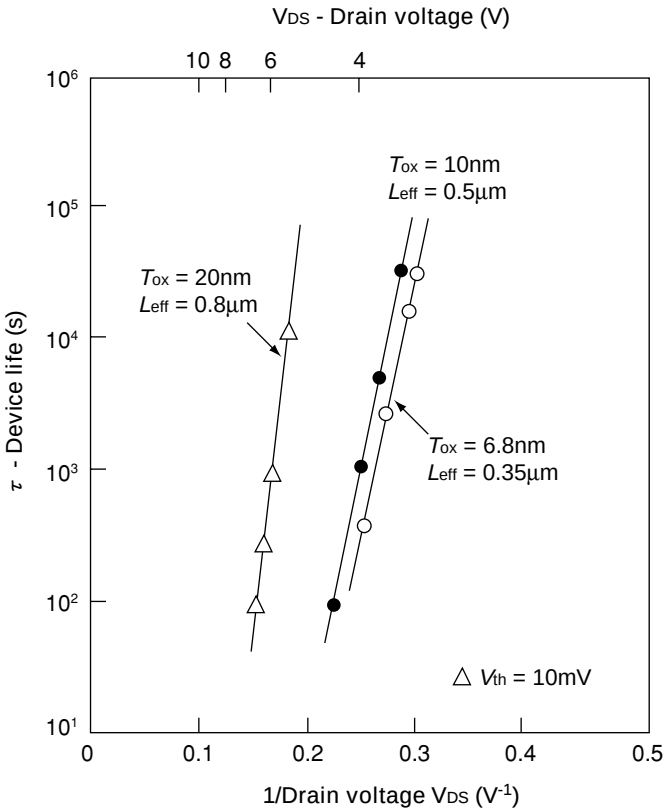


Fig. 2-2 Device Life Dependency on Drain Voltage

In addition, hot carrier effects become prominent at lower temperatures, so low temperature tests are also performed.

Hot carrier effects are effectively suppressed by moderating the electric field using a Lightly Doped Drain (LDD) structure which creates a high resistance layer near the drain. (Fig. 2-3)

However, even this has its limits, so recently further reductions in supply voltages are being promoted to prevent hot carrier effects from becoming a serious problem.

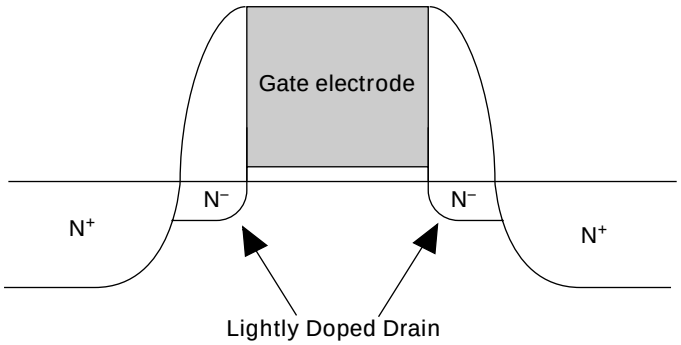


Fig. 2-3 LDD Structure

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5) E. Takeda, H. Kume, Y. Nakagome, S. Asai, "An As-P (n^+–n^-) double diffused drain MOSFET for VLSIs," *1982 Symp. on VLSI Technology, Tech. Dig*., pp.40-41 (Sep. 1982).
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2.2.2 Time-Dependent Dielectric Breakdown (TDDB)

2.2.2.1 Description

Even at normal voltages, continuously applying stress to the gate oxide film (hereafter abbreviated as "oxide film") will eventually produce insulating film breakdown. This breakdown of the insulating film over time is called time-dependent dielectric breakdown (TDDB). Differences in reliability can be clearly understood even for oxide films which show no difference at the initial withstand voltage, by accelerated TDDB evaluation using high stress.

This makes it possible to evaluate new processes and quickly detect trouble occurring in manufacturing lines.

In addition, high reliability can be assured by predicting oxide film life from accelerated TDDB data, setting optimum screening conditions, and eliminating initial defects.

2.2.2.2 Experimental Data

Time-dependent oxide film breakdown phenomena can generally be divided into an initial breakdown area when breakdown occurs sporadically and a genuine breakdown area when all samples rapidly break down after a long period of time.

Fig. 2-4 shows the TDDB evaluation results for a 4.2 nm oxide film at constant voltage.

The initial and genuine breakdown areas can be separated according to differences in the shape parameter (equivalent to the graph slope) of the Weibull distribution function.

Initial breakdown produces the serious result of failure in a short time after the device has entered the market, and the number of occurrences must therefore be reduced as much as possible.

In contrast to this, genuine breakdown indicates the life limit of the oxide film, and is an important factor in determining the product life.

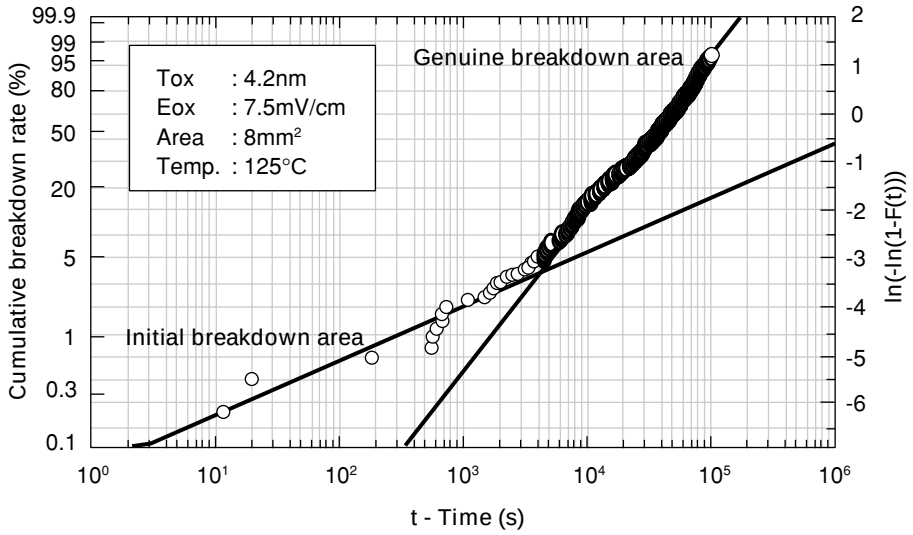


Fig. 2-4 TDDB Characteristics at Constant Voltage

<References>

1) Realize Inc., Editor K. Taniguchi, “Silicon Thermal Oxide Films and Their Boundaries”, pp.235-240 2.2.5

2.2.3 Electromigration and Stress Migration

2.2.3.1 What is Migration?

The increased integration and miniaturization of semiconductor devices has increased the current density in the metal wiring, and larger circuit scales have also increased the power consumption. This has resulted in even higher temperature rises during actual operation.

The metal wiring used in semiconductor devices has a polycrystalline structure. Photo 2-1 shows a view of this structure.

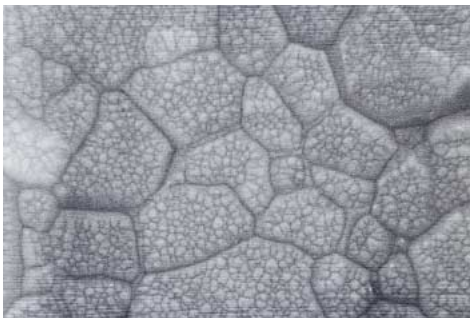


Photo 2-1 View of Polycrystalline Structure

As shown in Fig. 2-5, in a polycrystalline structure the structure (orientation) differs for each crystal grain, so many defects are scattered around the grain boundaries (the boundaries between the crystal grains) and some of the metal atoms caught in these defects have weak inter-atom bonds. Due to these structural factors, if the current density or thermal stress acts in excess of a certain allowable range, the weakly bonded metal atoms begin to migrate. This causes aluminum atom voids to form and grow, which produces the problems of increased wiring resistance and disconnection.

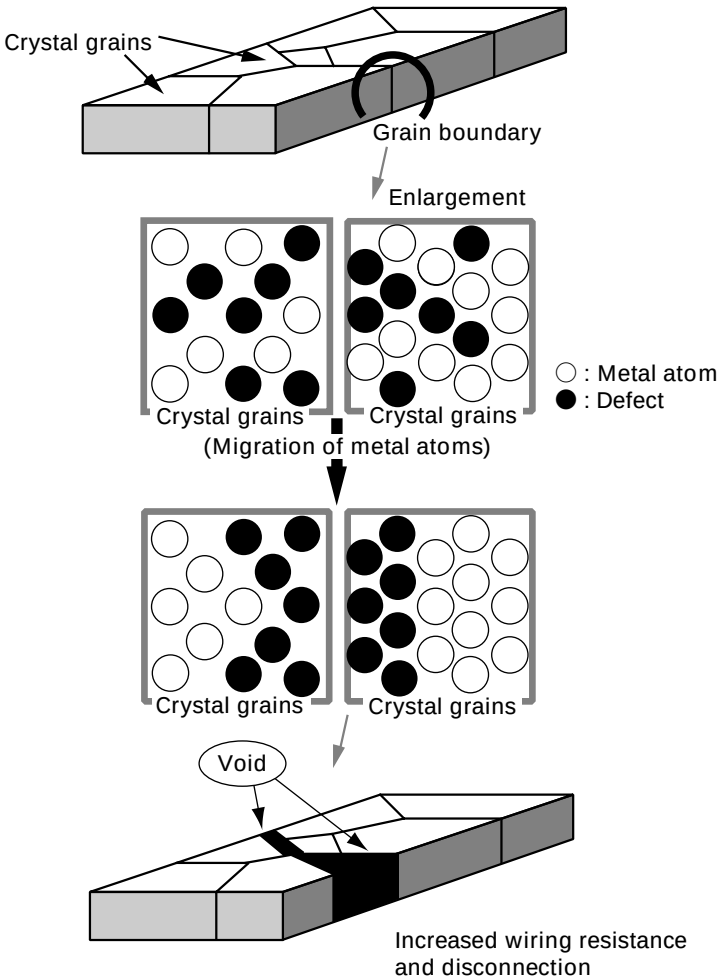


Fig. 2-5 Concept Drawing of Defect Generation by Metal Atom Migration

2.2.3.2 Electromigration

(1) Description

Electromigration is a phenomenon where the metal atoms comprising metal wiring move due to impacts with electrons.

When current of a certain current density or higher flows continuously through metal wiring under a high temperature environment, electromigration causes the metal atoms to move, resulting in disconnection and other defects.

Note that this phenomenon becomes more apparent with the passage of operating time, so it is classified as a progressive defect.

Photo 2-2 shows an example of a disconnection defect during an accelerated life test. This accelerated life test was carried out at a via hole in multi-layer wiring, and it can be confirmed that a void occurred in the lower layer wiring of the via hole, resulting in a disconnection defect.

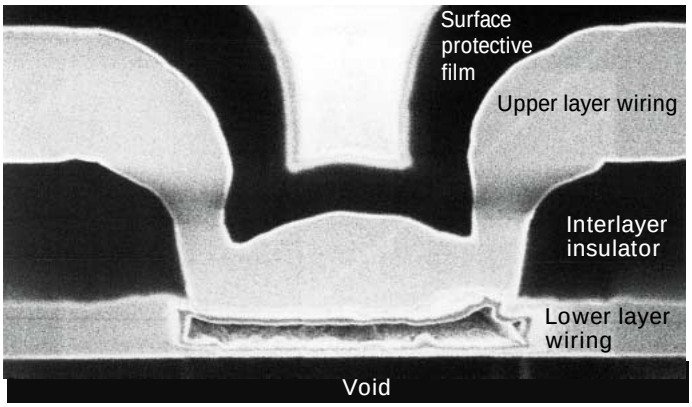


Photo 2-2 Disconnection Defect due to Electromigration

(2) Theory

When current with a current density in excess of the allowable range flows through metal wiring, metal atoms colliding with electrons acquire momentum in the direction of the electron flow. Metal atoms with this momentum then migrate in the direction of the electron flow along the crystal grain boundaries where diffusion is easy. In addition, metal atom movement becomes more active at higher temperatures, so electromigration also becomes more apparent. In this manner, current density and temperature are major factors in the occurrence of electromigration.

Electromigration is a phenomenon which appears when current flows continuously through metal wiring under certain conditions, and directly affects the wiring life.

Crystal grain boundaries exist in metal wiring, but these grain boundaries are not uniform between individual metal wiring, so there is some variance in the wiring life. Therefore, statistical techniques must be used when judging the wiring life.

Individual wiring lives obtained through accelerated life tests are statistically processed, and the median wiring life value of these is called the median life (MTF).

The median life due to electromigration is generally expressed using Black's empirical formula[1].

$$MTF = AJ^{-n}\exp\left(\frac{Ea}{kT}\right)$$

Where,

MTF : Median life [h]
A : Wiring intrinsic constant
J : Current density [A/cm^2]
n : Constant indicating the current density dependence
Ea : Activation energy [eV]
k : Boltzmann's constant (8.616×10^{-5} eV/K)
T : Absolute temperature [K]

Examples of countermeasures against electromigration are as follows.

- Improving the wiring structure
  …Using barrier metal structures or AlCu alloys and designing a wiring structure capable of assuring sufficient wiring life.
- Semiconductor device manufacturing equipment control
  …Controlling the wiring film quality and wiring cross section and maintaining wiring quality.
- Addition of a smoothing process to the semiconductor device manufacturing process and adjustment
  …Designing a manufacturing process capable of assuring a sufficient wiring cross section.
- Confirmation and adjustment of semiconductor device design rules
  …Prescribing current densities and formulating and enforcing rules based on the results of accelerated life tests.

(3) Test data

Electromigration resistance tests set a relatively high current density under high temperature environments and confirmed the wiring life.

Fig. 2-6 shows an example of accelerated life tests. These accelerated life tests were conducted at test temperatures from 150 to 200℃, and confirmed that the life was longer at lower test temperatures.

The activation energy of -0.6 eV was obtained from the Arrhenius plotted results of these median lives. (Fig. 2-7)

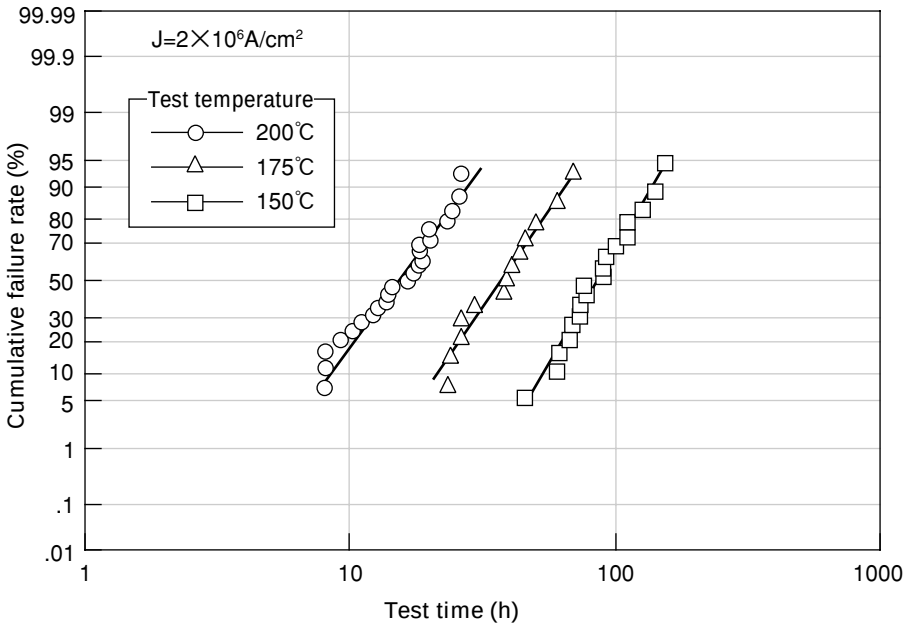


Fig. 2-6 Wiring Life in Accelerated Life Tests

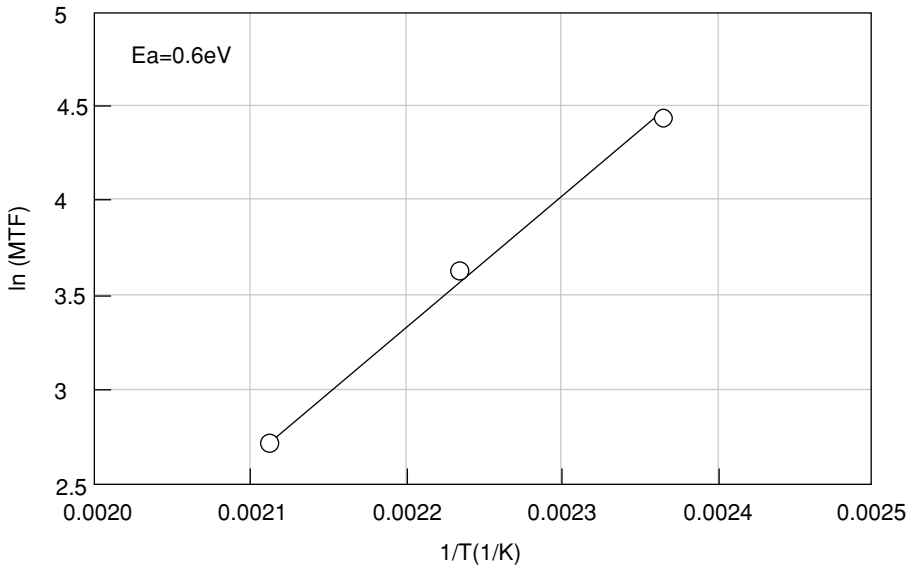


Fig. 2-7 Temperature Dependence of Electromigration Life

2.2.3.3 Stress Migration

(1) Description

Stress migration is a phenomenon where the metal atoms comprising metal wiring migrate due to stress.

In semiconductor devices, stress produced by the structure acts on the metal wiring.

When these semiconductor devices are subjected to high temperatures, differences in the thermal expansion between materials cause the stress acting on the wiring to increase even further.

When this stress exceeds a critical level, the metal atoms begin thermal diffusion through the crystal grain boundaries, and the defects scattered in each grain boundary migrate. As a result, defects converge locally in some places, causing disconnection defects and other problems in miniaturized wiring.

In this manner, stress migration is thought to be a plastic deformation phenomenon caused by stress.

Photo 2-3 shows an example of a disconnection defect during an accelerated life test of multilayer wiring. Here, a void has occurred in the 1Al wiring, resulting in a disconnection defect.

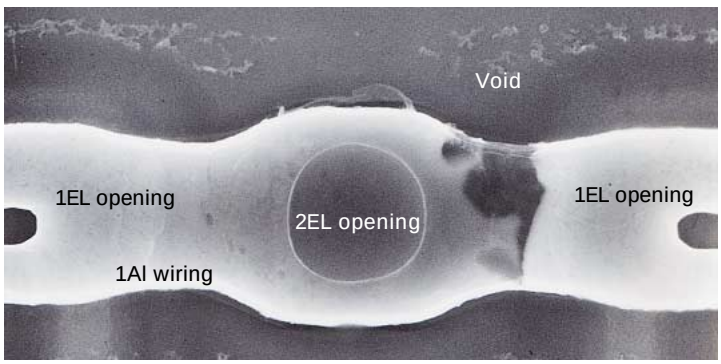


Photo 2-3 Disconnection Defect due to Stress Migration

(2) Theory

Various research is currently underway on stress migration, but its mechanism has not yet been clarified.

This section describes the basic contents of stress acting on metal wiring.

The stress acting on metal wiring is expressed as the sum of the intrinsic stress and thermal stress.

- **Intrinsic stress**

The materials and molding method used for semiconductor devices may cause distortion in the crystal lattice of the semiconductor substrate. Intrinsic stress occurs in the direction to alleviate this distortion.

- **Thermal stress**

Semiconductor devices are molded from various different materials, and the difference in coefficients of thermal expansion between these materials produces stress. This stress depends on temperature, and is expressed by the following formula.

$$\sigma_{th} = \frac{E}{(1-\nu)} \int_{T_2}^{T_1} (\alpha_1 - \alpha_2)\, dt$$

where,

σ th: Thermal stress E: Young's modulus ν : Poisson's ratio α_1, α_2: Coefficients of thermal expansion

T_1, T_2: Temperatures

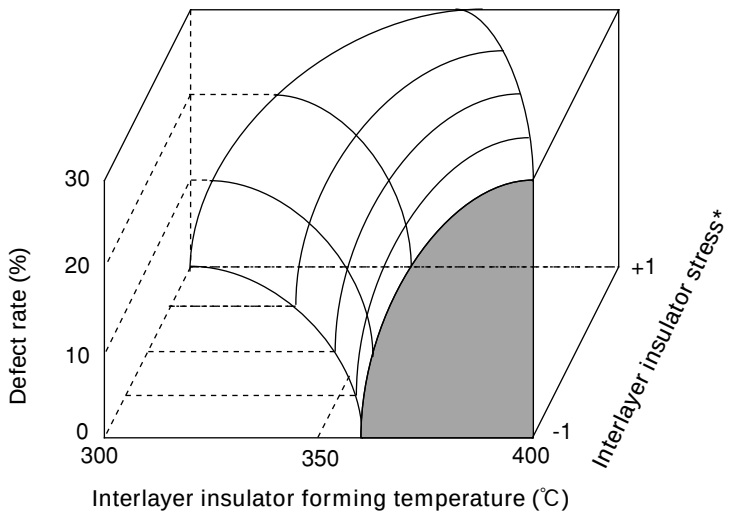
(Coefficients of thermal expansion of typical materials)

Si: 2.5, SiO_2: 0.6 to 0.9, SiN: 2.8 to 3.2, Al: 23.0 (10^{-6}/℃)

However, this stress is also affected by the semiconductor device structure, so adequate consideration must be given to each structure.

Therefore, reducing these stress factors is a countermeasure against stress migration. However, compound factors may be present, so diversified countermeasures are necessary.

Fig. 2-8 shows an example of investigation using the design of experiment method. This investigation showed that the stress migration defect rate for the insulating film on metal wiring can be reduced by adjusting both the film forming temperature and the intrinsic stress.



*Note) Interlayer insulator stress +1: Compressive, -1: Tensile

Fig. 2-8 Relationship between the Interlayer Insulator Forming Temperature and Stress

(3) Temperature dependence and the effects of device structure

The major factors affecting stress migration are as follows.

- **Temperature dependence**

Stress migration is thought to have two modes: a low temperature long-term mode where disconnection occurs after long-term storage at approximately 200℃ or in aging tests, and a high temperature short-term mode where voids occur during heat treatment in the semiconductor device manufacturing process.

The failure rate for the low temperature long-term mode has been reported to peak at 150 to 200℃.[2)] This is thought to be because while the metal atom diffusion speed increases at higher temperatures, the stress produced by the insulating film on the metal wiring and other factors becomes smaller.

In the high temperature short-term mode, stress migration is improved by reducing the temperature in the high temperature heat treatment process within the semiconductor device manufacturing process, and by adjusting the heating and cooling processes.

- **Effects of device structure**

Table 2-3 lists general cases which have been confirmed thus far.

Table 2-3 Effects of Device Structure

Structure	Life	Primary factor	
Wiring film thickness	Thick > Thin	Increased defect density	3)
Wiring width	Wide > Narrow	Increased defect effect	3)
Wiring length	Short > Long	Increased defect dependence rate	4)
Insulating film on wiring	Thin > Thick	Increased tensile stress	5)
Level differences under wiring	None > Present	Concentration of defects due to stress	6)

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2.2.4 Soft Errors

2.2.4.1 Description

Semiconductor memory defects that can be recovered by rewriting the data are called soft errors.

In addition to being caused by the power supply line and ground line noise and other factors of the system using the semiconductor memory, soft errors are also caused by α rays emitted from the trace amounts of uranium, thorium and other radioactive substances contained in the package or wiring materials.

This section describes MOS SRAM soft errors due to α rays.

2.2.4.2 Physical Mechanism

When α rays penetrate silicon, electron (e^-) and hole (e^+) pairs are generated along the α ray path as shown in Fig. 2-9. Of these, the electric field causes holes generated inside the depletion layers to migrate to the p-well region, and the electrons cluster together in the n diffusion area.

These clustered electrons cause the memory node potential to drop.

In the SRAM memory cell shown in Fig. 2-10, when the High side memory node potential falls below the driver transistor threshold value, the two inverters forming a Flip-Flop both turn off at the same time, making the Flip-Flop unstable and causing misoperation. This phenomenon is a SRAM soft error.

Generally when the word line is selected, the High side memory node potential Vh drops to Vcc - Vth. Vth here is the word transistor threshold value.

When the word line is not selected, the High side memory node is charged by the memory cell load and the potential returns to Vcc. The faster this recovery time from Vcc - Vth to Vcc, that is to say the greater the current supply capacity of the memory cell load, the more resistant the SRAM is to soft errors. Therefore, the resistance to soft errors by memory cell load type is as follows.

High resistance load < Thin Film Transistor (TFT) load < PMOS load

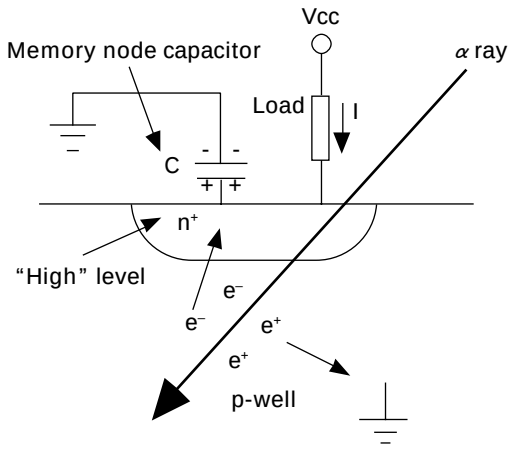

Fig. 2-9 Generation of Electron (e^-) and Hole (e^+) Pairs by α Rays

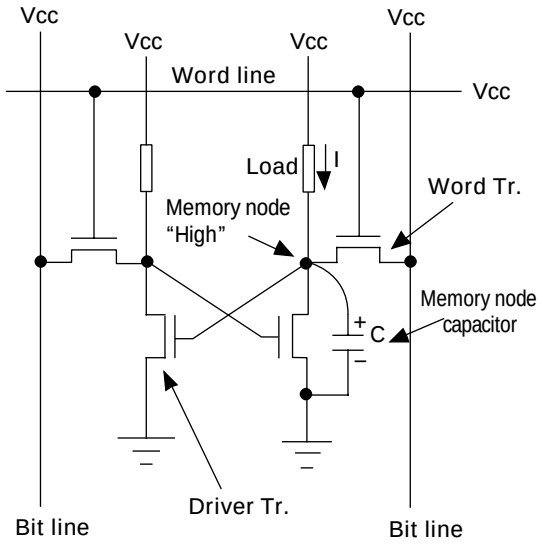

Fig. 2-10 SRAM Cell when "High" Level is written

2.2.4.3 Soft Error Evaluation Methods

There are two methods for evaluating soft errors: system tests which consist of actually operating large numbers of samples, and accelerated tests using an α ray source.

When evaluating the soft error absolute value it is necessary to conduct system tests. However, system tests require many samples and long times (for example, 1,000 samples and 1,000 hours or more).

In contrast, accelerated tests allow evaluation in a short time, but have the problem that it is difficult to accurately obtain accelerated characteristics for a market environment.

Therefore, the soft error rates for various products and conditions are obtained using a combination of system tests and accelerated tests. Soft error rates are expressed in FIT units.

$$1\text{FIT} = \frac{1\text{Failure}}{10^9\ \text{Device-hour}}$$

Fig. 2-11 and Fig. 2-12 show the results of soft error accelerated tests for Sony 8M bit SRAM.

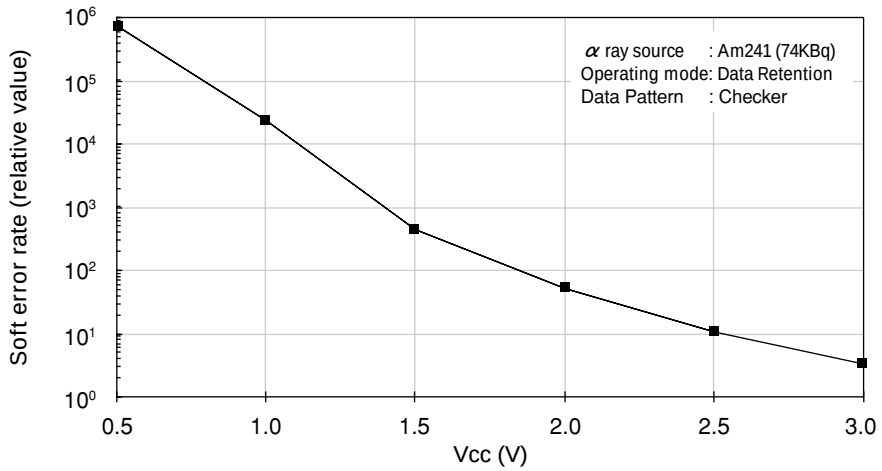

Fig. 2-11 Dependence of 8M SRAM Soft Error Rate on Supply Voltage

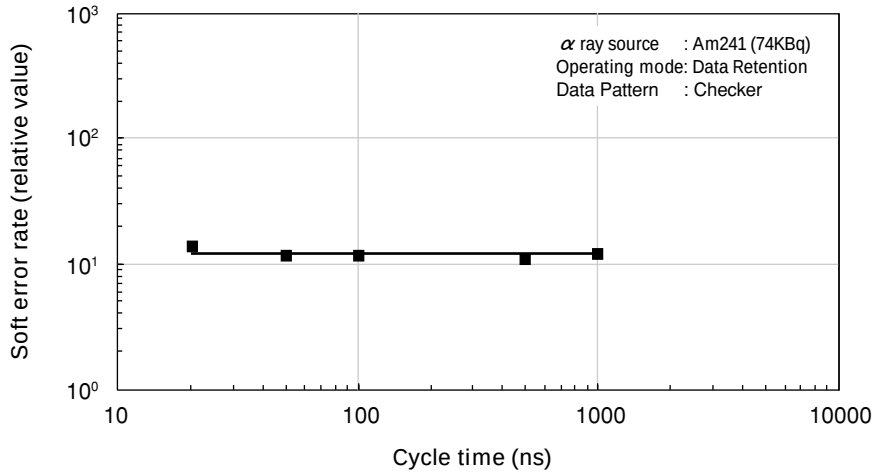

Fig. 2-12 Dependence of 8M SRAM Soft Error Rate on Cycle Time

As the supply voltage drops, the charge level accumulated in the node decreases, so soft errors occur more easily. In Sony products, the soft error rate increases by a digit when the supply voltage is 2.0 V compared to 3.0 V. (Fig. 2-11)

Sony products adopt the Pulsed-Word-Line system and the word line open period is always constant and short regardless of the cycle time, so the memory cell High side node potential is constantly maintained at approximately Vcc. For this reason, the soft error rate is constant regardless of the cycle time. (Fig. 2-12)

2.2.4.4 Soft Error Countermeasures

The following three countermeasures can be considered for improving the soft error rate.

(1) Reducing the level of α rays penetrating the chip.
(2) Making it difficult for electrons generated by α ray penetration to cluster together at the memory nodes.
(3) Increasing the memory node capacitance.

(1) can be achieved by reducing the amount of radioactive substances contained in the package and wiring materials, or by coating the chip surface to attenuate the α rays penetrating the chip.
(2) can be achieved by reducing the diffusion layer area or increasing the substrate impurity density, etc.
(3) can be achieved by reducing the insulating film thickness or adding capacitance to the memory nodes.

As the miniaturization of semiconductor devices progresses, capacitance is decreasing and supply voltages are dropping, so the situation regarding soft errors is becoming even more severe. In addition, it is now known that neutrinos generated by cosmic rays also cause soft errors.

Under these circumstances, it is necessary to implement a well-balanced combination of countermeasures (1) to (3) above.

2.2.5 Failures Rooted in the Wafer Process

2.2.5.1 Dust-induced Failure

The effect produced by dust adhering to the wafer in the wafer process differs according to the process in which the dust adheres, the position at which the dust adheres on the chip, and the dust size, shape and composition.

Wiring disconnection and shorts : Dust adhered when forming the wiring may disconnect wiring passing over the dust. In addition, if non-etched metal remains around the dust, the dust's own conductivity may cause adjacent wiring to short. (Photo 2-4) When wiring is destroyed in this manner, the wafer fails the electrical characteristics inspection and the yield drops.

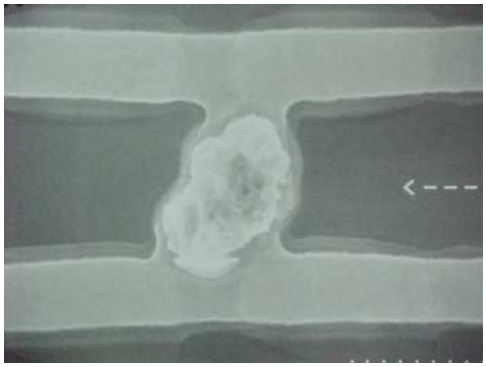

Photo 2-4 Dust-induced Wiring Short

Contamination : When dust containing metals or other elements adheres, the wafer becomes contaminated. Contamination is described in the following section, but contamination occurring before or after transistor forming in the wafer process causes electrical characteristic fluctuation, abnormal oxidation and other effects.

Dust in the wafer process is an unavoidable problem, but care should be given to the following points to maintain and improve product quality.

1. Not generating dust

Sources of dust include the wafer processing equipment, the clean room air circulation system, and dust brought into the clean room from outside, etc. Various steps must be taken to prevent the generation of dust, and dust levels must also be monitored and fluctuations dealt with.

Dust generated by equipment adheres directly to wafers, and thus has a large effect. Sufficient consideration should be given to dust when selecting equipment models, and it is also important for device manufacturers to take steps to reduce dust generation when setting process conditions or performing maintenance during production, etc.

Air flow control is important for maintaining clean room cleanliness. Down-flow is generally used in clean rooms, but the air flow is not uniform due to openings and equipment placements. The key points are not to generate turbulence and not to allow air flows to converge in areas where wafers are handled from surrounding areas. Air flows are controlled by installing partitions and adjusting the floor opening amounts, etc.

2. Not carrying in dust

Dust may be carried in by people entering and leaving clean rooms. Not only must the prescribed clean clothing be worn correctly inside clean rooms, but it is also important to have workers wash their hands and take air showers to remove any dust adhered to the clothing before entering clean rooms.

Dust may have adhered to or mixed with the wafers, resist or other materials brought in from outside. Dust control by material manufacturers is important, but device manufacturers must also sufficiently confirm the data from material manufacturers when materials are received. Also, care should be taken for handling during transport to prevent dust from packing materials or other sources from being carried in.

3. Not allowing dust to adhere

The wafer storage location and storage method is important for not allowing dust to adhere to wafers. In particular, the static electricity of wafers attracts dust to the wafers, so wafer charge removal measures are indispensable. For example, countermeasures might include installing an ionizer to remove charges.

2.2.5.2 Failure due to Contamination

Contamination of the wafer surface affects the device characteristics in various ways. MOS type devices in particular suffer severe effects such as endurance voltage deterioration or Vth fluctuation if the gate oxide film is contaminated. Table 2-4 shows different types of contaminants and their effects.

Table 2-4 Contaminants and Effects on Devices

Contaminant	Effects on devices
Heavy metals	Increased junction leaking, insulating film endurance voltage deterioration, oxidation speed fluctuation
Light metals	Insulating film endurance voltage deterioration, Vth fluctuation
III group elements	Conversion to P
V group elements	Conversion to N

Sources of contamination include wafer processing equipment, materials, the clean room atmosphere, and dust produced from operators. Countermeasures for reducing contamination must be taken for each contamination source.

Processing equipment

: The chamber inner wall and electrode materials may undergo spattering or etching and adhere to wafers. Materials which are resistant to spattering and etching or which have little effect on wafers should be used, and the process conditions which reduce the chance of spattering and etching should be selected. The work flow includes wafer washing as appropriate to eliminate contamination, but the degree of contamination effect on the wafer must be monitored to prevent the washing chemicals themselves from becoming a source of contamination.

In addition, when forming conductive films, an oxide film may form on the surface if the degree of vacuum is insufficient. Therefore, a sufficient degree of vacuum must be maintained during metal wiring spattering and polysilicon chemical vapor deposition (CVD).

Materials

: The silicon wafers, resist and various chemicals and gases contain impurities which may cause contamination. Quality control by the material manufacturers is important, but device manufacturers must also sufficiently confirm the data from material manufacturers when materials are received.

Clean room atmosphere

: Various contaminants carried by dust may adhere to and contaminate wafers. In addition to dust, the atmosphere itself may cause contamination. If phosphorous and other light metal compounds are present in the air, wafers which contact the air may be contaminated.

Wafers which are susceptible to contamination must be shelved and the degree of contamination effects monitored.

Dust produced from operators

: Dust produced from operators normally contains sodium, and sodium contamination of the gate oxide film produces severe effects on devices such as Vth fluctuation. Clean work rules must be observed to prevent contamination.

2.3 Failure Mechanisms Rooted in the Assembly Process

The three main types of failure mechanisms occurring in the semiconductor device assembly process are as follows.

1. Failure mechanisms related to the wire bonding junction reliability of metal wire (Au, etc.) connections between the semiconductor chip surface electrode (Al pad) and the package inner leads.
2. Failure mechanisms caused by Al sliding due to stress on the semiconductor chip from the package.
   When Al sliding occurs, cracks form in the chip surface passivation. Moisture, impurity ions and other matter then enters through these cracks and leads to Al corrosion and other reliability failure.
3. Failure mechanisms caused by fillers contained in the encapsulating mold resin.
   Stress produced by fillers causes passivation cracking which leads to Al corrosion or pn junction leaks, causing device operation defects.

This section describes the failure mechanisms and phenomenon related to the above wire bonding reliability, Al sliding phenomenon, and filler attack.

2.3.1 Wire Bonding Reliability (Au-Al junction reliability)

2.3.1.1 Description

In semiconductor packages, wire bonding is the most widely used method of ensuring electrical conductivity from the LSI chip electrode (pad) to the external leads.

Wire bonding is divided into a number of types by differences in the wire used (Au/Al), the system (nail head/wedge), and the energy used for the junction (thermocompression/ultrasonic wave/ultrasonic wave + thermocompression). However, Sony uses the most common method of gold-wire nail head system wire bonding using ultrasonic wave + thermocompression.

Wire bonding uses ultrasonic wave vibration energy, pressurization energy and heat energy to destroy the oxide film on the Al pad and then form an Au-Al metal junction. Therefore, the junction condition is affected by the bonding conditions and the condition of the Al pad, and defects such as initial bond failure due to insufficient junction strength sometimes occur. These defects can be prevented by optimizing the bonding conditions. In addition, even if there is no problem with initial bonding, two types of failure modes may occur in consideration of long-term reliability.

(1) Mechanical stress

When heat cycles and stress are applied to mold resin encapsulated devices, the difference in coefficients of thermal expansion of the plastic and the wires applies mechanical stress to the wires, and wire fatigue may cause disconnection. In addition, wire deformation during molding may cause wires to contact each other or the chip edges at high temperatures and create temporary short conditions.

(2) Au-Al alloy progression

In Au-Al different metal junctions, the formation of intermetallic compounds is known to cause long-term life degradation phenomena which are structurally unavoidable.

2.3.1.2 Au-Al Intermetallic Junction Forming Mechanism

Wire bonding consists of forming an Au-Al intermetallic junction at the connection between the chip Al pad and the gold-wire wiring material. It is reported that when this Au-Al system junction is stored for long periods at high temperatures, the junction contact resistance increases and the junction ultimately experiences disconnection.[1)]

Au-Al system junctions are known to form multiple intermetallic compounds as shown in Fig. 2-13. Table 2-5 gives the properties of these intermetallic compounds, Au and Al.

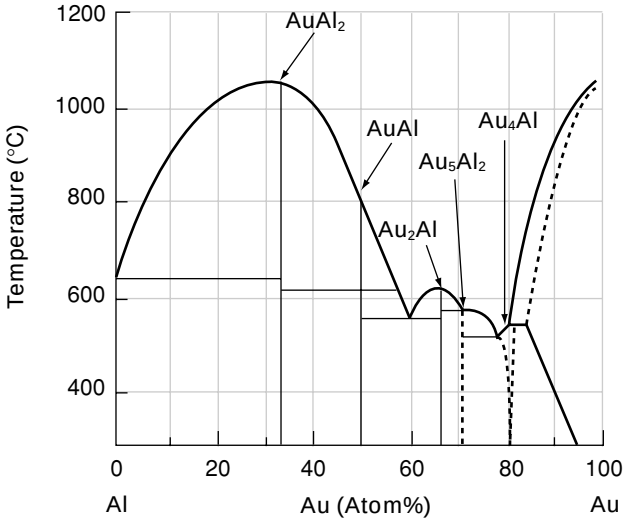

Fig. 2-13 Au-Al Phase Diagram[2)]

Table 2-5 Properties of Au-Al Intermetallic Compounds, Au and Al[3)]

Compound	Crystal structure (nm)	Unit volume (nm^3)	Number of atoms per unit volume		Volume before compound formation (nm^3)	Change in volume (%)	Compounds per unit Au	Hardness[4)] (Hv 5 kg)
			Al	Au				
Al	Face-centered cube α = 0.405	0.0664	4	0				20 to 50
$AuAl_2$	Face-centered cube α = 0.600	0.216	8	4	0.201	+7.4	3.19	263
AuAl	Face-centered cube α = 0.605	0.221	4	4	0.134	+67.9	3.29	249
Au_2Al	Structure unknown							130
Au_5Al_2	Lattice constant unknown							271
Au_4Al	Cube α = 0.6916 to 0.6923	0.331	4	16	0.338	-2.1	1.22	334
Au	Face-centered cube α = 0.408	0.0679	0	4			1	60 to 90

Degradation of Au-Al system junctions is thought to be caused by the following factors.

(a) As Au-Al diffusion proceeds, mismatching of the expansion rates between the Au_5Al_2 and Au_4Al layers among the multiple intermetallic compounds formed within the diffusion layer causes degradation of the junction strength.

(b) The difference in the diffusion coefficients of Au in Al and Al in Au causes the generation of voids around the junction (Kirkendall effect), degrading junction strength.

(c) Oxidation of the Au_4Al alloy layer using the bromine (Br) contained in the flame retardant in the mold resin as the catalyst causes formation of a high resistance layer.

The Arrhenius model is applied to degradation phenomena caused by diffusion such as that in Au-Al alloys. (See 4.3.3.)

2.3.1.3 Test Data

Photo 2-5 shows a cross sectional view of a pin bonding junction which failed an open short check after the package was shelved at 200℃ for 200 hours after plastic encapsulating. In addition, Photo 2-6 shows the failed pin junction after unsealing the plastic. These photos show that the open short failure after shelving at high temperature was caused by the formation of voids in the junction.

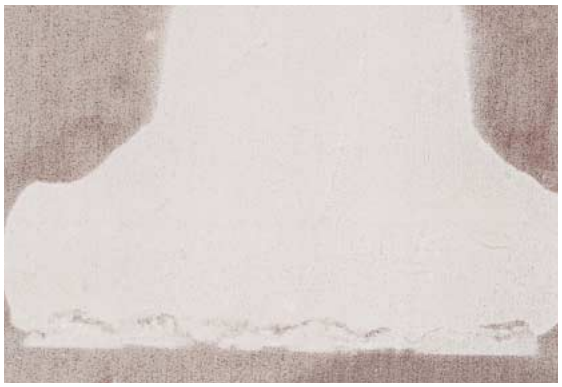

Photo 2-5 Cross Sectional View of Bonding Junction after Shelving at High Temperature

Photo 2-6 Bonding Junction

Fig. 2-14 shows the cumulative open failure rate after shelving at the high temperatures of 150℃ and 200℃ plotted on Weibull probability paper. These results show that the temperature acceleration coefficient for 200℃ is six times that for 150℃.

In addition, the Au-Al diffusion activation energy is estimated from the Arrhenius formula as Ea = 0.6 eV.

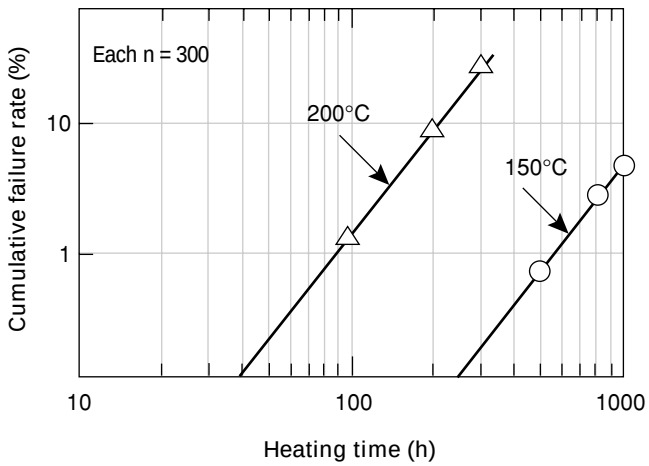

Fig. 2-14 Open Failure Rate after Shelving at High Temperature

2.3.1.4 Summary

Au-Al system wire bonding is subject to a life limit imposed by the alloy system. To improve reliability, the Sony Semiconductor Network Company optimizes the bonding conditions and selects the proper materials. Therefore, this life does not present a problem in actual use.

<References>

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2.3.2 Al Sliding

2.3.2.1 Description

Al sliding is a type of failure produced by mechanical stress on semiconductor products. Al sliding is a failure mechanism by which thermal stress produced by the difference in the coefficient of thermal expansion with the mold resin causes the Al wiring materials on the semiconductor chip to deform and slide.[1) 2)] (Photo 2-7)

When Al sliding occurs, cracks form in the passivation film which is used to protect the surface, and moisture entering through these cracks causes Al wiring corrosion which leads to wiring disconnection failures and inter-wiring leak failures.

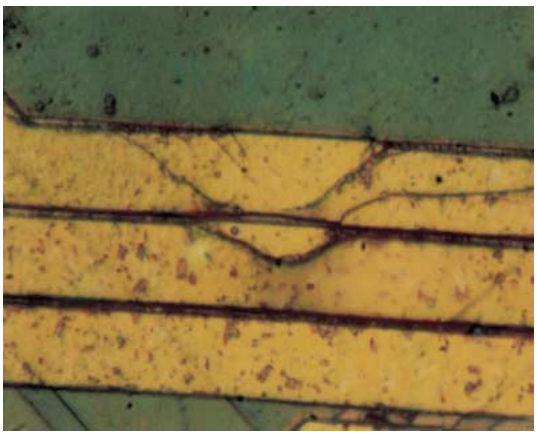

Photo 2-7 Cracking due to Al Sliding

2.3.2.2 Phenomena

Each material used in semiconductor products has its own characteristic coefficient of thermal expansion. For example, the coefficient for the substrate silicon is approximately $3\times10^{-6}/℃$, for the silicon nitride film used as the passivation film it is approximately $2\times10^{-6}/℃$, and for the mold resin it is approximately 10 to $20\times10^{-6}/℃$.[3)] Therefore, when the temperature rises the mold resin exerts outward-directed force on the chip, and when the temperature cools the opposite force is exerted on the chip. Particularly large stress is applied to the chip corners, so Al sliding is more prominent in these portions.

In addition, Al sliding occurs more easily when the mold resin has a large coefficient of thermal expansion, so mold resin with a low coefficient of thermal expansion should be used.

Furthermore, Al sliding tends to be accelerated when the stress from rapid temperature changes is also present, so countermeasures must be taken in consideration of the method in which the semiconductor device will be used.

When stress acts on a chip, stress is first applied to the passivation film on the outermost surface, and then the stress extends to the lower level Al wiring. Whereas the passivation film is resistant to plastic deformation, Al easily undergoes plastic deformation, thus causing Al sliding. When the Al deforms and the stress on the passivation film exceeds the plastic limit, cracks form in the passivation film. (Fig. 2-15) Therefore, increasing the passivation film thickness is an effective countermeasures. In addition, when the deforming Al wiring has a narrow width, the deformation amount is small and there is little chance of it developing into cracking. Therefore, inserting slits to wide Al wiring is an effective countermeasure. Applying a polyimide plastic or other buffer film between the mold resin and the chip so that stress does not act directly on the chip is also effective. In this case, the stress causes plastic deformation of the buffer film itself, thus moderating the stress propagation to the chip and preventing Al sliding.

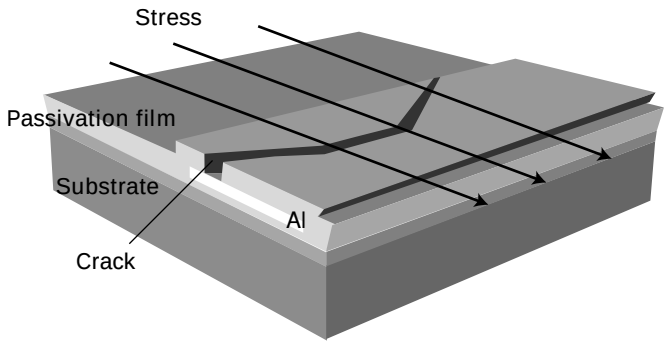

Fig. 2-15 Crack Generation Model Drawing

2.3.2.3 Summary

Al sliding is a failure mechanism by which thermal stress produced by the difference in coefficients of thermal expansion of the materials used in semiconductor products cause the Al wiring to deform and create cracks in the passivation film. The following countermeasures are effective against this type of failure.

(1) Using mold resin with a low coefficient of thermal expansion.
(2) Increasing the passivation film thickness, or coating the chip surface with polyimide plastic or other buffer film.
(3) Not locating wide wiring on the chip corners, or inserting slits to the wiring when this cannot be avoided.

<References>

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2.3.3 Filler Attack

2.3.3.1 Description

The reliability of plastic encapsulated LSI has improved significantly in recent years, and plastic encapsulated LSI are now used in almost all fields for both consumer and industrial use. However, as the degree of semiconductor integration increases, chips and packages are becoming larger and the mechanical stress received by chips is also increasing. Regarding stress-related failure, it has become known that the filler in the mold resin (encapsulating plastic) used as LSI plastic encapsulating materials is damaging the LSI chip surface and causing failures in the market and other places. In this failure mode the mold resin filler damages the chip surface, so it is called filler attack.

2.3.3.2 Phenomena

The inside of the IC package retains contraction stress produced by thermal hardening (approximately 170℃) of the mold resin. When the IC is heated by solder dipping during assembly or when the set power is turned on, the differences in the coefficients of thermal expansion of the lead frame, mold resin and the chip cause minute thermal deformation in the IC. At this time, if the filler within the plastic is contacting the IC chip surface at an acute angle, this deformation becomes a local stress concentration and presses against the chip surface. This has been found to cause cracking of the interlayer insulator on the IC chip surface and aluminum migration through these defects, resulting in electrical shorts.

Photo 2-8 shows a cross sectional view using FIB of a location where filler attack has damaged the insulating film between multilayer wiring within the chip and caused a short between the aluminum wiring resulting in an operation defect. This photo shows that the upper and lower aluminum wiring has shorted at the base of the crack.

Photo 2-9 shows the condition of mold resin which has undergone filler attack as confirmed using a scanning ion microscope (SIM). The mold resin used in this IC uses crushed filler which has the acute angle shapes seen in the photo.

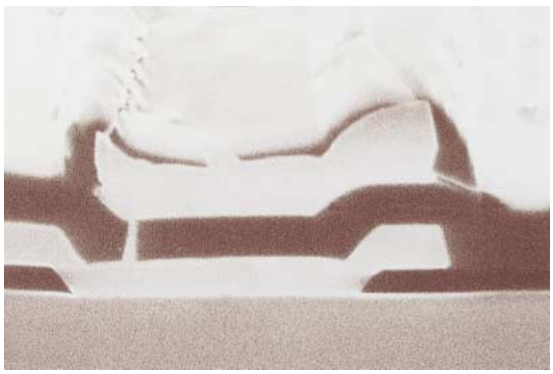


Photo 2-8 Cross Sectional View using FIB

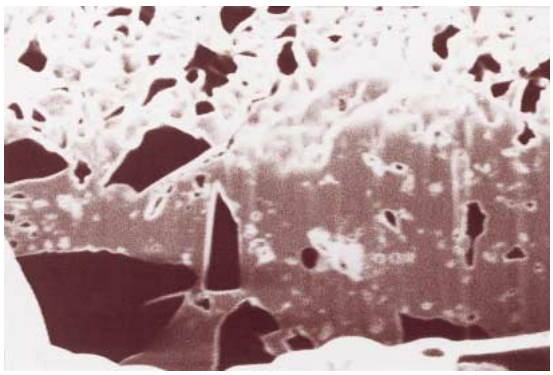


Photo 2-9 View of Mold Resin using SIM

As a countermeasure against filler attack, stress concentration can be prevented and cracking reduced by changing the mold resin used from crushed filler to spherical filler. (Fig. 2-16)

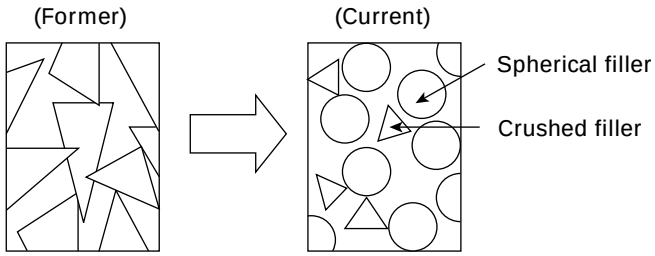


Fig. 2-16 Change in Filler Shape

Adopting these types of spherical filler materials creates no problems with reliability, and also effectively improves molding performance (spiral flow) and suppresses burring during molding.

Problems caused by local stress due to fillers include operation defects due to increased DRAM leak current, damage to the chip protective film due to local stress, and degraded moisture resistance, etc.

Methods of alleviating stress include using spherical filler, applying a special coating to the chip surface, and using low stress plastic. These measures are determined in consideration of the package shape and the IC chip process.

2.3.3.3 Summary

Selection of the filler in mold resin encapsulating materials has a great impact on semiconductor reliability. Using inorganic fillers with as little zirconium and ferric compounds which emit high levels of α rays as possible is an effective countermeasure for preventing semiconductor memory soft errors. Other countermeasures include improving the thermal conductivity, using spherical alumina powder as a filler component to increase the heat radiation performance of packages, and working to improve operation stability, life and moisture resistance.

With LSI increased integration, further advances in the development of high reliability sealing materials are predicted.

2.4 Failure Mechanisms Rooted in the Mounting Process and Occurring in the Field

2.4.1 Reliability of Surface Mount devices (SMD)

2.4.1.1 Transitions in Mounting Formats

As sets become lighter, thinner, shorter, smaller and incorporate more advanced functions, high density mounting of electronic components is becoming necessary, and semiconductor package formats are changing from through hole devices (THD) to surface mount devices (SMD). (Fig. 2-17)

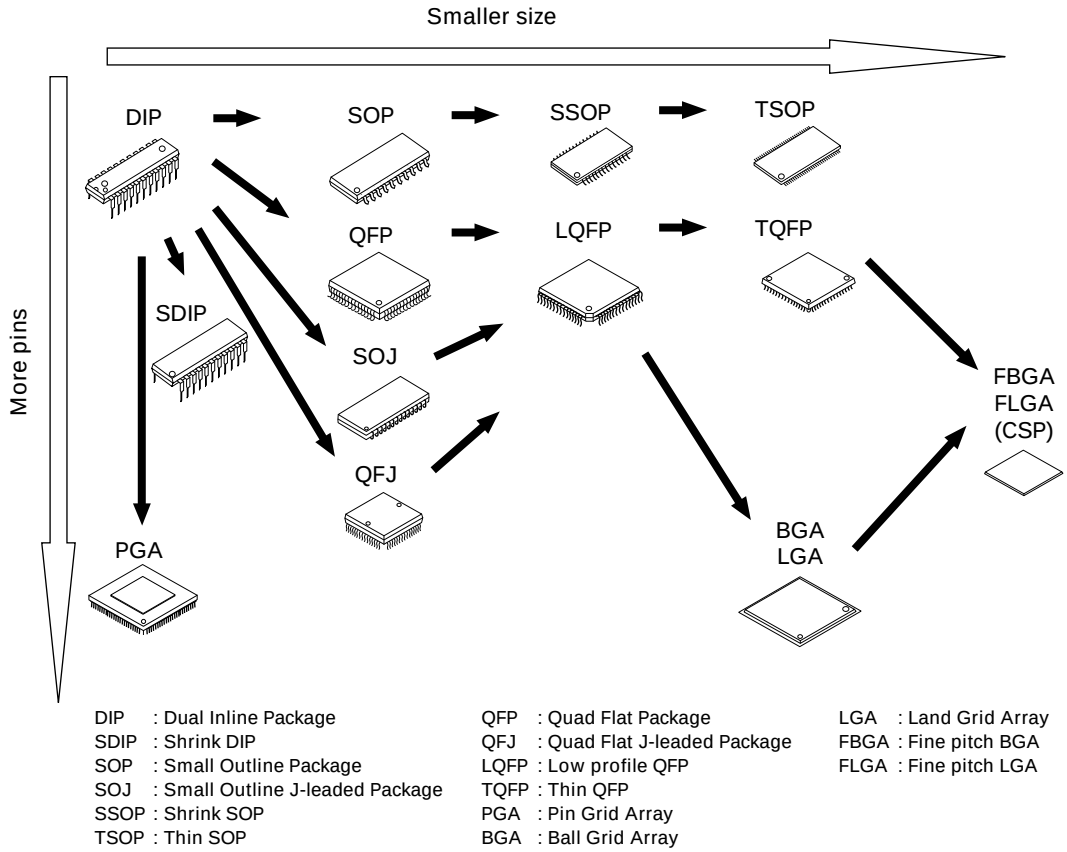


Fig. 2-17 Transitions in Semiconductor Package Types

THDs require through holes to insert the pins into the mounting substrate, causing the substrate area to increase and posing the limitation that other components cannot be mounted directly below the through holes.

In contrast to this, SMDs are mounted to the circuit portion of the substrate surface, so through holes are not necessary and the substrate area can be reduced by that amount. Furthermore, components can be mounted on both sides of substrates, making this format extremely suitable for high density mounting.

Initially, the main types of SMD were quad flat packages (QFP) and small outline packages (SOP) which had gull-wing shaped pins arranged around the package.

However, recent demands for larger numbers of pins are causing package sizes to increase, and reducing the pin pitch to meet demands for miniaturization is making mounting difficult.

Therefore, ball grid arrays (BGA) and land grid arrays (LGA) which arrange the pins in a grid pattern on the bottom surface of the package are appearing as package types which allow a wide pin pitch while suppressing increases in the package size. These types have achieved widespread use as compact, multi-pin packages.

Furthermore, recently so-called chip size/scale packages (CSP) with a package size close to the chip size are being used in video cameras and cellular phones. Various shapes have been proposed for these CSP centering on the above mentioned BGA/LGA format.

2.4.1.2 Surface Mounting Methods

(1) Surface mounting process

This section describes a typical example of reflow soldering as a surface mounting method.

Reflow soldering is a soldering method where solder paste is printed on the land of a printed substrate beforehand and then the solder is heated and melted by a reflow oven. Chip components and surface mount devices such as QFP and SOP are suitable for soldering, and large numbers of miniature components can be soldered at once with high accuracy.

The reflow soldering process is comprised of three main processes as shown in Fig. 2-18.

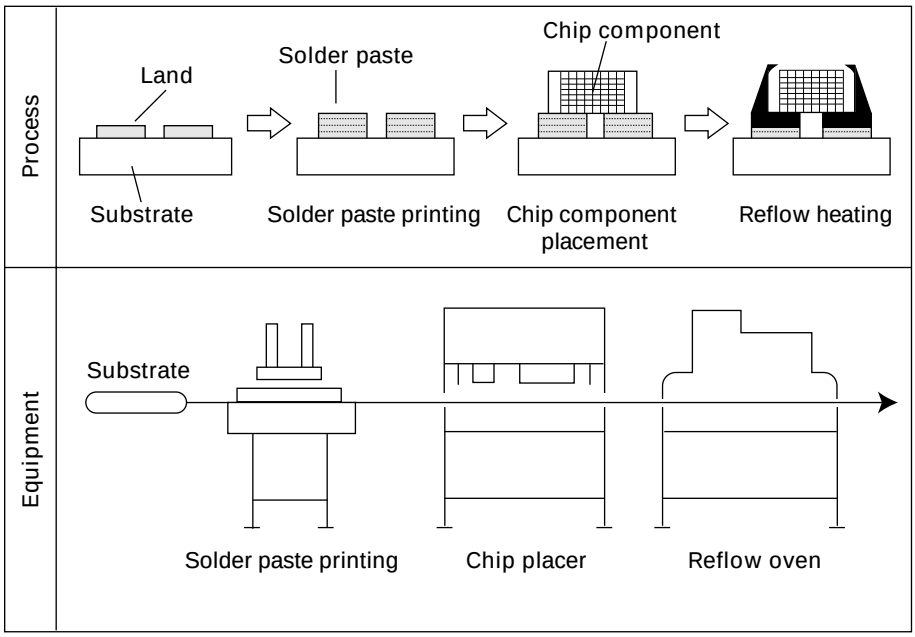


Fig. 2-18 Reflow Soldering Process and Equipment

① Solder paste printing process
The required amount of solder paste is supplied to the land of a printed substrate using a solder paste printer.

② Component mounting process
The component electrodes are mounted onto the solder paste using a chip placer.

③ Reflow process

The solder paste is melted using a reflow oven and soldering is completed.

This reflow soldering process has three key points as follows, and excellent soldering quality can be maintained when all three of these points are satisfied at the same time.

① The proper amount of solder paste is printed in the proper position.

② Components are mounted in the proper position.

③ The solder paste is heated with the proper temperature profile.

(2) Soldering methods

Soldering methods for surface mounting can be broadly classified into two types according to the method of supplying heat. Each type has the following characteristics, and should be selected according to the purpose and application.

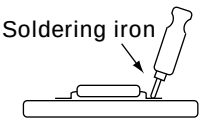
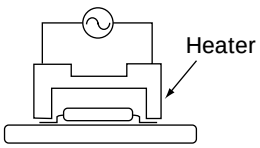
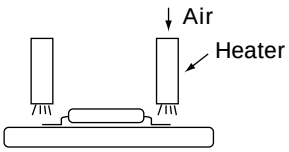
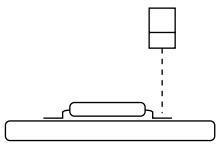
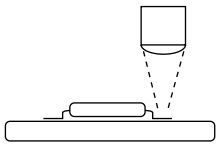
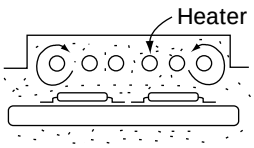
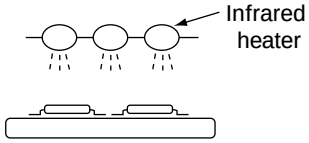
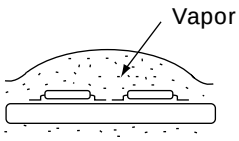
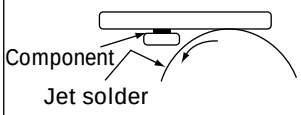
- Partial heating methods : These methods heat only the soldered portion (lead portion). There is little effect of heat to the component body or the substrate, but these methods are not suited for mass production.
- Complete heating methods : These methods heat the entire substrate and component. Multiple components can be processed at once, making these methods highly suited for mass production, but the component body and the substrate are subjected to thermal stress.

Table 2-6 shows the soldering methods and characteristics for surface mounting.

<References>

1) Mounting Technology for Surface Mounted LSI Packages and Improving Mounting Reliability
Applied Technology Publishing, Semiconductor Division Edition, Hitachi Ltd.

Table 2-6 Soldering Methods and Characteristics[1)]

	Soldering method	Work drawing	Characteristics
Partial heating methods	Soldering iron		• Simple tools • Worker skill and experience required • Proper temperature control difficult • Significant quality variance
	Pulse heater		• Little effect of heat on components • Relatively cheap equipment • Heater must be exchanged for each component dimension • Lead pressurization required
	Hot air		• Little effect of heat on components • Relatively cheap equipment • Heater must be exchanged for each component dimension
	Laser		• Little effect of heat on components • Heating of minute areas possible • Expensive equipment • Rapid heating • Shallow focus depth
	Optical beam		• Little effect of heat on components • Relatively cheap equipment • Wide focus
Complete heating methods	Hot air reflow (Air reflow)		• Cheap running cost • Little temperature difference between components and substrate
	Infrared reflow		• Relatively cheap equipment • Infrared absorption rate differs according to the component surface conditions causing temperature unevenness • Heater temperature must be set according to the printed substrate
	Vapor phase soldering (Reflow)		• Even temperature with no overheating • Expensive equipment • Expensive heat medium • High running cost
	Flow soldering		• THD components can be soldered at the same time • Significant effect of heat to components

2.4.1.3 Package Mold Resin Cracking

Package cracking caused by moisture absorption in the mounting environment or thermal stress during mounting is a problem for surface mount plastic packages.

Photo 2-10 shows an example of package cracking.

In this example, package cracking caused gold wire disconnection and a solder defect due to mold resin swelling.

Package cracking is described in detail in section 5.1.

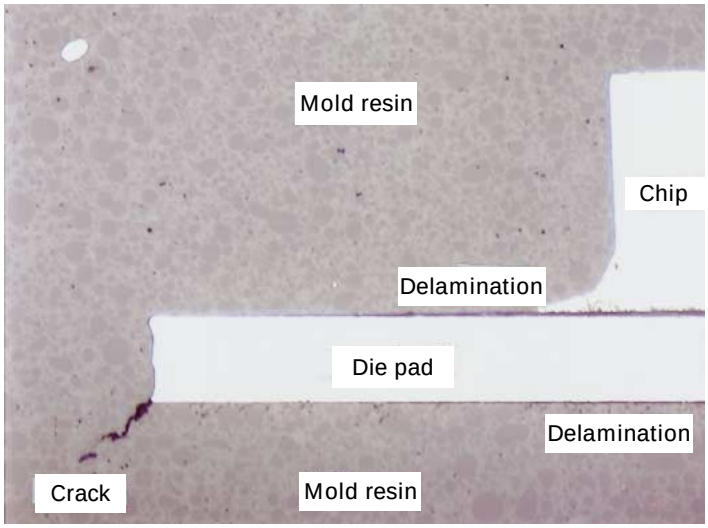


Photo 2-10 Package Cracking

2.4.2 Failure Modes Occurring in the Field

2.4.2.1 Description

Semiconductor device packages include conventional mold resin encapsulated packages and packages with new structures using substrate and tape materials. With improvements to the mold resin and lead frame, conventional packages can be said to have currently reached a reliability level where there are virtually no problems in the field. On the other hand, packages classified as new structures are being evaluated individually through accelerated tests to predict reliability and evaluation standards are being set.

This section focuses on the moisture resistance of conventional mold resin encapsulated packages and new structure packages using tape materials, and describes these failure mechanisms, accelerated characteristics and evaluation methods, etc.

2.4.2.2 Aluminum Corrosion

Aluminum corrosion is thought to be caused by the penetration of moisture and impurities from the outside. Penetration routes for conventional mold resin encapsulated packages are thought to be penetration through the boundary between the lead frame and the mold resin and penetration through the mold resin. For new structure packages using substrate and tape materials, in addition to the penetration route through the resin, penetration through the boundary between the resin and the substrate (tape materials) and penetration from the substrate (tape materials) side can also be considered. (Fig. 2-19)

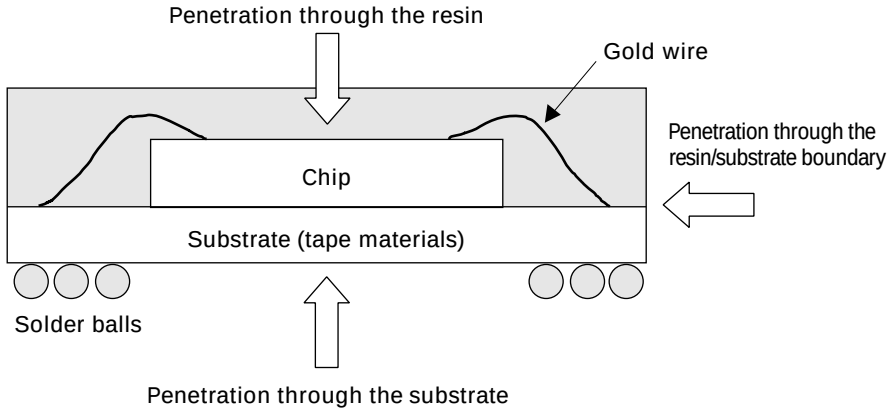


Fig. 2-19 Water Penetration Routes for Devices Using Substrates (Tape Materials)

Aluminum is an active metal even in consideration of ionization tendencies, and forms aluminum oxide (Al_2O_3) when left exposed to air. If there is sufficient water present, $Al(OH)_3$, which is amphoteric and can dissolve in either acid or alkaline solutions, is also easily formed. Example reaction formulas for aluminum corrosion due to penetration of moisture or impurities are shown below[1)], and aluminum corrosion conditions are shown in Photo 2-11.

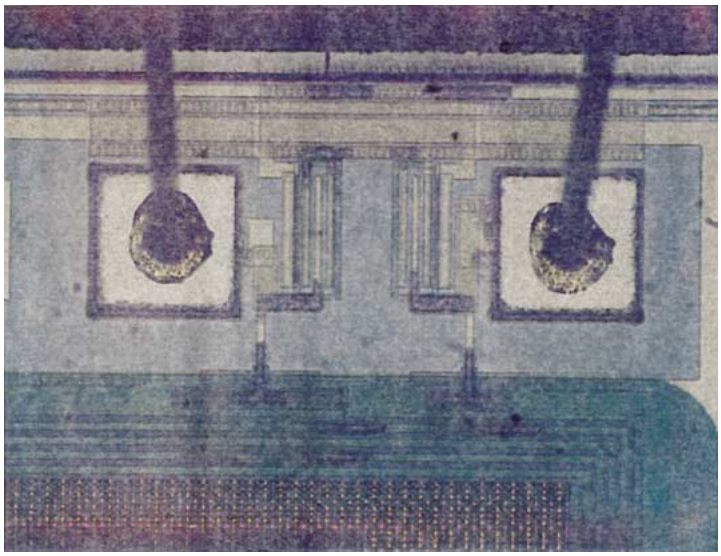


Photo 2-11 Aluminum Corrosion

Anode side

$$Al + 4Cl^- \rightarrow AlCl_4^- + 3e^-$$
$$AlCl_4^- + 3H_2O \rightarrow Al(OH)_3 + 3H^+ + 4Cl^-$$

Cathode side

$$O_2 + 2H_2O + 4e^- \rightarrow 4(OH)^-$$
$$Al + 3(OH)^- \rightarrow Al(OH)_3 + 3e^-$$
$$2Al^{3+} + 6H_2O \rightarrow 2Al(OH)_3 + 6H^+$$

2.4.2.3 Acceleration

The following acceleration models are generally given for conventional mold resin encapsulated type devices.

(1) Vapor pressure model

The time τ until a certain cumulative failure probability is reached is related to the vapor pressure P_{H_2O}.[2) 3) 4)]

$\tau \propto P_{H_2O}^{-n}$ (n is a constant)

(2) Reich-Hakim Model[5)]

The life τ is expressed by the function of the ambient temperature Ta (℃) and the relative humidity RH (%).

$$\tau \propto \exp\{-A(Ta+RH)\} \quad \text{(A is a constant)}$$

Acceleration cannot be unconditionally modeled due to differences produced by the resin and substrate (tape) materials comprising the package and the package structure. Fig. 2-20 shows the results of accelerated evaluation for Sony Semiconductor Network Company packages using tape materials. This accelerated life model used the steam pressure model, and the failure mechanism was pad aluminum corrosion.

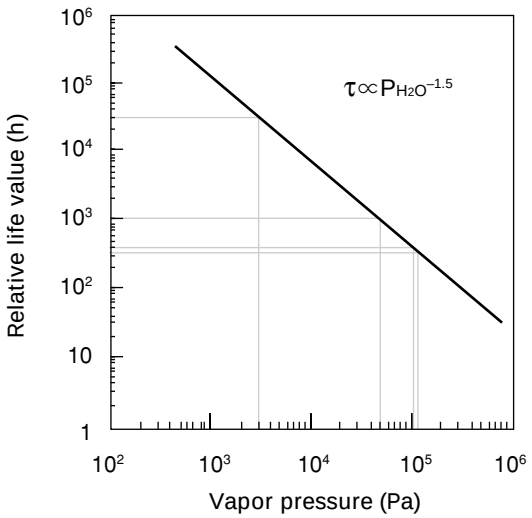


Fig. 2-20 Accelerated Evaluation Results

Of the failure mechanisms occurring in the field, this section described aluminum corrosion which is a typical failure mechanism for humidity. Focusing on this aluminum corrosion failure and assuming a market environment of 30℃ and 70% RH, the Fig. 2-20 graph results show that storage test times of 1000 h are required at 85℃, 85% RH, and 360 h at 110℃, 85% RH. (See Appendix 3.)

<References>

1) T. Ajiki, Editor, "Semiconductor Device Reliability Technology", JUSE Press, Ltd., pp.222-224 (1988).

2) F.N.Sinnadurai: "The Accelerated Aging of Plastic Encapsulated Semiconductor Devices in Environment Containing A High Vapor Pressure of Water", Microelectronics and Reliability, vol.13, pp.23 (1974).

3) N.Lincoudes: “Plastic Uses of Accelerated Testing”, The 13th Annual Proc. of International Reliability Physics Symp., pp.257 (1975).
4) J.L.Flood: “Reliability Aspects of Plastic Encapsulated Circuits”, The 10th Annual Proc. of International Reliability Phisics Symp., pp.95 (1972).
5) D.S.Peck and C.H.Zierdt: “Temperature-Humidity Acceleration of Metal-Electrolysis in Semiconductor Devices”, The 11th Annual Proc. of International Reliability Physics Symp., pp.146 (1973).

2.4.3 Solder Degradation Failure Mechanisms and Estimation of Life

2.4.3.1 Description

Even if components are soldered without problem and an initial junction is achieved, the electrical and mechanical junction or the insulation characteristics between conductors may deteriorate thereafter over time. Typical mechanisms include thermal fatigue failure, creep failure, and insulation defects caused by migration, etc. Of these, thermal fatigue failure of the soldered portion is described below.

2.4.3.2 Solder Degradation Phenomenon

Solder degradation due to thermal fatigue is a phenomenon where strain produced by the factors listed below acts repeatedly on the solder, causing cracks in the soldered portion. These cracks then progress until they pass entirely through the soldered portion, causing a conductivity defect.

- Differences in the coefficients of thermal expansion of constituent materials (components, solder, substrate, etc.)
- Electronic circuit heating and cooling due to ambient temperature changes and power-on/off

Specifically, cracks generally form as shown in Fig. 2-21.

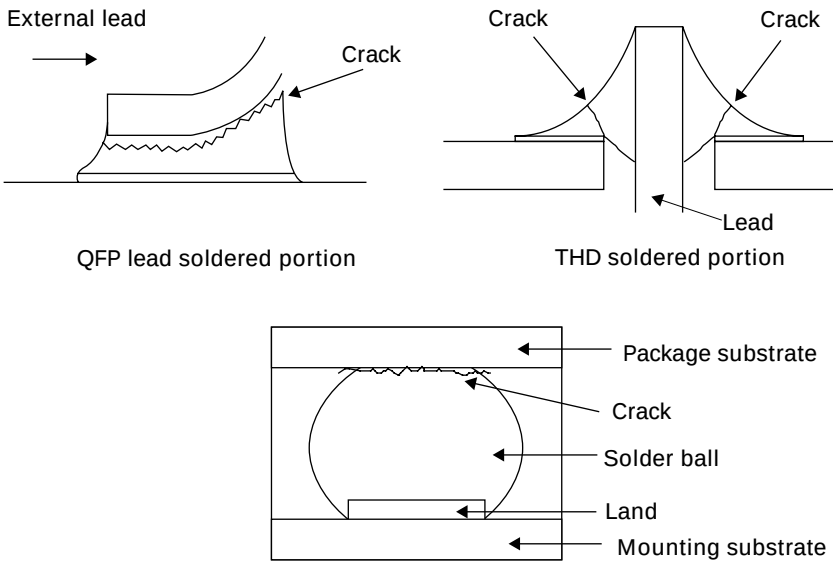


Fig. 2-21 Soldered Portion Failure due to Cracking

With trends toward high density mounting, junctions are becoming miniaturized, and operating environment conditions are becoming more diverse. Under these circumstances, thermal fatigue failure can be positioned as the most common of all solder junction failure modes.

2.4.3.3 Temperature Cycle Test Results

The phenomenon of solder degradation due to thermal fatigue is generally evaluated by mounting a semiconductor package on a test substrate and then subjecting it to a temperature cycle test. Normally, accelerated tests are conducted which subject the product to a harsher temperature and number of cycles than in the field in order to predict the product life in a short time and also to identify and analyze failure locations to aid in product improvement.

Fig. 2-22 shows an example of actual temperature cycle test data.

These results show that double-sided mounting has a lower failure life than single-sided mounting.

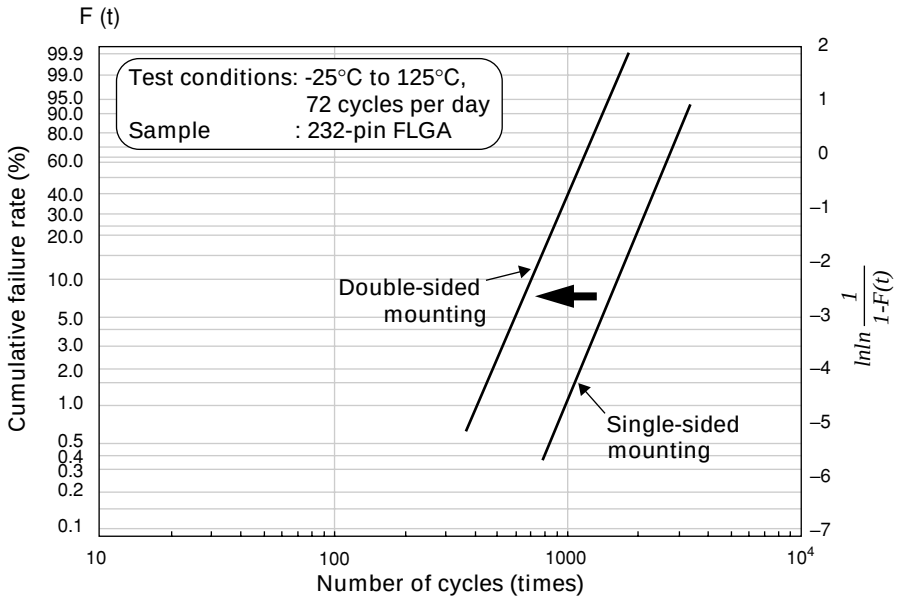


Fig. 2-22 Temperature Cycle Test Results

2.4.3.4 Estimation of Life

The thermal fatigue life Nf of soldered portions is generally known to depend strongly on the thermal fatigue strain amplitude $\Delta\varepsilon$, the repeat frequency f, the maximum temperature T_{max}, and other factors. A modeling formula which takes these factors into account (a revised Coffin-Manson model)[1) 2)] has been proposed as follows.

$$N_f \propto f^m(\Delta\varepsilon)^{-n}\exp\left(\frac{Ea}{kT_{max}}\right) = f^m(\Delta T)^{-n}\exp\left(\frac{Ea}{kT_{max}}\right)$$

where,

Ea : Activation energy k: Boltzmann's constant ΔT: Temperature difference m, n: Constants

From the above, the acceleration factor K of the temperature cycle test with respect to the field environment is expressed by the following formula.

$$K = \left(\frac{f_f}{f_t}\right)^m\left(\frac{\Delta T_f}{\Delta T_t}\right)^{-n}\exp\left\{\frac{Ea}{k}\left(\frac{1}{T_{max\,f}}-\frac{1}{T_{max\,t}}\right)\right\}$$

where,

f_f, f_t: Repeat frequency in the field and the test

ΔT_f, ΔT_t: Temperature width in the field and the test

$T_{max\,f}$, $T_{max\,t}$: Maximum temperature in the field and the test

m: 1/3 (general value used in solder thermal fatigue models)

n: 1.9 to 2.0 (general value used in solder thermal fatigue models)

The life of soldered portions in the field can be estimated by substituting the temperature cycle test results into the above formula.

2.4.3.5 Summary

This section discussed thermal fatigue destruction as a typical solder degradation mode. However, creep failure and insulation defects caused by migration must also be taken into account as time-dependent solder degradation as mentioned above.

In addition, overall reliability must be investigated further with regards to the introduction of lead-free solder in response to environmental problems.

<References>

1) Sato et al., Bulletin of the Japan Institute of Metals, Vol. 23, pp.1004 (1984).

2) K. C. Norris et. al, IBM J. Research and Development, 13, pp.266 (1969).

2.4.4 Reliability of S-Pd PPF

2.4.4.1 Description

The Sony Semiconductor Network Company has set forth policies to reduce or eliminate usage of various hazardous substances from the standpoint of protecting the global environment.

The external leads of semiconductors are plated with solder containing lead as a surface treatment, and environmental pollution caused by the elution of this lead by acid rain when semiconductors are disposed as industrial waste is becoming a problem.

The Sony Semiconductor Network Company is working to develop various technologies to create products in consideration of the environment, and the Sony specification palladium Pre-Plated lead Frame (S-Pd PPF) introduced here is one of these products.

Products using S-Pd PPF have eliminated plating which contains lead from the external leads to realize lead-free products which could be said to take into account protection of the global environment.

The mounting reliability of these products also fully satisfies the requirements for both conventional lead solder and for lead-free solder.

2.4.4.2 Assembly Performance and Reliability

(1) Assembly performance (S-Pd PFF have the same assembly performance as conventional partially silver-plated lead frames.)

- Die bonding performance

  The Sony Semiconductor Network Company has developed original plating technology and is working to increase the bonding strength between the lead frame and the chip.

- Wire bonding performance

  The Sony Semiconductor Network Company has developed original Pd PPF wire bonding technology and is performing wire bonding at the same reliability as conventional technology.

(2) Reliability

- Resistance to corrosion

  In addition to potentially noble palladium, the outermost surface of the S-Pd PPF used by the Sony Semiconductor Network Company is also coated with gold, so the resistance to corrosion for normal base coat plating is worse than for conventional solder plating. Therefore, we have developed original plating technology which ensures the same resistance to corrosion as conventional products.

- Resistance to package cracking

  S-Pd PPF exhibit excellent performance compared to copper alloy materials.

  The Sony Semiconductor Network Company also sufficiently tests and evaluates the mold resin to ensure the same plastic adhesiveness for S-Pd PPF as for conventional products. In addition, moisture absorption control ensures a resistance to package cracking which is top level in the industry.

- Solderability

  The Sony Semiconductor Network Company's S-Pd PPF plating structure uses gold plating on the outermost surface layer to prevent surface oxidization of the palladium and adsorption of organic substances. Furthermore, the fast diffusion speed of the gold and palladium inside the solder is used to improve the solder wetting speed.

  Accelerated tests are also conducted to confirm that the S-Pd PPF solderability does not deteriorate.

(3) Mounting reliability

- External shape during mounting

  S-Pd PPF are not subject to the excessive solder wicking phenomenon which occurred with conventional solder-plated products.

  The Sony Semiconductor Network Company's S-Pd PPF exhibit excellent solder wetting performance, and form the ideal fillet (junction shape). (See Photos 2-12 and 2-13.)

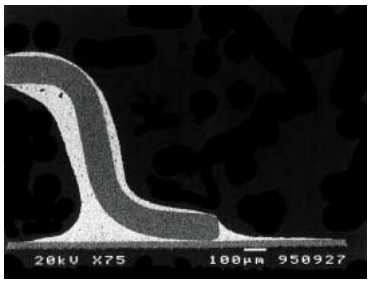


Photo 2-12 Conventional Solder Plated Product

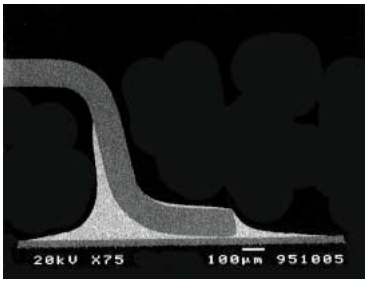


Photo 2-13 S-Pd PPF Product

- Junction mechanism

The S-Pd PPF solderability mechanism is as follows. The outermost gold plating layer and the middle palladium plating layer suppress oxidation of the nickel plating layer in the assembly process, etc. In addition, the gold and palladium diffuse into the solder bulk during soldering, so the solder contacts a fresh nickel boundary and forms a Ni_3Sn_4 intermetallic compound. (Fig. 2-23)

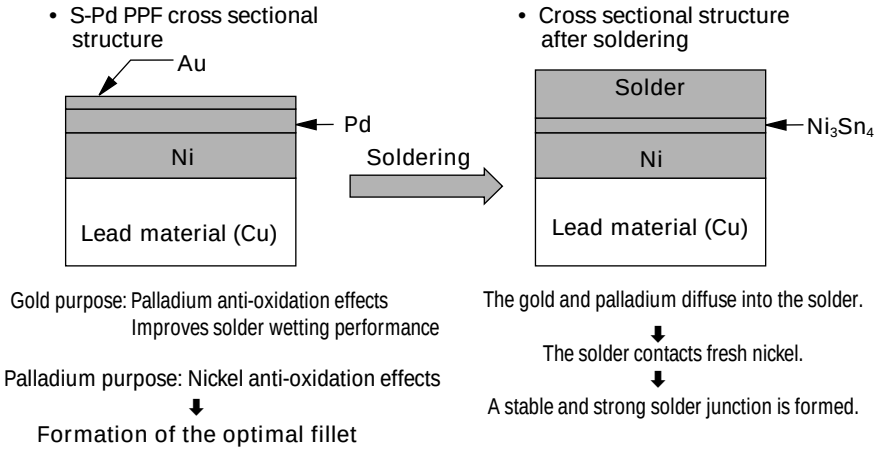


Fig. 2-23 Soldering Mechanism

In addition, gold and palladium are not present at the junction boundary, so these intermetallic compounds are not formed and the junction reliability does not drop. (Fig. 2-24, Photo 2-14)

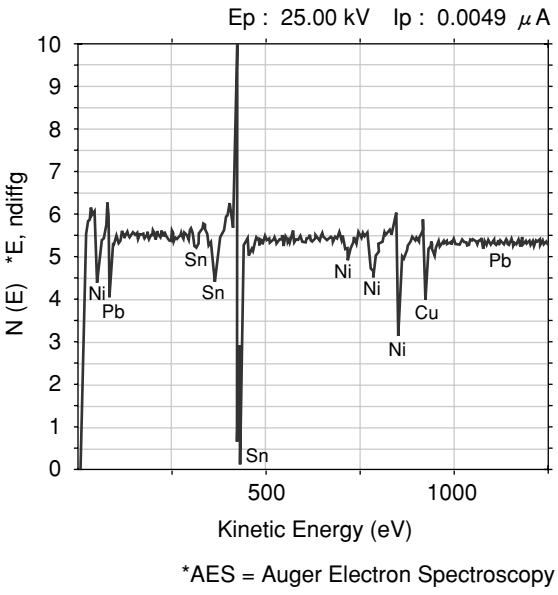


Fig. 2-24 Junction Boundary (Sn/Ni) AES Spectrum

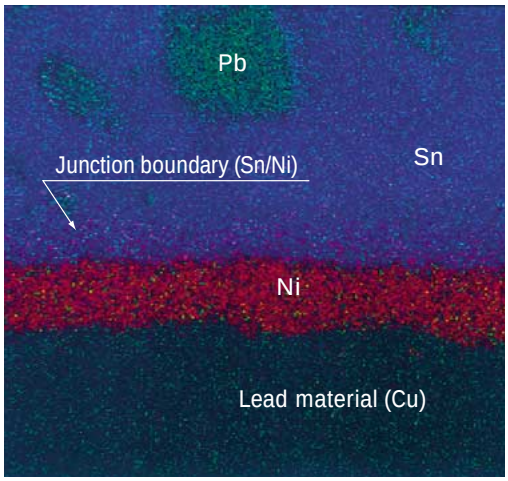


Photo 2-14 AES* Surface Analysis results

• Mounting junction strength

The initial junction strength after S-Pd PPF mounting is not only the same level as that for conventional solder-plated products, but the S-Pd PPF strength drops less than conventional solder-plated products in thermal fatigue resistance tests, thus confirming that S-Pd PPF have superior thermal fatigue resistance. (Fig. 2-25, Photo 2-15)

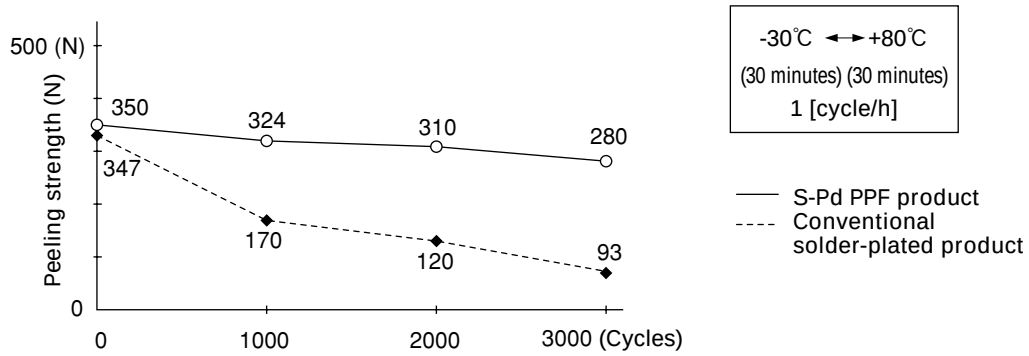


Fig. 2-25 Time-dependent Changes in Solder Junction Strength in the Temperature Cycle Test

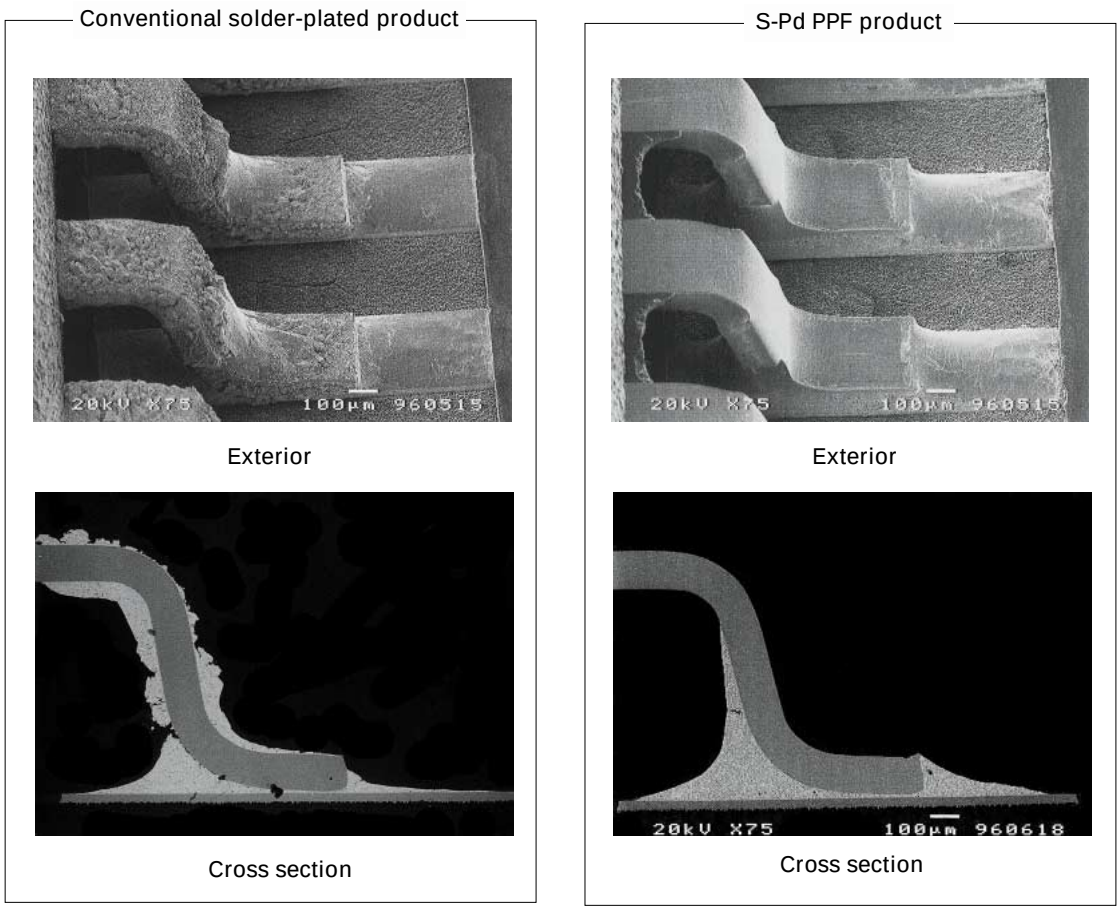


Photo 2-15 Exterior and Cross section after 3000 Cycles in the Temperature Cycle Test

2.4.4.3 Precautions

Fillet formation differs from normal solder-plated products, so care must be taken for the amount of solder paste during mounting according to the mounting conditions. In addition, adjustment may also be necessary during image recognition checks after mounting.

2.4.5 Bump Reliability

2.4.5.1 Description

The importance of Flip-Chip mounting technology is increasing further as LSI devices become faster and more highly integrated and sets become smaller and lighter weight. The Sony Semiconductor Network Company has developed and applied bump forming technology and Flip-Chip mounting technology to mass production since 1994, and employs chip size/scale packages (CSP) called transformed grid arrays (TGA) in Sony passport-size digital camcorders. Fig. 2-26 shows the solder bump structure.

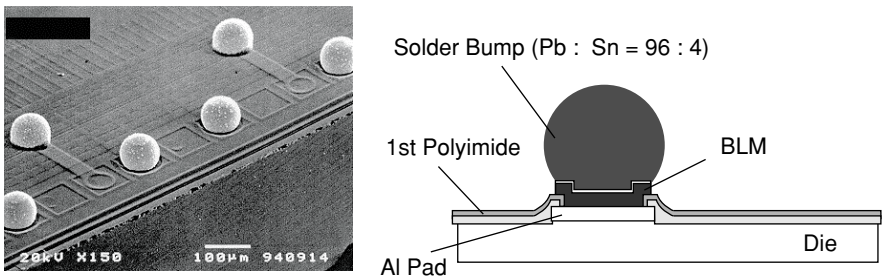


Fig. 2-26 Solder Bump Structure

Bump forming technology for Flip-Chip mount chips includes various types of bump forming methods. Typical types are solder bumps and gold stud bumps.

What these bumps all have in common is that the junction between the bump and the base coat metal film is achieved by the formation of intermetallic compounds. The junction condition is the most important factor affecting bump reliability, and a key point is how to best form a stable alloy layer with a strong junction strength. Reliability is discussed below with the solder bumps used by the Sony Semiconductor Network Company as examples. Fig. 2-27 shows the main failure mechanisms anticipated for bump junctions.

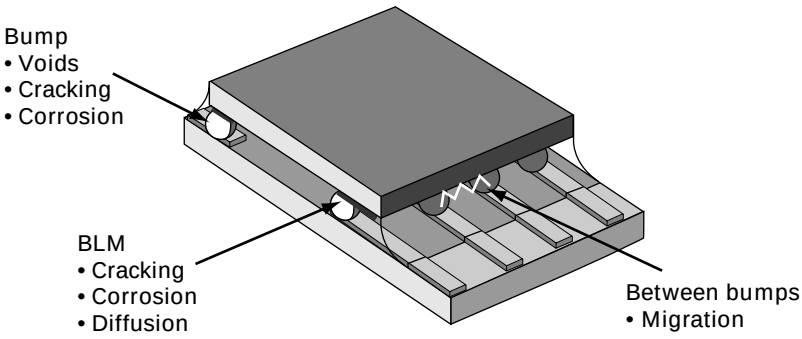


Fig. 2-27 Bump Junction Failure Mechanisms

For solder bumps, the quality of the ball limiting metal (BLM) film, the condition of the crystals constituting the solder bump, voids produced during bump forming, and other factors also affect the junction strength, so evaluation must take these factors into account. In addition, solder bumps are generally Flip-Chip mounted onto mounting substrates or other boards and the junction strength is reinforced by encapsulating the gaps with plastic to disperse and absorb the stress acting on the solder bump. When evaluating solder bump reliability, the effects of the mounting conditions (flux residue, washing damage, etc.) and the encapsulating plastic must also be taken into account.

General items for evaluating factors which affect solder bump reliability are as follows.

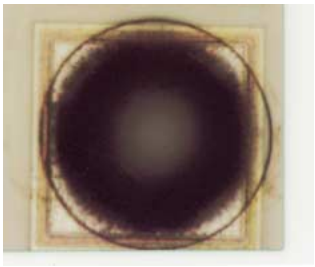
- **Bump shear and bump pull tests**
  The bump junction strength and peeling break surface are evaluated to confirm the junction condition and the initial quality such as the presence of voids.
- **Temperature cycle life test**
  Thermal fatigue of the solder bump junction due to the generation of heat during operation, mounting substrate warpage caused by this heat, or other stress is evaluated through accelerated tests and the life is predicted.
- **High temperature operation and storage tests**
  Connection resistance value fluctuation, etc. produced by changes in the intermetallic compounds formed at the solder junction due to the generation of heat during operation or other stress is evaluated through accelerated tests and the life is predicted.
- **Moisture resistance tests (PCT test, high temperature and humidity bias test)**
  In the field, solder bump junctions experience fluctuations in the inter-bump insulation resistance value and connection resistance value, and changes in the bump junction strength due to swelling of the encapsulating plastic and hydrolysis. These effects are evaluated through accelerated tests by storing at high temperatures and humidity or applying voltage and the life is predicted.

When evaluating solder bump reliability, special test element groups (TEG) are also used to divide defects into defects rooted in devices and defect modes inherent to solder bumps in order to evaluate the condition of just the solder bump junction.

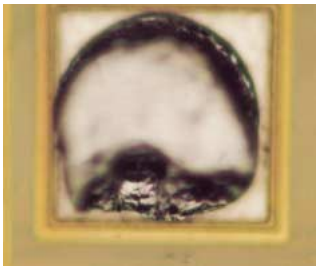
2.4.5.2 Tests

(1) Solder bump shear test

The solder bump shear test is used to evaluate the solder bump junction strength, and allows evaluation of the initial intermetallic compound condition. In addition, voids may occur within solder bumps during bump forming, so it is important to evaluate not just the strength but also the peeling break surface due to shearing. For solder bumps, if a stable alloy layer is formed, the obtained break surface is the ductile break surface within the solder. However, if the alloy layer is not stable, the break surface occurs at the bump and BLM film boundary, inside the BLM film, or along a void surface, etc. Fig. 2-16 shows a typical peeling break surface in a solder bump shear test.



(a) Normal shear surface



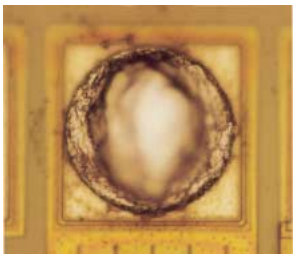
(b) Abnormal break surface
(void within the bump)

Photo 2-16 Peeling Break Surfaces Obtained in the Bump Shear Test

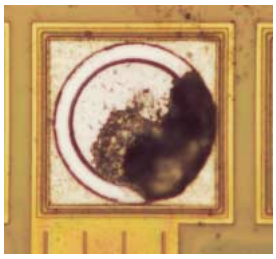
(2) Solder bump pull test

Like the shear test, the solder bump pull test also evaluates the solder bump junction strength. In particular, force also acts on the solder bump in the pull direction through encapsulating plastic swelling or hydrolysis in the PCT, high temperature and humidity bias and other tests, so it is important to evaluate the junction strength in the pull direction. Also like the shear test, it is important for the pull test to evaluate not just the strength but also the pull break surface.

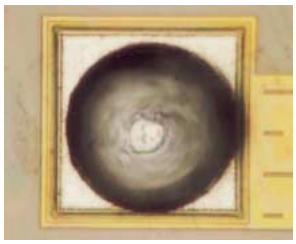
For solder bumps, if a stable alloy layer is formed, the obtained break surface is the ductile break surface within the solder as shown in Photo 2-17(a). However, if the alloy layer is not stable, the break surface occurs inside the BLM film as shown in Photo 2-17(b) or along a void as shown in Photo 2-17(c).



(a) Normal shear surface



(b) Abnormal break surface
(BLM strength deterioration)



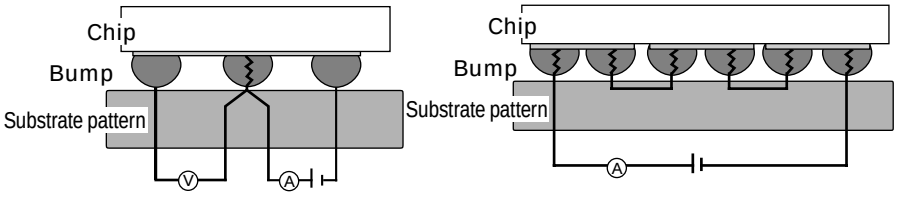
(c) Abnormal break surface
(void within the bump)

Photo 2-17 Peeling Break Surfaces Obtained in the Bump Pull Test

(3) Temperature cycle life test

The temperature cycle life test is used to evaluate deterioration of the solder bump junction strength due to thermal stress in the mounted condition. This is generally evaluated by measuring the bump connection resistance after mounting on a substrate and then judging defects by the degree of change in the connection resistance. The solder bump connection resistance is measured using the 4-wire and continuous measurement methods.

The 4-wire measurement method enables measurement of the connection resistance one bump at a time, so subtle rises in resistance due to micro-cracking can be monitored. Evaluation is easy, but there is also the disadvantage that measurement takes an extremely long time. The continuous measurement method forms a daisy chain to allow measurement of the resistance for all the bumps in each cycle, so the behavior at low and high temperatures can be monitored. Continuous measurement requires little measurement time, but there is also the disadvantage that the resistance value is large and subtle changes in the resistance cannot be detected. Fig. 2-28 shows an outline of the 4-wire and continuous measurement methods.



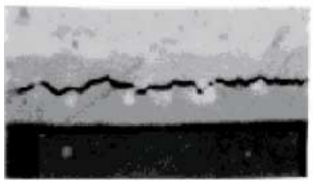
(a) 4-wire measurement pattern (b) Continuous measurement pattern

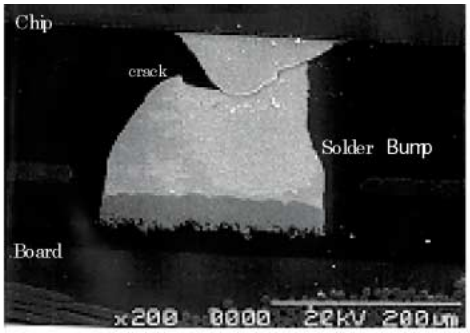
Fig. 2-28 Bump Connection Resistance Measurement Patterns

When evaluating the temperature cycle life of solder bumps, cracks occurring in solder bumps during the course of the temperature cycle may reunite and the resistance value may recover, or the connection may be open during the high temperature test but the resistance value may recover at room temperature. These phenomena may also not be observed due to differences in the bump or junction method, so it is important to carefully infer the failure modes when selecting the evaluation methods.

The failure mechanism may differ according to the test conditions, so it is important to determine the test conditions after first investigating whether market failure mechanisms can be reproduced.

Photo 2-18 shows typical solder bump failure mechanisms in the temperature cycle test.





(a) BLM cracking (b) Bump cracking

Photo 2-18 Failure Mechanisms in the Temperature Cycle Test

(4) High temperature operation and storage tests

The high temperature storage test is used to evaluate the deterioration in junction strength due to the growth of intermetallic compounds in the solder bump junction at high temperatures. Evaluation is possible using the same methods as in the temperature cycle test. However, the failure mode in the high temperature shelf test is a change in the junction resistance due to the growth of intermetallic compounds in the junction, and since the continuous measurement method has low measurement sensitivity which makes it difficult to detect subtle changes in the resistance, the 4-wire method is thought to be best.

Bearing in mind that this is a high temperature operation test using actual devices, the test conditions must be set in consideration of temperature rises during operation. The temperature is generally set at 125℃, although 150℃ may also be used in some cases.

In addition, the growth rate of intermetallic compounds greatly affects the life, so the junction reliability generally tends to be higher for slower intermetallic compound growth rates. That is to say, how to best form a stable alloy is a key point. For solder bumps, the BLM film quality and the solder constitution and crystal conditions also affect the life. Particular care must be taken when using copper in the BLM film. Copper and

silicon react easily and the diffusion speed of each within the other differ greatly, so Kirkendall voids form at the junction boundary, causing the strength to drop and the junction resistance to rise. This phenomenon also differs greatly according to the BLM film quality, the formation of intermetallic compounds during bump forming, and the bump crystalline structure.

(5) Moisture resistance test (High temperature and humidity bias test)

The high temperature and humidity bias test is used to evaluate migration due to deterioration of the bump junction strength caused by resin swelling or hydrolysis at high temperatures and humidity, or due to bump corrosion or the application of voltage. The evaluation method generally consists of measuring the inter-bump insulation resistance and then measuring the inter-bump migration life from the degree of insulation resistance deterioration. In addition, the effects of the mounting conditions (corrosion due to flux residue, migration) can also be evaluated. However, care must be taken as bump open defects cannot be detected by this method.

Like the temperature cycle test, the measurement method consists of applying the prescribed voltage at high temperatures and humidity and continuously measuring the insulation resistance.

Photo 2-19 shows an example solder bump failure mode in the high temperature and humidity bias test.

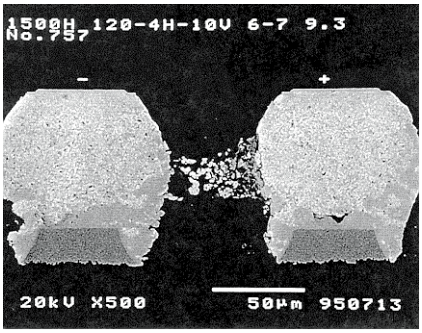


Photo 2-19 Failure Mechanism (Migration) in the High Temperature and Humidity Bias Test

(6) Moisture resistance test (PCT test)

The PCT test is a test item for evaluating the solder bump junction strength at high temperatures and humidity, and evaluation can be performed using the same methods as the temperature cycle test. This method is particularly effective for evaluating junction strength deterioration due to force on the bump in the pull direction caused by hydrolysis or swelling of the encapsulating mold resin used during mounting, or due to bump corrosion caused by the residue of the flux used during mounting.

Photo 2-20 shows an example solder bump failure mechanism in the PCT test.

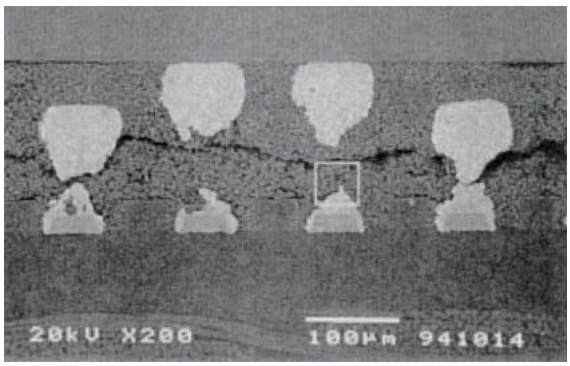


Photo 2-20 Failure Mechanism (Cracking due to plastic swelling) in the PCT Test

2.4.5.3 Summary

Numerous methods for forming bumps on Flip-Chip mount chips have been proposed by various companies. What these methods all have in common is that junctions are achieved by forming intermetallic compounds between bumps and the base coat metal film, and this junction condition greatly affects the bump reliability.

The most important items for bump reliability are:

- Stabilizing the intermetallic compounds formed between different metals such as the bump and the BLM film.
- Ensuring a strong and stable bump pull strength.

In addition, solder bumps are generally Flip-Chip mounted onto mounting substrates or other boards and the junction strength is reinforced by encapsulating the gaps with plastic to disperse and absorb the stress acting on the solder bump. When evaluating solder bump reliability, the effects of the mounting conditions (flux residue, washing damage, etc.) and the encapsulating mold resin must also be taken into account. Table 2-7 summarizes the failure mechanisms predicted for bump junctions and their primary factors.

Table 2-7 Bump Junction Failure Mechanisms and their Primary Factors

Failure mechanism	Primary factors	
Bump internal cracking, BLM cracking	Mounting substrate	Coefficient of linear expansion (α), Tg, modulus of bending elasticity, curved layer configuration, board materials, thickness, manufacturing method
	Bump	Constitution, bump height, bump size
	BLM	Junction strength, materials, BLM layer configuration, BLM thickness
	Encapsulating mold resin	Coefficient of linear expansion (α), Tg, modulus of bending elasticity, swelling, hydrolysis
	Chip	Size, thickness
	Mounting conditions	Flux residue, washing damage
Migration, corrosion	Encapsulating mold resin	Swelling, hydrolysis
	Mounting conditions	Flux residue
BLM diffusion	BLM	Junction strength, materials, BLM layer configuration, BLM thickness

2.4.6 Electrostatic Breakdown

2.4.6.1 Description

As element units become smaller and oxide films become thinner with the miniaturization of semiconductor devices, lower electrostatic discharge (ESD) breakdown voltages are becoming a serious problem. Protection circuits are used as a countermeasure in semiconductor devices to protect the internal circuits from electrostatics, but electrostatic countermeasures in the boad mounting process are also vital to prevent semiconductor devices from suffering electrostatic breakdown.

2.4.6.2 Static Electricity

Static electricity refers to when an object holds a charge and becomes electrically charged. When there is a surplus of electrons in an object it is negatively charged; when there is a shortage of electrons the object is positively charged.

In terms of general electrical properties, objects can be classified as items which easily acquire electrons and items which easily give electrons. Table 2-8 shows the so-called Faraday triboelectric series. Here, when a higher item in the triboelectric series contacts or rubs against a lower item, the higher item easily gives electrons and becomes positively charged, while the lower item easily acquires electrons and becomes negatively charged. Table 2-9 shows an example of typical charge voltages.

Table 2-8 Frictional triboelectric series Table[1)]

Positive (+)	Acetate
↑	Glass
↑	Nylon
↑	Wool
↑	Silk
↑	Aluminum
↑	Polyester
↑	Paper
↑	Cotton
↑	Steel
↑	Nickel, copper, silver
↑	Zinc
↑	Rubber
↑	Acrylic
↑	Polyurethane foam
Negative (–)	PVC (vinyl)
	Teflon

Table 2-9 Examples of Static Electricity Generation[2)]

Static electricity source	Charge voltage	
	Relative humidity 10% to 20%	Relative humidity 65% to 90%
Walking on carpet	35,000V	1,500V
Walking on vinyl tile	12,000V	250V
Person working at a general workbench	6,000V	100V
Card case	7,000V	600V
Plastic bag taken from a workbench	20,000V	1,200V
Urethane foam cushion chair	18,000V	1,500V

The two main mechanisms for generating static electricity which causes the ESD phenomenon within processes where semiconductor devices are handled are as follows.

(1) Charging due to contact and separation (rubbing) between objects

When two objects contact each other, a charge migrates between the objects at the contacting surfaces. (Fig. 2-29) If the objects are separated in this condition, the surface of each object retains this biased charge condition, and becomes electrostatically charged. Triboelectric charging is generally held to be the cause of static electricity, and can be thought of as the condition where this contact and separation occur repeatedly.

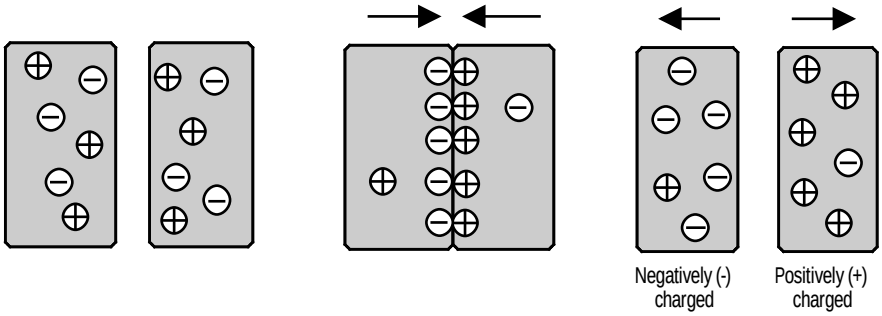


Fig. 2-29 Mechanism for Generating Charges through the Contact and Separation of Objects

(2) Charges due to induction from charged objects

When a charged object approaches an insulated conductor, the effect of the electric field from the charged object produces a charge bias due to electrostatic induction inside the conductor. (Fig. 2-30) In this condition, the conductor is in an inductively charged state. (Fig. 2-30(a)) When inductive charging occurs and the charge becomes uneven, if a part of the conductor contacts a ground (GND) or another conductor, a charge having the same polarity as the charged object which approached moves from the conductor to the GND or the other conductor, and the ESD phenomenon occurs. (Fig. 2-30(b)) Furthermore, if the conductor is then separated from the GND and the charged object is moved away from the conductor, the charge in the conductor that was attracted to the charged object becomes free and exists in surplus inside the conductor, which becomes charged with that polarity. (Fig. 2-30(c)). If a part of the conductor then contacts the ground (GND) or another conductor again in this condition, the charge is discharged. (Fig. 2-30(d))

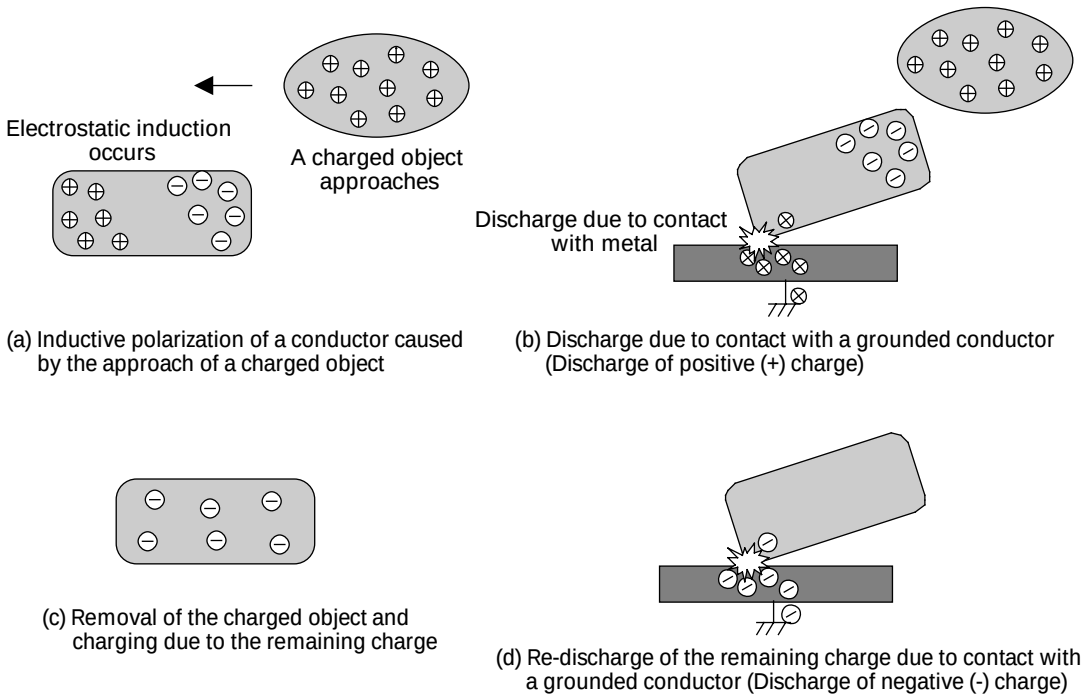


Fig. 2-30 Generation of an Inductive Charge Due to the Approach of a Charged Object and the Double-Discharge Phenomenon

When this charge phenomenon is applied to semiconductor devices, the chip and lead frame are treated as conductors. Simply bringing a charged object close to an insulated semiconductor device generates an inductive charge in the chip, and there is the risk of ESD occurring if the pins are contacted with metal. Also, if the surface of a plastic package becomes charged by rubbing or other, the surface may act as a charged object to generate an inductive charge in the chip, thus causing ESD in the same manner by inductive charging.

This type of inductive charging occurs not only in semiconductor devices, but also in ungrounded metal objects. For example, the same type of inductive charge is produced in tweezers or other tools held by an insulated glove or finger sacks, PCB substrate wiring patterns, FPC metal wiring and other objects. These items may cause ESD with respect to semiconductor devices in the mounting process.

In this manner, eliminating charged objects which cause inductive charges in devices is an important countermeasure when handling semiconductor devices within processes.

2.4.6.3 ESD Test Methods

Electrostatic discharge phenomena produced by handling semiconductor devices are classified into a number of models according to the charged object and the discharge mode. The testing methods used to evaluate the resistance of semiconductor devices to electrostatic discharge were devised based on these electrostatic discharge models.

(1) Human Body Model (HBM) [3),4),5)]

The human body model is a testing method which models the discharge of electrostatic charge accumulated in a charged human body to a semiconductor device. This testing method represents the capacitance of the human body and the contact resistance between the human body and the device using a 100 pF capacitor and a 1500 Ω resistor. This testing method has been used for quite some time in the U.S. MIL standard (MIL-STD-883D method3015.7), and is thus widespread overseas. In Japan it was formally adopted as one of the testing methods in the EIAJ (Electronic Industries Association of Japan) standard in 1988. The 1994 revision (EIAJ ED-4701-1 C111A) positioned the conventional machine model (200 pF/0 Ω) testing method as a reference test, so the HBM is currently prescribed as the standard testing method for the EIAJ standard.

The HBM discharge waveform is prescribed by the MIL and JEDEC standards, so there is little data variance between testing equipment, and the HBM is considered to be a testing method which allows fair comparison of test results between multiple device manufacturers and users.

(2) Machine Model (MM) [3),6)]

The machine model ESD testing method originated as a human body discharge model based on the worst values for human body capacitance and discharge resistance (200 pF/0 Ω). This testing method was used by domestic semiconductor device manufacturers mainly as a means of discovering circuits which are susceptible to electrostatic breakdown during the device design verification. These test results were then presented to users as ESD withstand voltage data for semiconductor devices, and this method spread as a testing method for determining the ESD withstand voltage of semiconductor devices between domestic device manufacturers and users.

When this testing method was just starting to spread, many device manufacturing processes and user mounting processes were still being performed by hand, and there was a lack of ESD protective items with superior characteristics such as exist now. Therefore, it is said that the electrostatic breakdown phenomenon occurring in processes matched with the test results using this model in many cases. However, recent automated assembly and mounting processes which mainly use surface mounted packages have reduced the chances for electrostatic discharge to occur directly from workers to devices, so cases of MM test breakdown modes occurring in processes have become extremely rare. In addition, this testing method did not prescribe the discharge waveform of the testing equipment, so the ESD endurance voltage varied greatly according to the testing equipment and there were many problems where the results of tests performed by manufacturers and users differed greatly.

With the 1994 EIAJ standard revision, the MM testing method was changed from a formal testing method to treatment as a reference test on the assumption of future abolition.

(3) Charged Device Model (CDM) [7)~11)]/Charged Package Model (CPM) [12)]

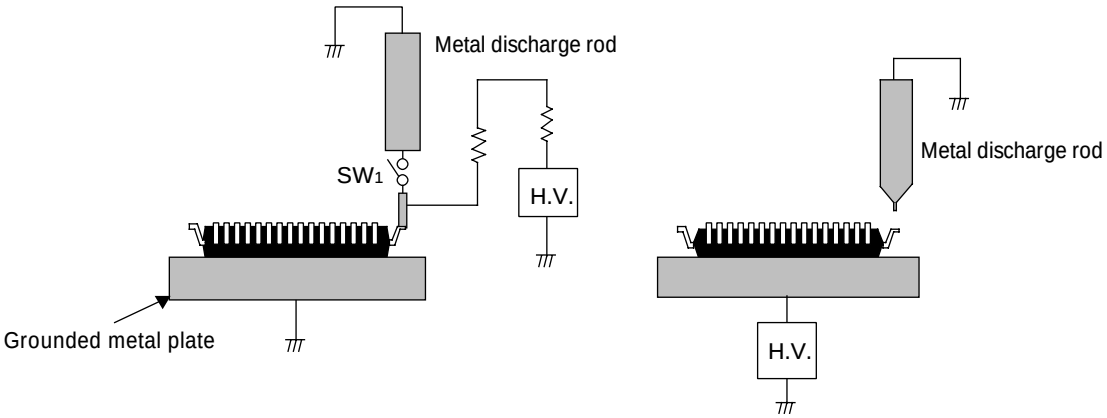
The charged device model/charged package model is a testing method which models the phenomenon where the semiconductor device itself carries a charge or where the charge inducted to the device from a charged object near the device is discharged.

This model is characteristic in that it reproduces the discharge mechanism in the form closest to the discharge

phenomenon occurring in the field. In addition, numerous correlations with the ESD failure modes occurring in processes have also been confirmed.

The CDM and CPM testing methods are shown in Fig. 2-31. CDM connects a high voltage source to the device side and accumulates a charge in the parasitic capacitance formed between a grounded electrode plate and the device. This accumulated charge is then discharged to the GND via a metal discharge rod by closing SW1 which is connected to a device pin. CPM applies high voltage to the metal plate side and generates a charge by producing an inductive charge inside the device. This charge is then discharged by contacting a grounded metal rod to a device pin.

The charging and discharging methods differ for these two testing methods, but the discharge phenomenon from the device is considered to be the same, so they are viewed as the same testing method. In either testing method, charging and discharging are repeated for each pin, and the device withstand voltage is evaluated by ultimately applying stress to all pins



(a) CDM (Relay discharge)　　(b) CPM (Aerial discharge)

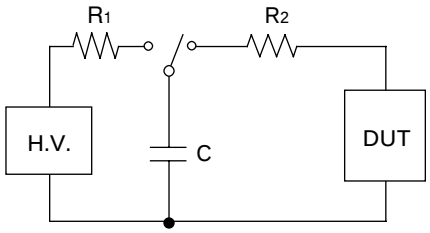
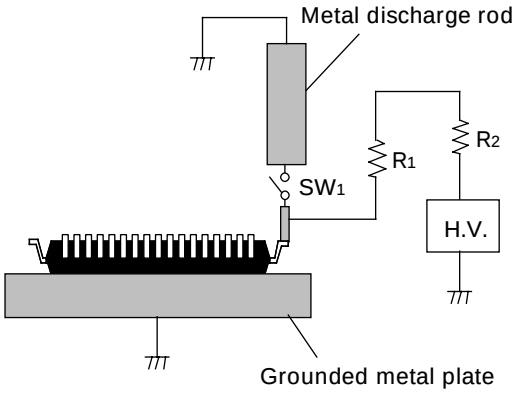
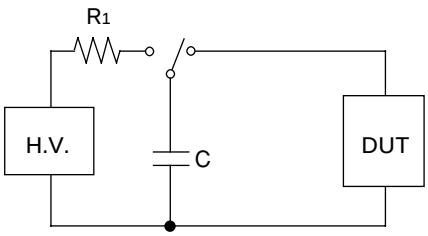
Fig. 2-31 CDM/CPM Testing Methods

(4) ESD Test Standards

ESD testing methods currently prescribed as official standards are shown in Table 2-10. The HBM, CDM/CPM and MM testing models are each prescribed as standards. In the Japanese domestic EIAJ standard, MM is treated as a reference test and CDM/CPM are still in the preliminary standard (EDX-4702) stage. In the U.S., the HBM testing method is standardized in the MIL standard, and the HBM, CDM and MM testing methods are standardized in the JEDEC standard.

By standardizing the discharge waveforms, these testing standards aim to reduce variance in the failure endurance voltage between testing equipment, ensure ESD resistance data correlation between device manufacturers and between manufacturers and users, and eliminate disadvantages due to differences in testing equipment. Currently HBM is the only testing method for which waveform regulations are unified for the most part between standards.

Table 2-10 List of Semiconductor ESD Testing Methods and Corresponding Standards

Testing model	Test circuit	Standards
Human Body Model (HBM)	 C = 100pF R2 = 1500Ω Number of applications: 3	EIAJ ED-4701 C111A C-111A (1994) EIA/JESD22-A114-A (1997) ESD Ass. S5.1 (1993) MIL-STD-883D Method.3015.7 (1989)
Charged Device Model (CDM)	 Number of applications: 1	EIAJ EDX-4702(1994) JESD22-C101(1995)
Machine Model (MM)	 C = 200pF R = 0Ω Number of applications: 1	EIAJ ED-4701 C111A (1994) (Reference test) EIA/JESD22-A115-A (1997)

2.4.6.4 Failure Mechanisms due to ESD Breakdown

The main ESD breakdown mechanisms for semiconductor devices include the following phenomena.

(1) Thermal breakdown (junction breakdown, melted wiring)

(2) Insulating film breakdown (gate oxide breakdown, interlayer insulator breakdown)

(1) Thermal breakdown

Thermal breakdown phenomena mainly include junction breakdown and melted wiring. Junction breakdown can occur at relatively low energy, but melted wiring generally requires high energy, so it is thought to occur more from electric over stress (EOS) phenomena (lightning surge, soldering iron leaks, etc.) than due to ESD.

The junction breakdown phenomenon occurs when an excessive current flowing through the junction causes the temperature to rise locally in the junction and exceed the melting point of silicon (1415℃). The Wunsch & Bell model which uses a thermal diffusion equation is most generally used as a model to describe this junction breakdown. This model determines the junction breakdown phenomenon from the applied pulse width and the power density applied to the element.

Thermal breakdown requires relatively high energy, so within the process it is caused by discharge from a charged worker (human body) or discharge of the charge accumulated in a large-capacity condenser or other mounted component via the boad when mounting the semiconductor device onto a boad.

(2) Insulating film breakdown

Insulating film breakdown is a failure mechanism where the gate oxide film or the interlayer insulator shorts. Insulating film breakdown occurs often in MOS and other devices with thin gate oxide, and is the most common ESD breakdown failure mechanism seen within the process. The energy required for breakdown is small, so this phenomenon may occur at lower charge levels than thermal breakdown.

2.4.7 Latch-up Phenomenon

2.4.7.1 Description

Aside from the design circuits formed inside ICs, parasitic transistors comprised by the device structure may be triggered by external noise (surge) or other factors, resulting in the latch-up phenomenon where an excessive current flows continuously. CMOS devices inherently comprise bipolar parasitic transistor circuits which have the same structure as PNPN thyristors, and when these parasitic thyristors are triggered by an external surge or other factors, the latch-up phenomenon occurs. This results in IC operation defects or breakdowns, and poses a serious problem for practical use.

2.4.7.2 Latch-up Mechanism

Fig. 2-32 shows an example of when a positive external surge enters from the output pin of a CMOS IC.

① The external surge is applied to an output pin and the output pin potential becomes higher than V_{DD}.

② The p-ch transistor source potential rises, the area between the parasitic PNP transistor Tr_1 base and emitter becomes forward biased, and the current injected to n-sub flows through Rs to V_{DD}.

③ Tr_1 is triggered and the Tr_1 collector current flows through the Rw inside the p-well to V_{SS}.

④ A potential difference is produced at both ends of Rw, and Tr_2 is triggered.

⑤ The increase in the Tr_2 collector current produces a potential difference at both ends of Rs, and Tr_3 is triggered.

⑥ The parasitic thyristor structure comprised by Tr_2 and Tr_3 is triggered, and a current path is formed from V_{DD} to V_{SS}. As a result, positive feedback is applied to the circuit comprised of parasitic NPN transistor Tr_2 and PNP transistor Tr_3, and current flows constantly between V_{DD} and V_{SS}, causing latch-up.

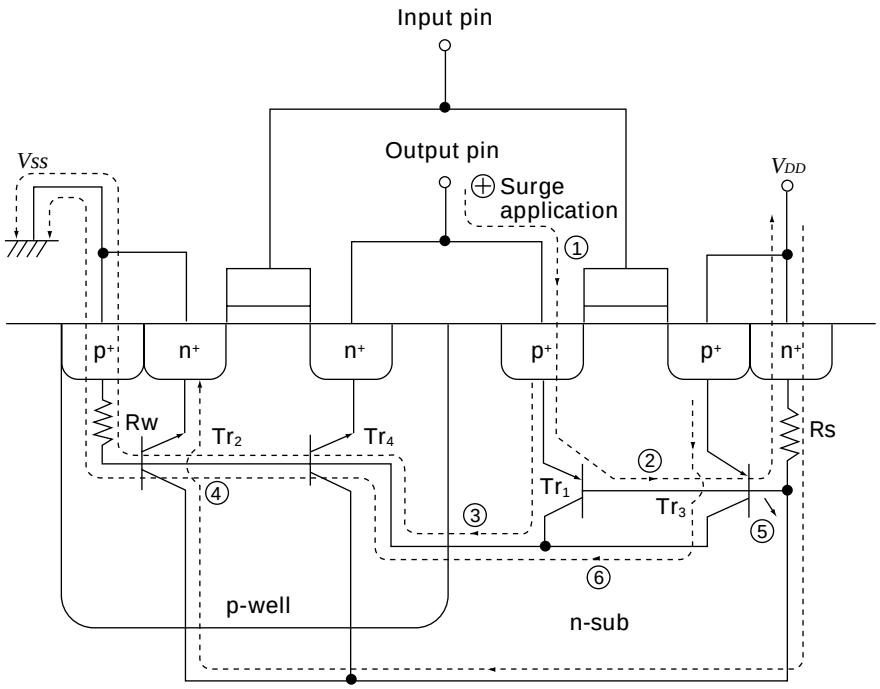


Fig. 2-32 Mechanism for Generating Latch-up at an Output Pin (for a positive external surge)

2.4.7.3 Methods for Measuring Latch-up[3)]

(1) Latch-up testing methods

There are two main testing methods known as typical methods for testing latch-up.

Pulse current injection method

This method applies a certain trigger pulse current in stages to input and output pins in the condition with the supply voltage applied to the device, and measures whether latch-up occurs. Latch-up is judged by the change in the supply current value. The pulse current at the point when a supply current of the individually prescribed failure criterea or higher flows is used as the latch-up current value for that device. This testing method is characteristic in that it specifies the pulse waveform conditions, so it has excellent reproducibility.

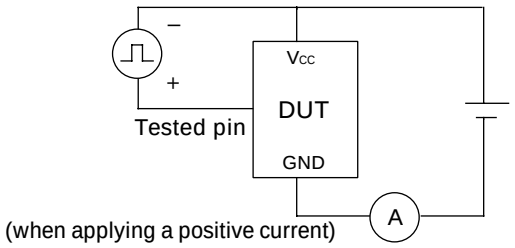
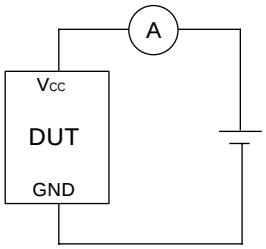
Power supply overvoltage method

This method adds a trigger pulse voltage to the supply voltage and determines whether latch-up occurs. Latch-up is judged by the change in the supply current value.

(2) Latch-up testing standards

Table 2-11 shows the latch-up testing methods currently prescribed as official standards. The current injection method and the power supply overvoltage method are both prescribed as standards.

Table 2-11 List of Semiconductor Latch-up Testing Methods and Corresponding Standards

Testing model	Test circuit	Standards
Current injection method		EIAJ ED-4701-1 C-113 (1994) EIA/JESD78 (1997)
Power supply overvoltage method		EIAJ ED-4701-1 C-113 (1994) EIA/JESD78 (1998)

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1) Itoh and Adachi, “Electrostatic Discharge Countermeasures for Electrical Equipment Components”, Denshi-Gijutsu (Electronic Technology), July issue, pp.17-44 (1987).
2) 「MIL-HDBK-263A MILITARY HANDBOOK」 1991. 2. 22 Electrostatic Discharge Control Handbook for Protection of Electrical and Electrostatic Parts.
3) “EIAJ ED-4701 Semiconductor Device Environment and Durability Testing Methods”, Electronic Industries Association of Japan (1994).
4) 「MIL-STD-883D Test Method 3015.7: Electrostatic Discharge Sensitivity Classification」 Military Standard for Test Methods and Procedures for Microelectronics.
5) EIA/JESD 22-A114-A, JEDEC (1997).
6) EIA/JESD 22-A115-A, JEDEC (1997).
7) “EIAJ EDX-4702 Electrostatic Discharge Breakdown Testing Method for Semiconductor Devices (Charged Device Model)”, Electronic Industries Association of Japan (1994).
8) 「JESD22-C101」 Joint Electron Device Engineering Council Standard (1995).
9) 「ESD-DS5.3-1996: Electrostatic Discharge Sensitivity Testing Charged Device Model (CDM)」 Draft Standard for Electronic Discharge Association.
10) B. A. Unger, “Electrostatic Discharge Failure of Semiconductor Devices.” 19th. Annual IRPS Proc. (1981).
11) T. S. Speakman, “A Mode for Failure of Bipolar Silicon Integrated Circuit Subjected to Electrostatic Discharge.” 12th. Annual IRPS Proc. (1974).
12) Fukuda et al., “Electrostatic Discharge Breakdown Evaluation Method for MOS Devices - Package Charge Testing Method and Test Results”, Inst. Electrical and Communications Engineers of Japan, R03-33 (1983).

2.4.8 Color CCD Image Sensors Optical Reliability

CCD image sensors for color cameras consist of an organic color filter formed on a CCD which is formed on a silicon substrate. When strong light is continuously radiated to this color filter, the absorbed optical energy produces a photochemical reaction in the pigment molecules, causing the pigments to decompose and the chromaticity to change (color fading).

The rate at which the pigments decompose due to this photochemical reaction is thought to be proportional to the total amount of optical energy (including the reaction efficiency) absorbed by the pigments per unit time, so the light resistance life can generally be expressed as the product of the illuminance at the CCD image surface and the irradiation time. The illuminance at the CCD image surface can be obtained from the following formula.

$$\text{Image surface illuminance } (\text{lx}) = \frac{\text{Light source brightness } (\text{cd/m}^2) \times \pi \times \tau}{4 \times F^2 \times (1+N)^2}$$

τ : Transmittance of the lens, filter, etc.
F : Lens F value
N : Image formation multiple

The effect of changes in the chromaticity on picture quality differs according to the distribution and wavelength of the irradiated light, and the chromaticity fluctuation rate increases in areas where strong light or light on the high energy, short wavelength side of the spectrum (blue light) is irradiated. Temperature also has an effect, with the chromaticity changing more at higher temperatures. For applications which continuously image a fixed picture such as surveillance cameras, or when imaging with a bright point light source (sun, etc.) in the picture for long periods, the chromaticity on the image screen changes according to the distribution of the light incident to the color filter, and may appear as the image retention phenomenon in the picture.

2.4.9 LCD Optical Reliability

2.4.9.1 Description

The Sony Semiconductor LCD products include low temperature polysilicon thin film transistor (TFT) process LCDs used mainly for direct-view display applications, and high temperature polysilicon TFT process LCDs used for video camera viewfinder and LCD projector applications. External stress factors adversely affecting the reliability of these LCDs include general semiconductor stress factors and also the existence of light incident to LCDs.

Light stress on direct-view application LCDs is mainly natural light such as the sun's rays, so there are virtually no problems with optical reliability as long as these LCDs are not left exposed to direct sunlight for long periods or otherwise subjected to harsh environments. However, projector LCDs have an extremely large light density incident to the panel, and strong light stress is applied for long periods, so reliability problems due to incident light may occur depending on the method of use. This section discusses the optical reliability mainly of LCDs used for projector applications.

2.4.9.2 Deterioration Mechanisms

Reliability and characteristics problems caused by light incident to projector LCDs fall under two main phenomena. The first phenomenon is changes to the molecular structure of the organic compounds due to photochemical reactions caused by optical energy absorbed by the organic materials used. The other phenomenon is changes in the pixel potential due to electron-hole pairs generated when light straying to the pixel transistors is absorbed by the TFT transistor bulk.

(1) Deterioration due to photochemical reactions in the organic materials

Changes to the molecular structure of the organic compounds due to incident light are thought to be caused by the phenomenon where optical energy absorbed by the organic compound produces a photochemical reaction which causes dissociation of the organic bonds. As the photochemical reaction of the organic compound progresses, the picture quality may be affected by a drop in the orientation of the liquid crystals or the generation of ions.

The rate of the light-induced chemical reaction can be obtained using an Arrhenius equation expressing the function f (λ) of the absorbed energy that contributes to the photochemical reaction, the function f (P) of the incident light quantity, and the temperature dependence of the chemical reaction rate.

$$L = A \cdot f(\lambda) \cdot f(P) \cdot \exp\left(\frac{Ea}{kT}\right)$$

The photochemical reaction rate is proportional to the amount of optical energy absorbed, so the reaction rate becomes faster as the incident light quantity increases or as ultraviolet light with high photon energy is absorbed. Thus, the light exposure lifetime can be extended by cutting as much as possible of the undesired ultraviolet or near ultraviolet light from the wavelength component of the light incident to the LCD panel, or by lowering the panel temperature to suppress the photochemical reaction.

(2) Signal charge fluctuation due to light absorption by pixel transistors

A pixel transistor comprises one pixel of the LCD. These transistors are photo-shielded on the top and bottom by a metal layer to prevent fluctuations in the characteristics due to light incident to the transistors. However, light diffracted by the edges of the photo-shielding film or light incident to the panel from an angle may stray and reflect from the edge of the photo-shielding metal and penetrate to the TFT transistor portion. In this case, light absorption by the bulk generates electron-hole pairs and causes the phenomenon where the pixel potential changes.

When light incident to a pixel transistor is absorbed by the transistor bulk, electron-hole pairs are generated inside the bulk by photoelectric conversion. For the electron-hole pairs generated in the depletion layer on the pixel electrode side of the TFT transistor, the electric field inside the depletion layer causes the electrons to migrate toward the pixel electrode side and the holes to migrate toward the drain side. When electrons migrate toward the pixel electrode side, the pixel potential on which the video signal is written fluctuates and the electric field applied to the liquid crystal changes. If the incident light intensity increases, causing the generated electron-hole pairs to increase and amount of electrons flowing to the pixel electrode to exceed a certain level, the normal hold voltage cannot be maintained and the picture quality may deteriorate.

This phenomenon is not progressive, so there is no effect on long-term reliability. However, it is an index indicating the characteristics limit with respect to the incident light quantity.

2.4.9.3 Light exposure test Method

Fig. 2-33 shows the optical system of the device used to light exposure test of projector LCDs. The light source is the high voltage mercury (UHP) lamp generally used in projectors, and changes in the optical characteristics are evaluated by irradiating light so that the condensing lens condenses light evenly to the LCD panel surface.

The main acceleration factors in the light exposure test are control of the incident light quantity and the panel temperature.

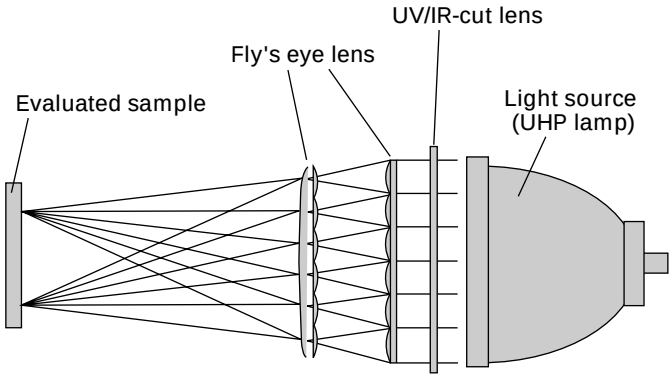


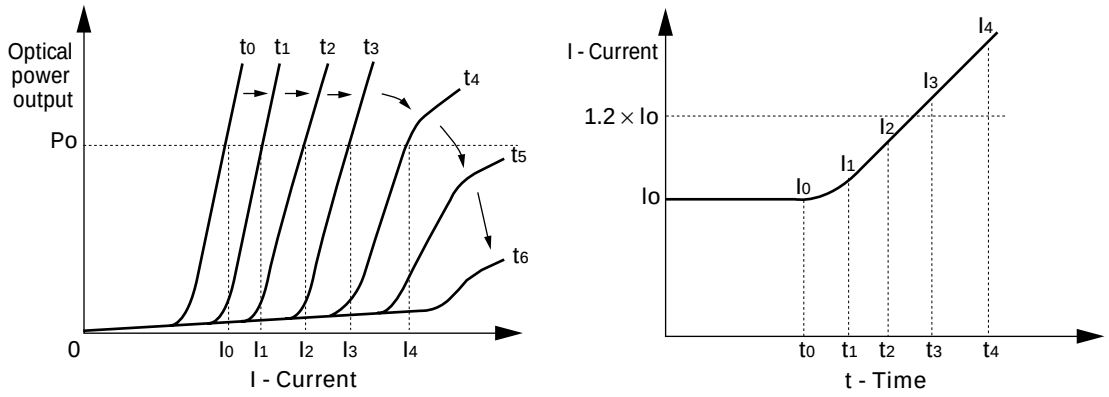
Fig. 2-33 Light exposure test system

2.4.10 Laser Diode (LD) Reliability

2.4.10.1 LD Failure

When laser diodes, which are light emitting elements, operate in the forward direction, the increase in current which does not contribute to light emission causes the light emission characteristics to change over time. Among these characteristics, the element life is generally defined by the time-dependent change in optical power output vs. operating current characteristics, which have a large effect on the drive circuit. This is shown in Fig. 2-34(a). When automatic power control (APC) drive which maintains a constant optical power output is performed, light emission at the constant optical power output P_0 is no longer possible at time t_5.

In consideration of the effect on systems using laser diodes, Sony defines the laser diode life as the time when the operating current becomes 1.2 times the initial value. (Fig. 2-34(b)) However, as shown in Fig. 2-34(a), this does not mean that the laser diode is no longer able to emit light.



(a) Time-dependent change in optical power output vs. operating current characteristics

(b) Time-dependent change in optical power output vs. constant value operating current

Fig. 2-34 Time-dependent Changes in Optical Operation Current Characteristics

2.4.10.2 Degradation Factors

Laser diode reliability is closely related to the operating temperature, and the degradation speed rises exponentially with the operating temperature (rise in drive current per unit time: ΔIop/Δt). This relationship can be expressed as follows.

$$\tau \propto \frac{\Delta Iop}{\Delta t} \propto \exp\left(\frac{-Ea}{kT}\right)$$

Ea : Activation energy (eV)
k : Boltzmann's constant (8.616×10^{-5}eV/K)
T : Absolute temperature (K)

Based on the relation between the temperature and drive current rise ratio, laser diode degradation is generally obtained at Ea ≒ 0.7 eV[1)], so near room temperature the life drops to approximately 1/2.2 for a temperature rise of 10℃. Equipment sizes are becoming more compact, so sufficient care must be given to thermal design to suppress laser diode temperature rises. In addition, the degradation speed generally becomes faster at temperatures in excess of the specified operating temperature upper limit, so sufficient care must be given to extrapolation using Ea ≒ 0.7 eV in consideration of reliability. In this manner, degradation which determines the long-term life is called degradation in the gradual degradation mode, or wear degradation. This wear degradation accelerates as the optical power output increases. Therefore, use within the range of the specified upper limit optical power output or less is important for obtaining sufficient reliability.

Laser diode failure during use is often edge degradation caused by a surge current or overcurrent. In laser diodes, as the current is raised to increase the optical power output, at a certain point the optical power output drops suddenly and irreversible damage occurs. This type of degradation is also called catastrophic optical damage (COD), and occurs when high optical power output density operation causes momentary melting of a part of the laser diode edge and the formation of crystal defects. Semiconductor devices are generally susceptible to surge currents, and laser diodes with a high response speed of 1 GHz or faster and a low operating voltage of approximately 2 V in particular are damaged instantly by surges. This is an inherent failure mechanism of laser diodes. In order to avoid this COD failure due to surges, it is necessary to prevent even momentary excessive optical power output from being generated by a momentary overcurrent entering from the power supply or surges. In addition, even if a relatively weak surge is applied and there is little initial deterioration in the laser diode characteristics, this has been confirmed to shorten the operating life thereafter, so care should be taken.

Laser diodes also deteriorate and fail due to crystal defects. Perfect semiconductor crystals have structures with a regular atom arrangement, but actual semiconductor crystals have crystal defects which are non-conforming portions in the atom arrangement. In addition, crystal defects may also be produced by mechanical stress applied to semiconductor chips in the laser diode manufacturing process. These crystal defects inside laser diodes have non-light emitting properties, and the energy provided when the power is on is converted to heat instead of light. Dark line defects (DLD) are when a dislocation, which is a type of crystal defect, grows and expands while the power is on. These DLD expand and grow faster at larger current densities or higher operating temperatures, and can cause degradation or failure. AlGaAs laser diodes often experience laser diode degradation due to DLD at approximately 100 hours, and this is called degradation by the rapid degradation mode.

2.4.10.3 Methods for Estimating Life

The average life of laser diodes is generally expressed by the mean time to failure (MTTF) obtained from high temperature accelerated life test data and Weibull charts. The estimated average failure time at room temperature for compact disc laser diodes obtained using the average failure time and activation energy at 70℃ is one million hours or more, indicating sufficient reliability for practical use.

Life tests are conducted on element lots screened using fixed methods to confirm that elements satisfy the demanded average life and have no initial failures, and the relation between the cumulative failure rate and the drive time is investigated. Fig. 2-35 shows an example Weibull chart. The life prediction calculated using a degradation activation energy of 0.7 eV is shown by the dotted line. The plotted life data shows that the laser in this figure has a failure rate in the accidental failure (m = 1) range, and that the average life (MTTF) corresponding to the time for 63.2% of all test samples to fail is one million hours or more at room temperature.

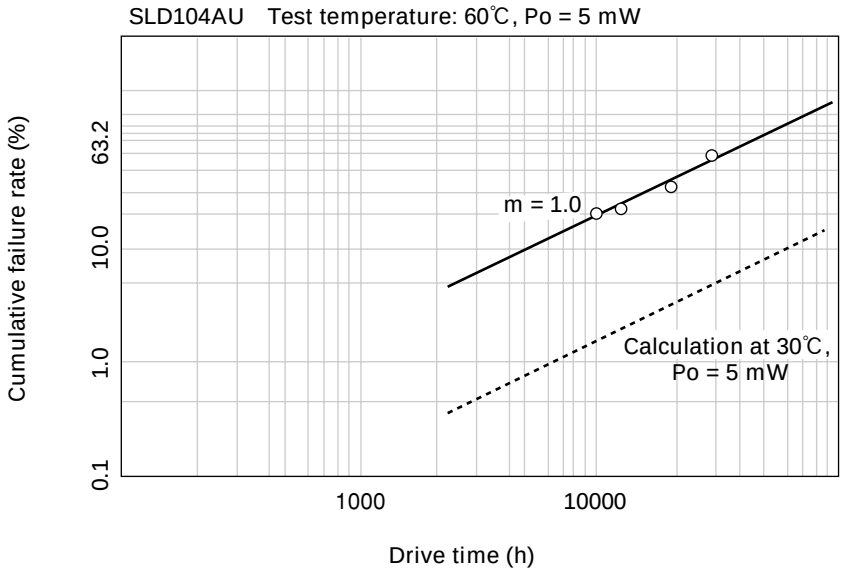


Fig. 2-35 SLD104AU Accelerated Life Test Results

2.4.10.4 Failure Analysis

When trouble occurs in laser diodes, an overall inquiry is made as to the cause by investigating the electrical and optical characteristics and observing the laser diode with optical microscopes and SEM, etc.

When current flows through a laser diode, the stripe portion emits light, and the cause of the failure is generally inferred by observing this emitted light. The observed positions are the laser diode edges which emit light, and the entire stripe portion which is observed by removing the photo-shielding electrode and semiconductor layers from the inside of the laser diode.

This section presents failure analysis methods using the light emission characteristics which differ from general semiconductor devices.

(1) Analysis of light emission at the laser light emission edges

Laser diode failure during use is often edge degradation due to a surge current or overcurrent. This degradation is also called catastrophic optical damage (COD), and occurs when high optical power output

density operation causes momentary melting of a part of the laser diode edge and the formation of crystal defects. This melted portion absorbs light, so it is observed as degradation of the laser diode characteristics. When the operating current needed to obtain a certain optical power output increases (large Iop), the rated output is not produced, the laser diode does not oscillate, or an extremely large overcurrent flows, this is viewed as a failure such as current being unable to flow. Fig. 2-36 shows the device configuration for observing edge light emission.

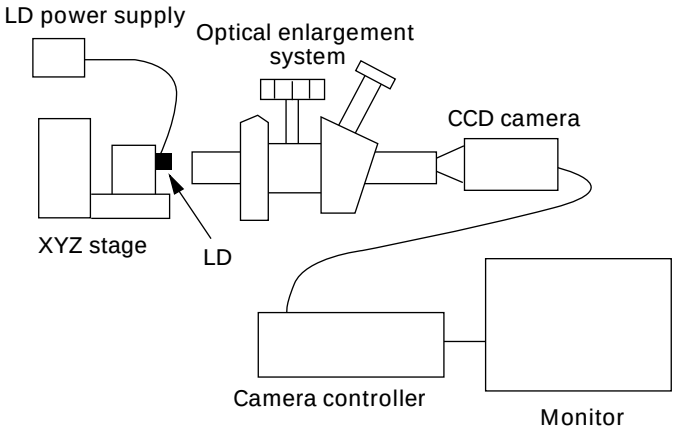


Fig. 2-36 Device for Observing Edge Light Emission

A low current of several mA is flowed to the laser diode to make it emit light, and the light intensity distribution at the light emission edge is observed (near field pattern observation). Normal laser diodes exhibit a Gaussian distribution as shown in Photo 2-21. During laser oscillation, the light density is highest in the center of the light emission area of the light emission edge, so crystal melting occurs in this location. Therefore, when the center of the near field pattern appears dark and forms a double peak or when the pattern appears divided into a number of peaks, this indicates that a surge or overcurrent has been applied and edge degradation has caused a light absorbing area near the center of the light emission area. (Photo 2-22)

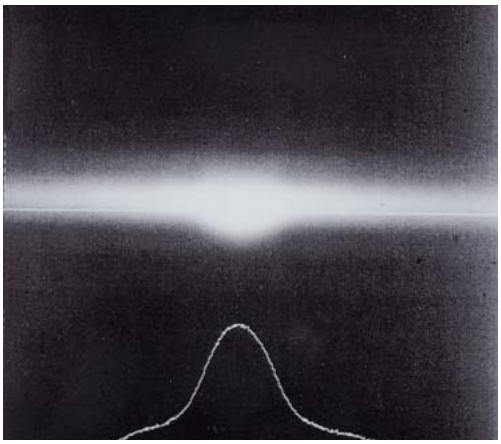


Photo 2-21 Normal Edge Light Emission Pattern

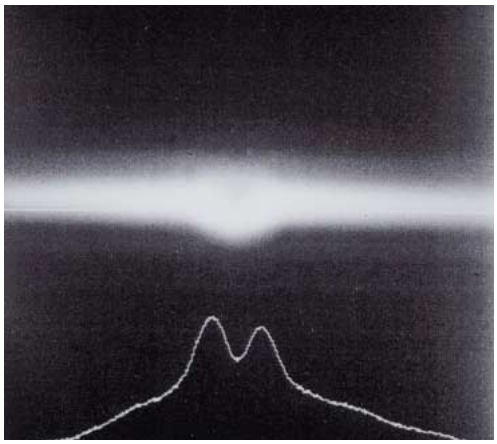


Photo 2-22 Degraded Edge Light Emission Pattern

(2) Analysis of light emission over the entire laser diode surface

For test samples where abnormalities are not visible by observing light emission from the edges or when defects occur inside the laser diode chip, the entire stripe must be analyzed. The cathode luminescence method allows observation of the entire stripe of failed laser diodes. This is done by removing the photo-shielding electrode and semiconductor layers using chemical etching to allow observation of light emission from the light emitting layer inside the laser diode chip. Then, the light emitting layer of the laser diode is made to emit light by irradiating it with electron rays instead of flowing current. If the emitting layer contains a DLD, this makes it possible to accurately know the DLD shape, orientation and resolution. Photos 2-23 and 2-24 show cathode luminescence images of a laser diode in which a crystal defect called a <110> DLD has formed near the edge. In addition, a faint <100> DLD can also be seen.

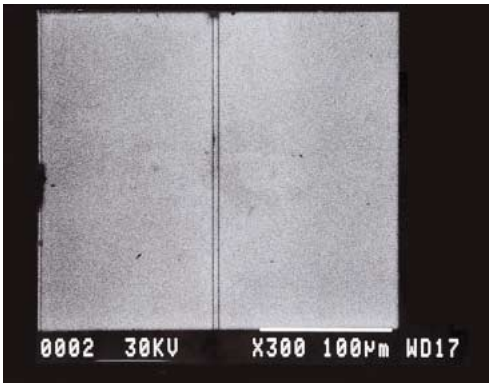


Photo 2-23 Cathode Luminescence Image of a Laser Diode with a Crystal Defect near the Edge

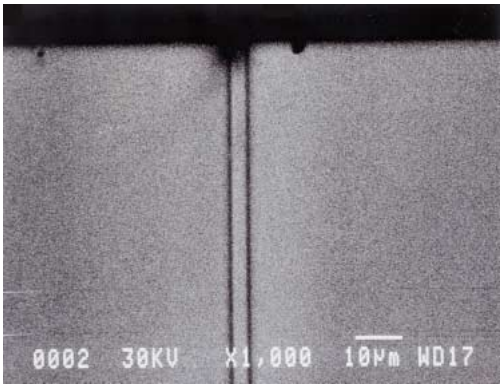


Photo 2-24 Enlarged View

<References>

1) R. L. Hartman and R. W. Dixon, “Appl. Phys. Lett. 26”, pp.239-242 (1975).

CHAPTER 3 - FAILURE ANALYSIS

3

CHAPTER 3 - FAILURE ANALYSIS

3.1 What is Failure Analysis?

Failure analysis consists of confirming reported failures and clarifying failure modes or mechanisms using electrical measurements and various scientific analysis technologies.

This chapter introduces specific failure analysis methods. However, before performing the actual analysis work it is necessary to thoroughly investigate failure circumstances and accurately understand the failure contents. This makes it possible to determine the optimum analysis methods and carry out swift processing.

Fig. 3-1 shows an example failure analysis procedure.

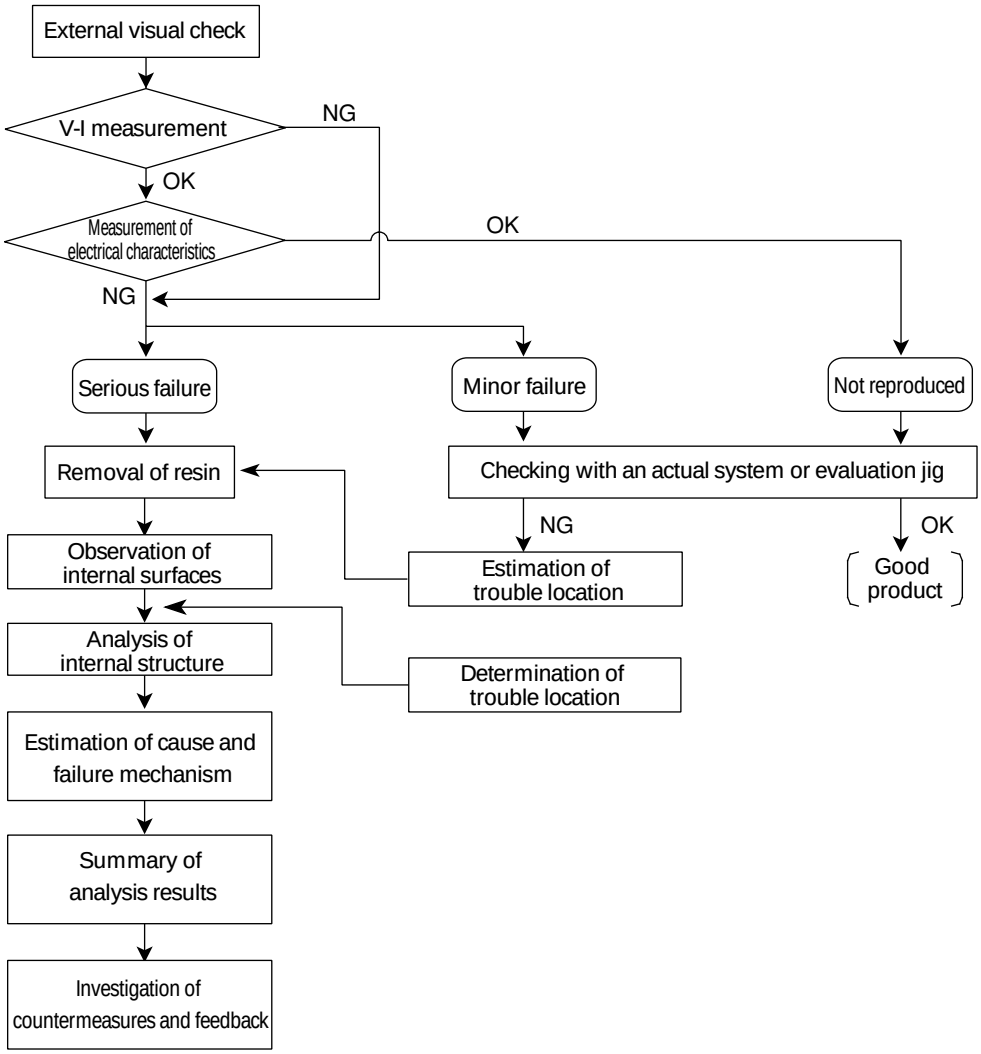


Fig. 3-1 Failure Analysis Procedure

3.2 Necessity of Failure Analysis

As semiconductor devices become more highly integrated and incorporate more advanced functions, manufacturing processes are becoming more miniaturized and complex, and include diverse reliability factors. In addition, semiconductor devices have come to be used over an extremely wide range of fields, so failure causes and mechanisms are also complex.

Under these circumstances, an extremely high reliability level is required of semiconductor devices.

Reliability must be built in from the device development stage to the manufacturing stage in order to ensure a high level of reliability. Therefore, it is important to analyze failed products occurring in reliability tests, customer processes and the market, clarify failure modes and mechanisms, and provide feedback to improve the manufacturing and design processes.

Failure analysis is not simply investigating the failure causes and mechanisms of failed products. It is a vital and essential technical field for the design and manufacture of high quality and high reliability devices.

3.3 Failure Analysis

3.3.1 Investigation of Failure Circumstances

When failures occur, it is important to understand the failure circumstances in order to determine the failure analysis methods and procedures so that failure analysis can proceed smoothly.

When a failure sample is obtained, as much information as possible about that sample is gathered at the same time. The product name, production lot number, number of failures and failure rate, trouble contents, mounting conditions, place where the trouble occurred, circuits used, operating conditions, environmental conditions and other information are understood accurately and compiled into a list to assist in estimation of the failure mechanism and simulations, etc.

3.3.2 Handling of Failure Samples

Failure samples contain a great deal of information, and are highly valuable as their number is limited. If failure analysis is unsuccessful it is possible that no information may be obtained. Therefore, the following precautions should be observed when handling failure samples.

(1) Maintenance of failure conditions

If stress (mechanical, electrical, thermal) which changes the failure conditions is applied prior to analysis, accurate analysis is impossible.

Therefore, failure samples must be processed and stored in a manner which maintains the failure conditions.

(2) Lead processing

When analyzing devices which are solder-mounted onto substrates, samples removed from substrates may require lead processing for LSI tester measurement or other analysis. The utmost care should be taken during this processing not to apply heat to the device or to damage the leads.

(3) Storage

In addition to the identification of samples, care must also be taken for storage.

Care must be taken for environmental factors such as temperature and humidity, and also to prevent the progression of electrical and mechanical damage. Care must also be taken for storage to prevent the adherence of dust or surface scratching of samples with decapped packages.

3.3.3 External Visual Inspection of the Package

Visual inspection of the external condition is important, and in many cases provides useful information for analysis when quality trouble occurs.

The entire package should be carefully observed using the naked eye to ascertain differences from good products, and then detailed observation should be made using a stereoscopic microscope. With the stereoscopic microscope, it is important to adjust the lighting in a variety of angles to obtain the best view of the observed location. If necessary, abnormal locations should also be searched for using an optical microscope with higher magnification (approximately 100 to 1000×). If further detailed observation is required, SEM is used to search for break surfaces, discoloration and migration, and SAT is used for internal analysis such as delamination and cracking. When elemental analysis is required and a sufficiently large number of samples is available, atomic absorption spectrometry or other methods are used. When taking samples of foreign matter from minute areas is difficult, electron probe micro analysis (EPMA) is used.

Key points for external visual inspection are as follows.

(1) Voids and pinholes

The mold resin normally used for semiconductor devices has low viscosity and is molded at low pressure, so residual air bubbles may cause voids and pinholes. (Void: air bubble inside the package, pinhole: air bubble on the package surface) When voids occur on element surfaces or over metal wiring, water may condense and corrode the wiring, causing problems with moisture resistance reliability.

In addition, pinholes are appearance and reliability defects, and cracking may originate at pinholes (and voids) during reflow. The generation of voids and pinholes is greatly influenced by the water content, viscosity and gap ratio (materials and mold structure) of the mold materials. These factors can be suppressed to a level which poses no problems for practical use by setting appropriate conditions.

(2) Package cracking

Cracking is caused by the penetration of moisture from outside the package. Cracking may be easily overlooked depending on the package structure and materials, so sufficient care must be taken for observation. Inspection using fluorescent penetrant fluid is effective for observing minute cracks.

(3) Mechanical damage to external pins

Damage modes differ depending on the pin shape, load, environment and other factors.

These modes include fatigue damage caused by repeat stress, shock damage caused by sudden stress, and creep damage caused by application of a constant stress over a long time. Wave-like patterns appearing on crack and break surfaces indicate that these are due to mechanical fatigue. For example, a dish-shaped or ratchet-shaped break surface indicates that there exists stress concentration at that point.

(4) Adherence of foreign matter

Foreign matter adhering to external pins is a cause of connection defects when mounting on a substrate.

This problem occurs when the handling or work environment in the manufacturing process or the storage environment is inappropriate. In addition, conductive foreign matter (such as whisker-like plating formations) occurring between external pins may cause short circuits between leads.

(5) Contamination

Contamination by remaining traces of water, oils, flux, and various spray liquids (such as insulation materials) may cause connection and/or leakage defects.

(6) Lead discoloration

To improve solderability and resistance to corrosion of the lead frames used in semiconductor devices, the external leads are normally solder-plated except for S-Pd PPF (Sony Specification palladium Pre-Plated lead Frame). Plating discoloration is caused by chemical reactions such as oxidation and sulfurization due to heating, flaws in the base material, incomplete pretreatment, and plating flaws, etc.

(7) Metal migration

When voltage is applied at high temperatures and high humidity, metallic ions inside the insulation material or at its surface migrate from the positive electrode to the negative electrode where they collect, are reduced and precipitate. This may ultimately lead to a short between the two electrodes. Inspection using a metallurgical microscope or EPMA is effective for observing these features.

(8) Stress corrosion cracking of leads

Stress corrosion cracking occurs when Cu-Zn alloys and other copper based alloys which are subject to tensile stress due to external stress or internal residual stress are exposed to ammonia, amines, high temperatures and humidity or other environmental factors. These conditions can be judged by inspecting cracking break surfaces and observing grain boundary conditions and other factors using SEM.

3.3.4 Evaluation of Electrical Characteristics

(1) Evaluation using a LSI tester

Test programs for design evaluation and analysis are used to evaluate the electrical characteristics of failure samples.

These results are then used to classify and analyze failure modes, infer failure mechanisms, and determine subsequent analysis methods.

Evaluation of electrical characteristics makes it possible to accurately understand failure mechanisms in detail from the failure circumstances, and effective analysis methods can be determined based on these results.

In addition, when evaluating memory LSI the detailed failure location can often be pinpointed on the chip, so detailed evaluation of the electrical characteristics is important.

(2) DC characteristics evaluation

This evaluation method investigates the DC characteristics of chips using a curve tracer, picoammeter and other equipment.

Pin damage, open connections, short circuits, DC characteristics deterioration and other problems can be detected.

The analysis sensitivity for minute deterioration and damage can be improved by comparing the characteristics with good chips to ascertain the difference.

(3) Mounting evaluation

This method mounts the sample on actual electronic equipment for evaluation.

This method is effective for reproducing and confirming failure modes when failure locations cannot be determined using methods (1) and (2) above. When the failure cannot be determined using methods (1) and (2) but is confirmed to occur during mounting evaluation, the failure may not have been reproduced because the failure circumstances could not be simulated, or the failure may have been caused by some problem with device operation.

3.3.5 Non-destructive Internal Analysis of Packages

Methods of analyzing the internal structure of a device without opening the package include radiography, ultrasonic examination, and hermeticity evaluation.

3.3.5.1 Radiography

Radiography allows observation of the wire bonding condition (wire loop condition, arch shape and arch height). In addition, the wetting performance of the silver paste between the chip and die pad, and the presence of voids in the molded resin can be inspected.

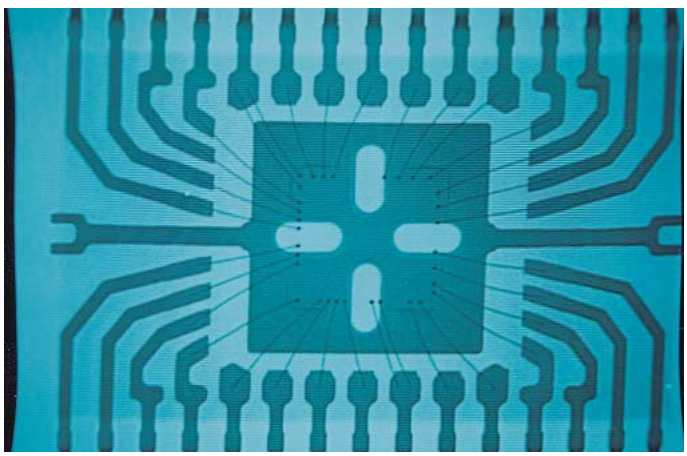


Photo 3-1 Radiography

3.3.5.2 Ultrasonic Analysis

Scanning acoustic tomographs (SAT) use ultrasonic waves (reflected waves) to enable non-destructive observation of the junction conditions at internal boundaries as shown in Fig. 3-2, and are used to evaluate solder heat resistance and other characteristics.

The SAT image is determined by the inherent acoustic impedance of each material at the junction boundary and the reflectivity R which depends on the material combination. When ultrasonic waves enter an area where the resin has been delaminated (air layer), the reflectivity is 100%, which provides a brighter picture than adhered portions. In addition, the reflected waveform phase is inverted at this time.

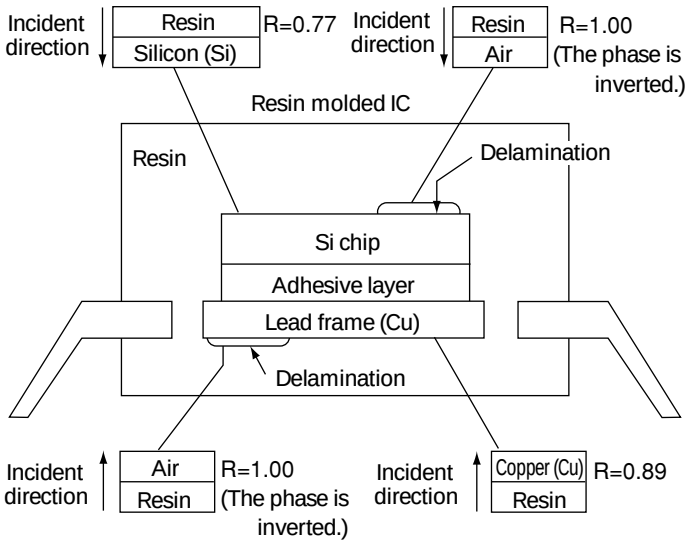


Fig. 3-2 Package Internal Junction Conditions and Reflection

Photo 3-2 shows an example of SAT analysis of a 28-pin SOP package.

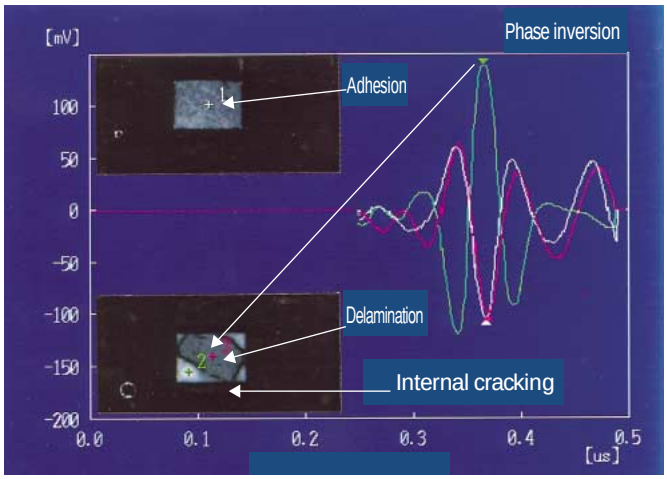


Photo 3-2 28-pin SOP Ultrasonic Analysis Diagram

Photo 3-3 shows a cross sectional SEM photo of a 28-pin SOP package.

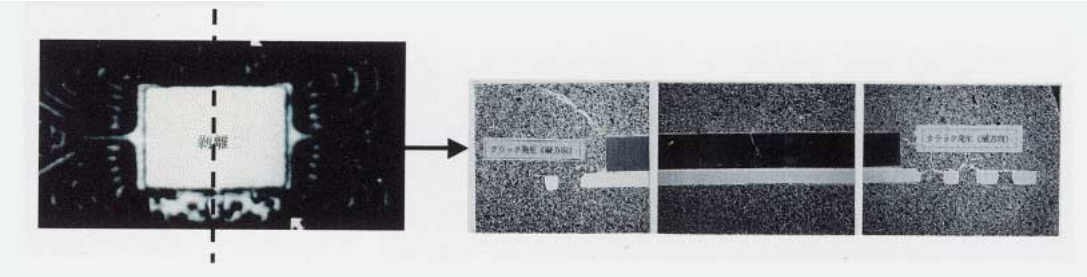


Photo 3-3 28-pin SOP Cross Sectional SEM Photo

The presence of delamination must be determined comprehensively by comparison with a reference sample in addition to the analysis image and reflected waveform (phase inversion).

As shown in Photo 3-2, internal cracking can also be checked by SAT analysis, but ultimately cutting and polishing of the cross section are necessary for the visual check.

3.3.5.3 Hermeticity Evaluation

Metal and ceramic type packages are hollow inside and sealed with nitrogen gas, and leakage must be limited to suppress the entry of moisture and impurities and corrosion of the aluminum pad. A leakage measurement method using helium is used to measure fine leaks.

3.3.6 Determining Failure Locations inside Chips

3.3.6.1 Description

When analyzing chip failures, the location of the failure inside the chip is first determined using failure locating technologies. Next, the form of the determined failure location is observed, and then composition analysis and other physical analysis are carried out to establish the cause of the failure.

Failure location uses the following methods.

The infrared radiation detection method is used to discover abnormal temperature distributions inside chips, the hot spot observation method is used to detect leaks using liquid crystals, and the photoemission method which detects feeble light emission is used to detect micro leaks, etc. Analysis of operating conditions includes the EBIC method which uses an electron microscope as a method of analyzing PN junction potentials, the OBIC method which uses a scanning laser microscope, and the voltage contrast method which analyzes wiring potentials using an EB tester.

These methods irradiate the chip surface with electron beams and detect light and other emissions from the chip surface, so the chip surface must be exposed while still in the package. Therefore, preparation such as decapping the package and removing the chip coating film is necessary.

3.3.6.2 Package Decapping Methods

Packages are decapped automatically using an acid decapsulator or manually by workers using tools. When using an acid decapsulator, decapping skill and experience are not required, and packages can be decapped easily even by unskilled workers. Photo 3-4 shows a 64-pin QFP package (chip size 3.6 × 3.6 mm) decapped using an acid decapsulator.

Photo 3-4 Package Decapping Example

There are a number of manual decapping methods using tools, and two examples are shown in Fig. 3-3 below. (a) shows the mold resin shaving method. Here, the resin over the chip is shaved with a grinder or drill, and the package is then immersed in a chemical solution to melt the resin. Dissolution is stopped when the chip becomes visible, and the package is then placed in an organic solvent and washed ultrasonically. This method immerses the entire package into the chemical solution, so the entire package surface melts. This method is used to decap DIP and other thick packages. (b) shows the acid resistant tape method.

Here, the package is covered with acid resistant tape, and the tape over the part to be melted is cut away. The package is then immersed in a chemical solution to melt the resin. Quartz is used to prevent lead bending. The acid resistant tape method melts only the target area, so packages can be decapped in an operable condition.

The acid resistant tape method is limited to QFP, SOP, BGA, CSP and other thin packages.

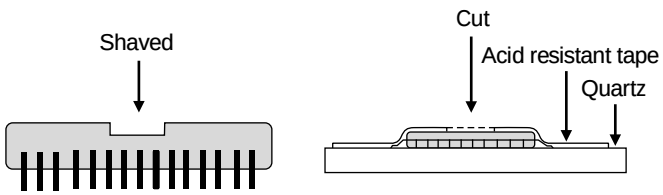


Fig. 3-3 Decapping Methods Using Tools

3.3.6.3 Fault Isolation

(1) Mechanical probing

This method contacts a fine metallic probe to the wiring inside the chip and measures the potential waveform of the internal wiring. This method has been used for quite some time, and it is the only method which can measure the absolute potential inside the chip.

In order to contact the metallic probe to the wiring, the wiring must be exposed to the chip surface. Therefore, the passivation film must generally be removed by plasma treatment.

To measure the signals in lower layer wiring, a hole is opened in the interlayer film using a focused ion beam (FIB), then a measurement pad is fabricated by depositing tungsten film and the probe is contacted to the wiring.

(2) Electron beam testing

This method irradiates a tightly focused electron beam to the chip surface and measures the potential distribution and voltage waveform in the internal wiring in the non-contact condition.

This method is non-contact, so high impedance measurement is possible and characteristics such as the waveform timing can be measured with high accuracy.

When an electron beam is irradiated to the chip surface, high energy secondary electrons are generated from the negative potential wiring and low energy secondary electrons are generated from the positive potential wiring. More secondary electrons are detected from the negative potential wiring than from the positive potential wiring, so the resulting contrast can be used to know the potential distribution over the wiring. (Photo 3-5) In addition, a voltage waveform can be obtained by fixing a pulse-converted electron beam at a single point on the wiring and detecting the potential information while shifting the timing at which the pulse beam is irradiated.

The information obtained from electron beam testing is waveforms and other logical information, so comparison with expected value information is necessary to determine the failure location. Therefore, methods such as comparing the potential distribution of good and defective chips or comparing actually measured waveforms with logical simulation waveforms are used to narrow down the failure location.

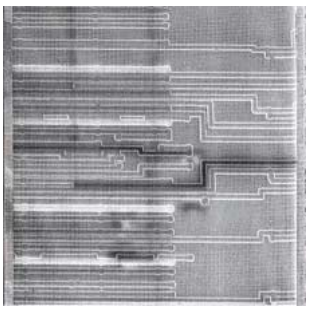


Photo 3-5 Potential Difference Analysis

(3) Photoemission analysis

This technique detects the feeble photoemissions produced by various types of failure on the chip surface using an emission microscope. Fig. 3-4 shows the photoemission analysis equipment configuration.

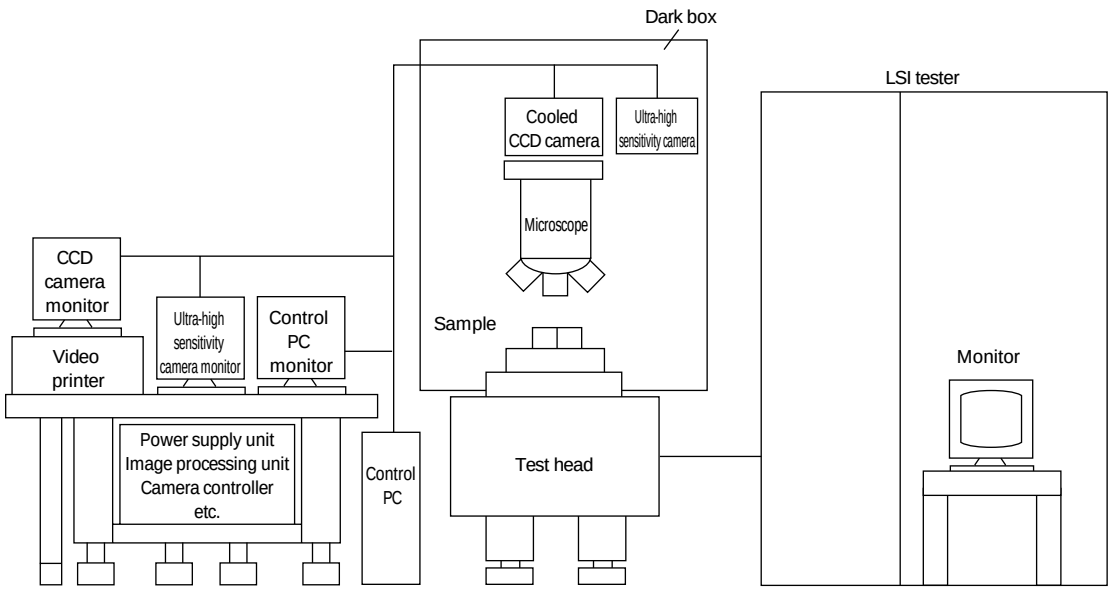


Fig. 3-4 Photoemission Analysis Equipment Configuration

The photoemission image and the reflected image (optical microscope image) are captured by the same high sensitivity camera, and the photoemission positions on the chip can be detected by combining these two images into a single composite image. (Photo 3-6(a))

When a leak current flows to the gate oxide film or a PN junction, a high electric field region is created and photoemission caused by the micro plasma phenomenon is observed.

Furthermore, failure locations can also be narrowed down indirectly by observing hot electron emission from MOS transistors caused by open wiring connections and short circuits. Photoemission analysis is mainly used for leak failures, but the causes of function failures resulting from micro leaks can also be determined by detecting photoemissions from chips operated on an LSI tester. (Photo 3-6(b), (c)) In addition, the detection of photoemissions from the chip surface has become difficult for microcomputers, ASIC and other chips with multilayer metallic wiring, so these chips are analyzed by detecting infrared transmitted from the rear surface of the chip through the silicon.

(a) Entire chip (b) Enlargement (block level) (c) Enlargement (cell level)

Photo 3-6 Detection of Micro Leaks Using Photoemission Analysis

(4) Thermal emission analysis

Leak and short defect locations which emit heat can be detected using a liquid crystal. When heat is applied to a liquid crystal, transition of the liquid crystal occurs, and this can be observed using a polarizing microscope.

There are two analysis methods. The first method pre-heats the LSI to a temperature where the crystal properties of liquid crystals change. The second method uses the process of forcibly causing a transition in the liquid crystal and then bringing the liquid crystal back below the transition point by a combination of natural and forced cooling.

(5) OBIC (optical beam induced current) analysis

When semiconductors are irradiated by an optical beam, the phenomenon of light absorption by the semiconductor produces an excitation current. This excitation current changes at failure locations, so failure locations can be determined by detecting these changes. This method is called OBIC.

This method irradiates a laser beam having a specific wavelength as the light, and views changes in the device current as a visible image or a so-called current map image. (Photo 3-7)

Examples of application to failure analysis are as follows.

1. Detection of leak current locations
   (PN junction leaks, gate oxide film leaks, etc.)

2. Detection of abnormal standby current locations
3. Detection of ESD breakdown locations
4. Evaluation of latch-up
5. Observation of the depletion layer

Note that the optical excitation current differs according to the failure conditions and mode, but this current is extremely small, so periodically flowing current should be canceled and only the OBIC current should be analyzed with high sensitivity.

Current equipment can support levels as low as several 10 pA.

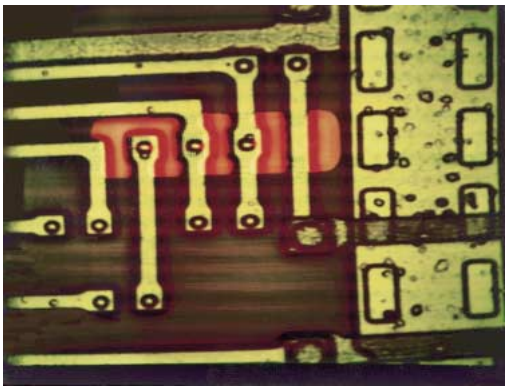


Photo 3-7 OBIC Analysis

3.3.7 Physical Analysis of Chips

Physical analysis of chips consists of observing the failure locations determined by the methods described thus far, and physically clarifying the cause of the failures.

Locations where the circuits comprising semiconductors have been damaged may be easily visible from the surface, but observation may be difficult when failures are located under other patterns. In these cases, the undesired patterns must be removed to facilitate observation.

Specific methods include removing patterns (exfoliation) from the upper surface layers to expose breakdown locations and causes, and exposing the cross section which contains the failure location. The appropriate method should be selected according to the results of electrical analysis, the exactness to which the location can be determined, and the results of surface observation from above the passivation film.

3.3.7.1 Exfoliation

This method removes the films in order from the passivation film, interlayer films, metal wiring and so on using methods appropriate to the film type. Care must be taken to apply as little damage as possible to the structure below the film to be removed, and to check and record the breakdown location exposure conditions at each stage.

Table 3-1 shows removal methods for various film types.

Table 3-1 Removal Methods for Various Film Types

Film type	Method	Chemicals and gases used
SiN	Dry etching	SF_6, N_2, O_2
	Wet etching	H_3PO_4
SiO_2	Dry etching	SF_6, N_2, O_2
	Wet etching	HF, CH_3COOH, SO-1 (HF, NH_4OH)
Al	Wet etching	HCl, H_2SO_4, H_2O_2
Ti/TiN/TiON	Wet etching	H_2SO_4, NH_4OH, H_2O_2
Poly Si	Wet etching	HF, HNO_3, CH_3COOH
	Ultrasonic washing	H_2O

3.3.7.2 Surface Observation (Optical Microscope, SEM)

In most cases, physical analysis starts from observation of the surface as this allows quick observation of a wide range. This method is used when exfoliating layers from the surface to expose failure locations.

Observation uses optical microscopes and scanning electrical microscopes (SEM).

In principle, optical microscopes use low magnification (up to approximately 2000×), but oxide films transmit light, so failure locations can sometimes be observed without exfoliation. In addition, interference colors are present depending on the thickness and refractive index of the transmitting film, so abnormalities during film forming can sometimes be detected by comparing the color with normal products.

SEM enable observation at magnifications of several ten to hundred thousand, and are indispensable for the physical analysis of semiconductors. Observed items include not only the external shape, but also conductivity and differences in formation from surrounding circuit elements. In addition, metal wiring which is floating electrically with respect to the silicon substrate is charged up and shines white, so contact defects and open connections can also sometimes be discovered.

3.3.7.3 Cross Sectional Observation (FIB, SEM)

Cross sectional observation is effective for determining the process in which foreign matter adhered and observing contact hole abnormalities. Methods used to expose the cross section include cutting, polishing, and focused ion beam (FIB). Observation normally uses SEM.

(1) Cleavage

This method splits the chip in the direction of the silicon crystals and observes the cross section. Depending on the observation target, slight etching may be performed using HF, H_2SO_4 or other etching agents to make contours easier to see. The observed location cannot be strictly determined, but this method is effective for observing repeated patterns and wide ranges.

(2) Polishing

Machining samples requires some time, but the cross sections at specific locations on chips can be observed more clearly than with FIB. First the chip is cut, then the piece containing the point to be observed is polished so that the cross section approaches the observation point. Polishing uses rough abrasives at first, and then switches to finer abrasive as the observation point is neared to prevent polishing mars, etc.

(3) FIB

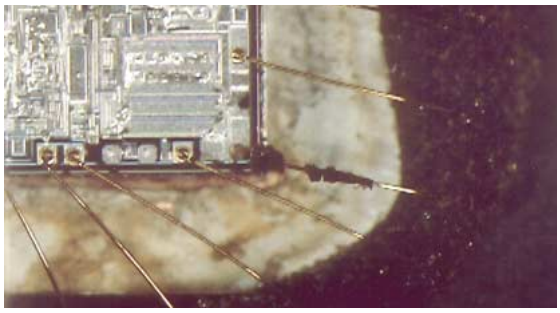
The chip surface is irradiated with a converged ion beam to etch the desired observation point on the chip and expose the cross section. The irradiated position can be determined while observing the image, so the cross section can be exposed with an accuracy of 1 µm or less.

3.3.7.4 Observation Points

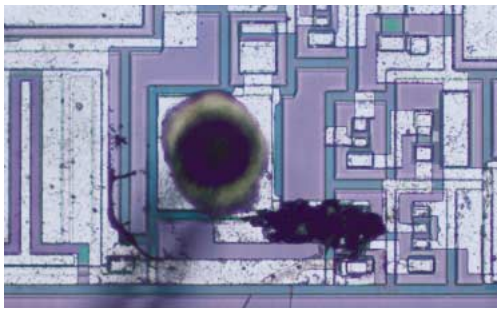
(1) Open connections, short circuits and leaks caused by excessive voltage and current

External surge voltages and currents may lead to open connections and short circuits. These failures mostly occur in the external input and output cells, but when surge voltages and currents cause latch-up, the aluminum wiring and gold wires used by internal cells may melt. (Photo 3-8)

Melting in the input and output cells can be easily confirmed by checking the electrical characteristics and observing from above the chip using a metallurgical microscope. However, internal cell melting requires careful observation with a metallurgical microscope, and polysilicon melting often occurs in the lower layers, so the upper layers must be exfoliated for observation.



(a) Open aluminum wiring connection inside a cell



(b) Open connection between the pad and aluminum wiring

Photo 3-8 Open Defects Caused by Excessive Voltage and Current

(2) Aluminum wiring corrosion

Moisture penetrating from outside the package, the formation of phosphoric acid, residual chlorine ions or other factors may cause aluminum corrosion resulting in open connections or short circuits between adjacent aluminum wiring. (Photo 2-11) Corroded aluminum wiring is often discolored, a condition which can easily be observed from above the passivation film using an optical microscope.

(3) Chip cracking (Photo 3-9)

Thermal stress may cause cracks in silicon chips, and these cracks have been confirmed to lead to electrical leaks between the power supply and GND in many cases.

Cracks may occur irregularly across the chip surface, or they may also occur along the grinding marks if grinding was insufficient or performed roughly during the rear surface grinding process. This failure mode can be easily discovered by observing the overall periphery of the chip using a metallurgical microscope. In addition, verification is also possible by removing the chip from the die pad and comparing the cracks with the grinding marks on the rear surface.

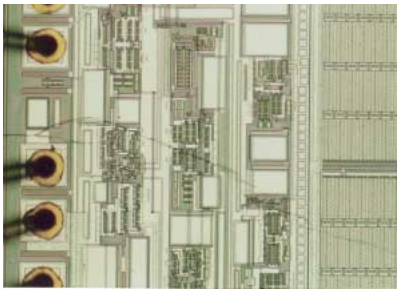


Photo 3-9 Chip Cracking

(4) Mask alignment offset

This is when the diffusion area, polysilicon, contact holes, aluminum wiring, and via holes are offset relative to the upper or lower adjacent layers, and can be detected by surface observation. However, information such as the machining dimensions of each circuit element, the positional relation as viewed from the cross section, and the shape observation results are necessary to determine the cause of the failure.

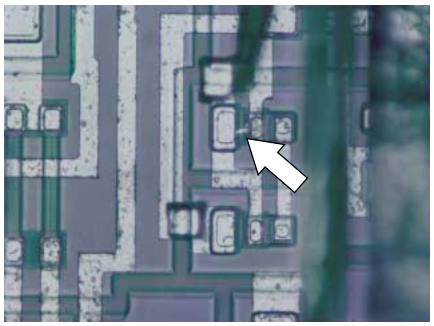
(5) Adherence of foreign matter

Foreign matter adhering within processes may cause slight deformations in the wiring or micro leaks. Continued use in this condition may lead to open connections or shorts due to electromigration. When the location of foreign matter is unclear, the surface layers must be exfoliated to allow observation, but when the location can be ascertained, the process in which the foreign matter adhered can be easily determined by observing the cross section with FIB, etc. In addition, the results of analyzing the shape and components of foreign matter also provide useful information for determining the cause.

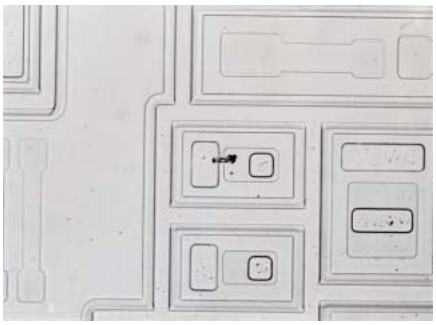
(6) Electrostatic breakdown (ESD)

The gate oxide film in current MOS devices is extremely thin, and these devices have low insulation strength. Therefore, when static electricity in excess of the IC endurance voltage is applied, breakdown results, and this phenomenon may manifest as short circuiting of the input and output pins. The breakdown mechanisms include aluminum wiring or polysilicon resistance burning, transistor gate oxide film damage, or junction damage, etc. Burning can be easily analyzed with a metallurgical microscope, but pinholes in the gate

oxide film require observation using SEM or other equipment. (Photo 3-10-(a), -(b))



(a) Aluminum wiring present



(b) Aluminum wiring removed

Photo 3-10 ESD Breakdown

(7) Electromigration and stress migration

Currents, temperature or mechanical stress within the manufacturing process or during use may cause a portion of the aluminum wiring surface to rise (hillock) or the wiring to crack (voids). Hillocks may cause short circuits with adjacent wiring to the side or above, or they may cause the passivation film to weaken and fail or the wiring to corrode.

Voids are caused by current-induced electromigration during use, and may result in increased resistance or open connections. Surface and cross sectional observation are used according to the analysis conditions.

3.3.8 Analysis and Structural Analysis Technologies

With increased LSI integration, cells are being miniaturized, and gate oxide films and capacitor insulating films are becoming thinner. Furthermore, multiple layers, trenches and other three-dimensional structures are making processes more complex and reducing manufacturing process margins. As a result, problems rooted in processes occur more easily, and make it difficult to ensure quality and reliability. Thus, analysis technologies are becoming more and more important in order to analyze process-related problems. The Sony Semiconductor Network Company has assembled the analysis technologies shown in Table 3-2 to assist in solving process-related problems.

Table 3-2 presents an overview of various analysis methods.

Table 3-2 List of Analysis Methods 1/3

	Analysis method	Measurement method	Obtained information	Measurement limits	Example measurement targets
Elemental Analysis	Ion Chromatography (IC)	Sample ion electrical conductivity	Ion presence and concentration in aqueous solutions	ppb level (ng/ml) to ppt level (pg/ml)	Inorganic anions and cations, organic ions
	Inductively Coupled Plasma Atomic Emission Spectroscopy (ICP-AES)	Light quantity emitted when atoms fall from an excited level to the normal level	Atomic concentration in solutions	ppb (ng/ml)～ ppm (μg/ml)	Inorganic materials, acids, alkali, organic solvents
	Atomic Absorption Spectrometry (AA/FAA)	Light quantity absorbed by atoms	Metallic atom concentration in solutions	ppt(pg/ml) ppm (μg/ml)	Semiconductor materials, acids, alkali, organic solvents
	Inductively Coupled Plasma Mass Spectroscopy (ICP-MS)	Introduction of atomized plasma samples to a mass spectrometer	Atomic concentration in solutions and qualitative analysis of elements in solids	ppg (fg/ml)～ ppt (pg/ml)	Inorganic materials, acids, alkalis, organic solvents, semiconductor materials
Chemical Structure Analysis	Fourier Transformation Infrared Spectroscopy (FT-IR)	Measurement of infrared absorption by substances at different wavelengths	Organic substance qualities and thin film quality	As small as several 10 μm in diameter	Organic materials, functional groups on semiconductor surfaces, etc.
	Visible Ultraviolet Spectroscopy (UV-VIS)	Measurement of ultraviolet or visible light transmittance through substances	Light transmittance of substances	0～2Abs	Glass, organic materials, etc.
	Raman Spectroscopy	Measurement of inelastic scattering of light due to lattice and molecular vibration	Measurement of inelastic scattering of light due to lattice or molecular vibration	Area resolution as small as 8 μm	Semiconductor materials (Si, GaAs, etc.), organic and inorganic materials
	Gas Chromatography/ Infrared Spectroscopy/ Mass Spectroscopy (GC/IR/MS)	Measurement of substances separated by gas-liquid division using an infrared spectrophotometer and a mass spectrometer	Determination and quantitative analysis of the structure of gasified organic substances	ng level	Organic mixtures (solids, liquids, gases)
	Gas Chromatography/ Atomic Emission Detector (GC/AED)	Elemental analysis of substances separated by gas-liquid division using photoemission analysis	Elemental analysis of organic substances	ng level or less (depends on the element)	Organic mixtures

Table 3-2 List of Analysis Methods 2/3

	Analysis method	Measurement method	Obtained information	Measurement limits	Example measurement targets
Chemical Structure Analysis	Gas Chromatography/ Hydrogen Flame Ionization Detector (GC/FID)	Ionization of substances separated by gas-liquid division in a hydrogen flame and detection of the resulting current	Composition ratio of organic mixtures	10～100pg	Organic mixtures
	High Performance Liquid Chromatography (HPLC)	Measurement of substances by solid-liquid division using a pump	Separation of organic substances	Depends on the substance	Organic mixtures
	Fourier-Transform Nuclear Magnetic Resonance (NMR)	Electromagnetic wave absorption in a magnetic field by substances having a magnetic moment	Detailed structure, composition and relaxation time of substances having complex structures	Minimum weight ^{1}H nucleus: 0.1 mg, ^{13}C nucleus: 5 mg	Organic compounds, polymers, biological materials, catalysts
	High Resolution Mass Spectroscopy (HRMS)	Volatilized ionization	Molecular weight and molecular composition formula	Molecular weight: approximately 5,000	Organic materials
Thermal Analysis and Thermal Physical Properties	Thermal Analysis (TG, DSC, TMA) (TG-DTA)	Measurement of changes in mass, heat input and output, and expansion of substances while varying the temperature	Evaluation of thermal stability from the crystalline structure transmutation temperature and the thermal decomposition temperature of substances	Several mg of sample are required	Glass, polymer materials
	Thermal Desorption - Quadrupole Mass Spectroscopy (TD-QMS)	Detection of gas released from samples while increasing the temperature	Gas adsorption and crystal water desorption from substrates	Depends on the substance	Ceramics, metallic materials, etc.
Morphology Observation and Micro Analysis	Scanning Electron Microscopy (SEM)	Scanning a primary electron beam and observing the two-dimensional distribution of the secondary electron or reflected electron intensity	Sample surface shape, sample composition distribution image, and sample morphology image	Resolution: 0.7 to 0.3 nm	Solids, powders
	Electron Probe X-ray Micro Analysis (EPMA)	Measurement of the wavelength (energy) and intensity of characteristic X-rays generated by electron beam irradiation	Sample composition and in-plane distribution (mapping image)	0.1% ^{5}B to ^{92}U Resolution: 5 to 10 eV (WDX) or 150 eV (EDX)	Solids, powders
	Atomic Force Microscopy (AFM)	Measurement of the atomic force between the sample and probe	nm-order surface morphology (even for insulating objects)	0.01 nm (vertical), 2 to 3 nm (horizontal)	Semiconductor substrates, LSI interlayer films, organic thin films
	Surface Shape Measurement	Measurement of the surface shape with a contact probe	Solid surface steps and roughness	0.03 nm to 0.5 nm (vertical)	Evaporated thin film thickness, IC surface type oxide film etching patterns

	Analysis method	Measurement method	Obtained information	Measurement limits	Example measurement targets
Surface Analysis	Auger Electron Spectroscopy (AES)	Measurement of the energy and intensity of Auger electrons generated by electron beam irradiation	Analysis of the composition and elements of several nm and thinner films in the depth direction	0.1%	Laser diode semiconductor samples, multilayer recording medium surface and interface analysis, composition changes
	X-ray Photoelectron Spectroscopy (XPS)	Measurement of the kinetic energy of photoelectrons emitted from the surface of solids by X-ray irradiation	Elemental composition and chemical bonding states to a depth several nm below the surface and analysis of these characteristics in the depth direction	0.1at%	Semiconductor, magnetic object and organic substance surfaces, various device surfaces
	Secondary Ion Mass Spectroscopy (SIMS)	Measurement of secondary ions released when solid samples are irradiated with ions	Mass spectrum, trace impurity density and distribution in the depth direction, and element distribution in the depth direction	10^{14}～10^{16} atoms/cm^3	Dopant profile in the depth direction inside semiconductor samples, elemental analysis of metal-semiconductor interfaces
Structural Analysis	Transmission Electron Microscopy (TEM)	Microscopy which enlarges images with an electromagnetic lens using the diffraction phenomenon of transmitted electrons	Crystalline structure, atomic arrangement, crystal defects, crystal orientation, magnetic domain structure, composition analysis and condition analysis	Point resolution: ≥ 0.19 nm Sample thickness: several nm to 300 nm or less	Semiconductor order structure, hetero-interfaces, ion implantation induced crystal defects, magnetic thin films, oxide superconductors
	Reflection High Energy Electron Diffraction (RHEED)	Irradiation of electrons along the surface and observing the diffraction map created by electrons diffracted by the surface	Crystal structure, orientation and damage at the top surface	Surface depth: several nm or less, measurement area beam diameter: 0.1 mm × sample size	Semiconductors, metallic thin films, magnetic materials (thin film bulk)
	X-ray Diffraction	Measurement of the diffraction angle and diffraction intensity of X-rays irradiated at samples	Lattice plane interval, crystalline structure, crystal properties, crystal orientation, residual stress (machining distortion)	10^{-3} at △d/d	Powders, polycrystalline films, epitaxial films, machined surfaces, adhering matter, magnetic films
	Pole figure Measurement	Tilting samples in various directions to investigate the X-ray diffraction intensity and crystal surface orientation	Distribution of crystal grain orientation in polycrystalline samples	Angular resolution > 2 °	Alloy films for magnetic heads, thin film magnetic mediums, coated tape, LSI wiring films
	X-ray Topography	Microscopy by irradiating X-rays and using the diffraction phenomenon to record imperfections inside crystals or at the crystal surfaces on a dry plate	Distribution of lattice defects (dislocations, precipitates, etc.) inside crystals, changes in lattice constants, lattice plane tilting	Resolution: several nm △d/d = 10^{-5} to 10^{-7}, 0.1 s	Semiconductor mono-crystals (Si, GaAs, etc.), magnetic crystals, optical crystals
	Laue Camera Method	Observation of white X-rays from mono-crystals and observation of the pattern symmetry	Crystal orientation	Angular resolution: 3 ° or less	Ferrite heads, optical crystals, semiconductors, metallic mono-crystals

3.3.8.1 Analysis of Metallic Impurities on Wafer Surfaces

Silicon wafer surface cleaning technology is essential for the manufacture of semiconductors, and contamination by metallic impurities is known to cause drops in the oxide film endurance voltage, increased leak current and other problems. Therefore, technology is needed to analyze impurity amounts of 10^8 to 10^9 atoms/cm^2 on wafer surfaces with high sensitivity.

In terms of chemical analysis methods, high sensitivity analysis was first made possible with the development of gaseous phase breakdown and atomic absorption photometry technologies, and improvements have since been made to the recovery method, which is where matters now stand. The recovery method distills hydrofluoric acid once and then takes metallic impurities into this highly pure hydrofluoric acid.

However, the purity of hydrofluoric acid has been improved to a level where there are presently no problems with its direct use. Therefore, the Sony Semiconductor Network Company has developed original contaminant metal dissolution and recovery technology called the indicator rod induction method. This method uses a small amount of highly pure hydrofluoric acid directly without distillation to allow the easy recovery of surface impurities. Fig. 3-5 shows an outline drawing of this technology.

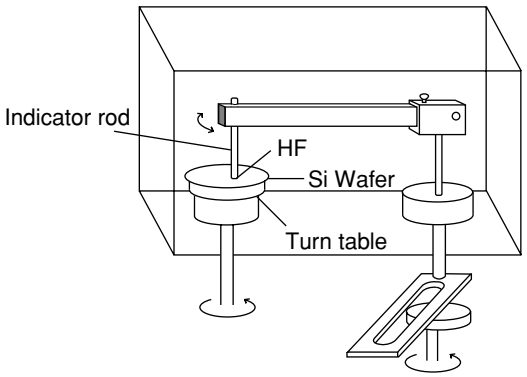


Fig. 3-5 Indicator Rod Induction Method Outline Drawing

The contaminant metal dissolution and recovery method first places a silicon wafer on a turntable, and then positions a 10 mm diameter indicator rod over the wafer with a gap of several millimeters. When 100 to 200 µl of highly pure hydrofluoric acid enters this gap, the surface tension keeps it within the gap and the wafer is rotated in this condition. On the other hand, the indicator rod has a mechanism which moves it back and forth over the wafer, and this moves the hydrofluoric acid evenly over the wafer in a spiral, making it possible to dissolve and absorb metallic impurities together with the natural surface oxide films into the hydrofluoric acid.

This simple recovery technology is combined with a high sensitivity atomic absorption photometer which uses a high luminance lamp to carry out analysis at the 10^8 atoms/cm^2 level and perform process line management.

An example of 9-element analysis performed after recovering the metallic contaminants from the surface of a washed 8-inch wafer using 200 µl of hydrochloric acid is shown below. Trace amounts of Na and K were detected, but all other elements were below the 10^8 atoms/cm^2 level detection limit.

Analysis of metallic impurities on the surface of a washed wafer ($\times 10^{10}$ atoms/cm^2)

Cr	Cu	Fe	K	Mg	Mn	Na	Ni	Zn
<0.04	<0.06	<0.03	0.16	<0.04	<0.01	0.38	<0.07	<0.05

CHAPTER 4 - RELIABILITY TESTS AND RELIABILITY PREDICTION

4

CHAPTER 4 - RELIABILITY TESTS AND RELIABILITY PREDICTION

4.1 Approach Toward Reliability

With recent advances in the systematization, functions and performance of equipment, the social impact and damages produced by failures are increasing, and high reliability has come to be demanded of equipment. This means that even higher reliability is demanded of the individual components which comprise equipment. Large quantities of semiconductors are used in a single piece of equipment, and these semiconductors often handle the main functions of that equipment, so high reliability is extremely important.

Semiconductors themselves are also becoming more miniaturized and highly integrated, with larger-scale circuit configurations. In addition, as semiconductor functions and performance advance and evolve into system LSIs, ensuring semiconductor reliability has become a vital matter.

The failure rate is often used as a general index for representing semiconductor reliability.

Semiconductor failure rates have been said to trend as shown in Fig. 4-1. This graph shape resembles a bathtub, so it is called a bathtub curve. In addition, failures have been classified into the three regions of initial failures, random failures and wear-out failures according to the time of occurrence.

Initial failures:

These are failures which occur at a relatively early time after the start of use.

These failures are characterized by a decrease in the failure rate over time.

The main causes of initial failures are manufacturing or material defects.

Random failures:

These failures are said to occur at a fairly constant failure rate after the initial failure period until wear-out failures occur.

With the exception of software errors described hereafter, intrinsic random failures are often thought not to exist.

Wear-out failures:

These are failures caused by wear and fatigue, and occur due to the physical limits of the materials which comprise semiconductor devices.

The failure rate increases with time, and these failures are used to determine the life.

However, the thinking that intrinsic random failures do not exist is changing recently.

That is to say, intrinsically only initial and wear-out failures exist as shown in Fig. 4-2, and the period between the two is comprised of the fringes of each failure distribution. This approach states that the failure rate during this intermediate period can be reduced by carrying out improvements for initial and wear-out failure factors.

The Sony Semiconductor Network Company also places emphasis on initial and wear-out failures in semiconductor reliability.

Initial failure rate levels are confirmed during development and design, and screening conditions are set as necessary to prevent defective products from escaping to the market.

In addition, semiconductor products are checked using accelerated tests to ensure that they have sufficient life so that wear-out failures do not occur during the normal usage period.

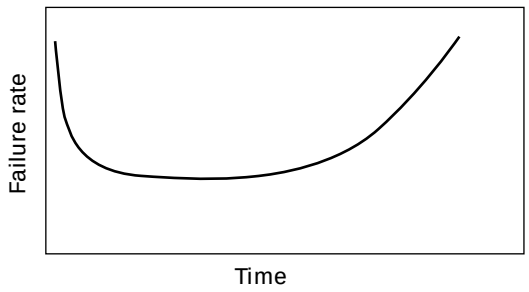


Fig. 4-1 Conventional Bathtub Curve

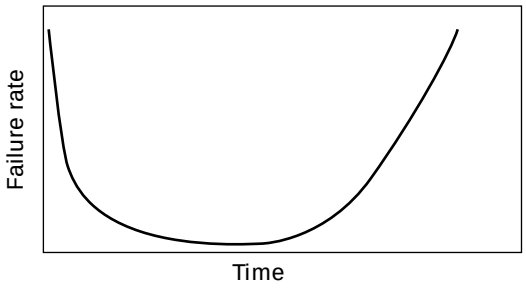


Fig. 4-2 Bathtub Curve Excluding Random Failures

4.2 What are Reliability Tests

4.2.1 Reliability Test Significance and Purpose

As defined under JIS Z 8115 (Reliability Terminology), “Reliability Test” is the general term for reliability determination tests and reliability compliance tests. In other words, reliability characteristics values (failure rate, reliability, average life, MTTF, etc.), which are scales representing the time-dependent quality of products, are estimated and verified statistically from the test data. These tests also play an important role in improving reliability by analyzing failures which occur during tests and clarifying these failure mechanisms. Reliability tests provide the greatest effects when statistics and failure physics function reciprocally.

Specific purposes of reliability tests are as follows.

(1) Product reliability assurance
(2) Evaluating new designs, components, processes and materials
(3) Investigating test methods
(4) Discovering problems with safety
(5) Accident countermeasures
(6) Determining failure distributions
(7) Collecting reliability data
(8) Reliability control

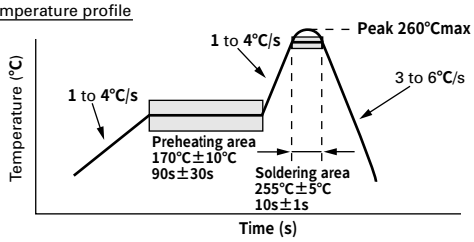
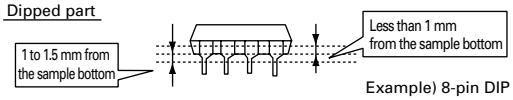
In addition, reliability tests are classified under various names according to the test format, purpose, method of applying stress, and other factors.

4.2.2 Reliability Test Methods

Reliability test items, conditions and other factors are determined based on customer needs for reliability, by clarifying the environmental and time conditions under which devices will be used and the failure definitions. It is also important to select test methods which are as standardized as possible in consideration of test reproducibility, cost effectiveness, data compatibility and other factors. The Sony Semiconductor Network Company has carried out tests centering on the JIS and MIL standards, and also performs reliability tests which support EIAJ, JEDEC and other standards as well.

Table 4-1 shows examples of standard reliability test items and methods used by the Sony Semiconductor Network Company.

Table 4-1 List of Standard Reliability Tests (IC) 1/5

<table>
<tr><th>Test item</th><th>Conditions</th><th>Failure criteria</th><th>Standard time</th></tr>
<tr><td>Soldering heat resistance [SMD]</td><td>Method 1: Solder bath dipping method at 260 ± 2°C
Method 2: Infrared reflow heating method at 260°Cmax
• Perform baking and moisture absorption at each of the conditions prescribed in the individual standards before heating.
The time from baking to moisture absorption shall be 5 minutes or less, and the time from moisture absorption to reflow or solder dipping shall be 2 hours or less.
• In method 1, solder dip the entire sample one time.
• The dipping time for method 1 shall be 10 ± 1 s.
• In method 1, perform flux dipping before solder dipping. (using rosin-based active flux)
• In method 2, heating shall be performed three times as standard based on the reflow temperature profile prescribed in the individual standards.
[Baking → moisture absorption → heating → heating → heating]
• In method 2, place the sample on a dedicated ceramic holder for heating.
Temperature profile
 
</td><td>Significant delamination shall not be confirmed through scanning acoustic tomography.
External and internal cracking shall not be confirmed through external visual inspection and cross section polishing inspection.
Failures shall not occur in continued reliability tests.</td><td></td></tr>
<tr><td>Soldering heat resistance [non-SMD]</td><td>Solder dip the prescribed part of the sample according to any one of the following methods.
<table><tr><th></th><th>Solder temperature [°C]</th><th>Dipping time [s]</th></tr><tr><td rowspan="2">Lead dipping only</td><td>260 ± 2°C</td><td>10 ± 1</td></tr><tr><td>350 ± 10°C</td><td>3.5 ± 0.5 ∗</td></tr><tr><td>Dipping to package bottom</td><td>260 ± 2°C</td><td>10 ± 1</td></tr></table>Dipped part
 

Example) 8-pin DIP
• The soldering iron may directly contact the sample pins. (∗)
• Dip the sample in rosin-based flux (active) before solder dipping.
• There is no particular need for moisturizing.</td><td>The electrical characteristics prescribed in the individual specifications shall be satisfied.</td><td></td></tr>
</table>

Table 4-1 List of Standard Reliability Tests (IC) 2/5

Test item	Conditions	Failure criteria	Standard time
High temperature bias (HTB)	Set the sample to the prescribed operating status under the following high temperatures. [Ambient temperature] A : 150 ± 5℃ B : 125 ± 5℃ • High temperature operation circuits (figure) shall be prescribed individually. • The ambient temperature shall be prescribed separately when the junction temperature (Tj) exceeds the rated value. • The preconditions shall be prescribed individually when necessary.	The electrical characteristics prescribed in the individual specifications shall be satisfied.	1000h
Low temperature bias (LTB)	Set the sample to the prescribed operating status under the following low temperature. [Ambient temperature] –65 ± 5℃ • Low temperature operation circuits (figure) shall be prescribed individually. • The preconditions shall be prescribed individually when necessary.	The electrical characteristics prescribed in the individual specifications shall be satisfied.	1000h
Temperature humidity bias (THB)	After performing the soldering heat resistance test as the preconditions, continue and supply power to the sample under the following high temperature and high humidity. Temperature [℃] | 85 ± 3 Humidity [%RH] | 85 ± 5 • The power-on (bias) circuits (figure) shall be prescribed individually. • Select intermittent power-on (1 h: ON/3 h: OFF) or continuous power-on according to the amount of heat generated by the sample.	The electrical characteristics prescribed in the individual specifications shall be satisfied.	1000h
Pressure Cooker Test (PCT)	After performing the soldering heat resistance test as the preconditions, continue and expose the sample to the following high temperature, high humidity and high pressure. Temperature [℃] | 121 ± 3 Humidity [%RH] | 100^{+0}_{-3} Vapor pressure [Pa] | $2.03 \times 10^5 \pm 10\%$	The electrical characteristics prescribed in the individual specifications shall be satisfied.	96h
Highly-accelerated temperature and humidity stress test (HAST)	After performing the soldering heat resistance test as the preconditions, continue and supply power to the sample under the following high temperature, high humidity and high pressure. Temperature [℃] | 130 ± 5 Humidity [%RH] | 85 ± 5 Vapor pressure [Pa] | $2.3 \times 10^5 \pm 10\%$ • The power-on (bias) circuits (figure) shall be prescribed individually.	The electrical characteristics prescribed in the individual specifications shall be satisfied.	

4

Table 4-1 List of Standard Reliability Tests (IC) 3/5

<table>
<tr><th>Test item</th><th>Conditions</th><th>Failure criteria</th><th>Standard time</th></tr>
<tr><td>Thermal shock (TS)</td><td>After performing the soldering heat resistance test as the preconditions, continue and perform this test.
Repeatedly subject the sample to sudden temperature changes in the liquid phase as shown in the table below.
<table><tr><td>Order</td><td>1</td><td>2</td></tr><tr><td></td><td>–65 ± 5°C</td><td>150 ± 5°C</td></tr><tr><td>Time [min]</td><td>5</td><td>5</td></tr></table>• Start from room temperature to the low temperature side.
• The temperature transition time shall be 10 s or less.
• The medium shall be Perfluoropolyether (GALDEN®).
[Electronics test grade D02 TS]</td><td>The electrical characteristics prescribed in the individual specifications shall be satisfied.</td><td>100 cycles</td></tr>
<tr><td rowspan="3">Temperature cycle (TC)</td><td>After performing the soldering heat resistance test as the preconditions, continue and perform this test.
Repeatedly subject the sample to sudden temperature changes in the gaseous phase as shown in the table below.
1) Plastic molded packages
<table><tr><td>Order</td><td>1</td><td>2</td><td>3</td><td>4</td></tr><tr><td></td><td>–65 ± 5°C</td><td>Room temperature</td><td>150 ± 5°C</td><td>Room temperature</td></tr><tr><td>Time [min]</td><td>30</td><td>5^{+0}_{-1}</td><td>30</td><td>5^{+0}_{-1}</td></tr></table>• Room temperature here indicates 25 ± 15 °C.</td><td>The electrical characteristics prescribed in the individual specifications shall be satisfied.</td><td>100 cycles</td></tr>
<tr><td>2) Flip chips and chip size packages (CSP)
<table><tr><td>Order</td><td>1</td><td>2</td></tr><tr><td></td><td>–25 ± 5°C</td><td>125 ± 5°C</td></tr><tr><td>Time [min]</td><td>10</td><td>10</td></tr></table>Note) For flip chips and CSP, the prescribed temperature shall be the sample surface temperature (T_s). For other conditions, the prescribed temperature shall be the temperature inside the test tank near the blow-off opening (T_a).</td><td>The electrical characteristics prescribed in the individual specifications shall be satisfied.</td><td></td></tr>
<tr><td>3) Ball grid arrays (BGA)
<table><tr><td>Order</td><td>1</td><td>2</td></tr><tr><td></td><td>0 ± 3°C</td><td>125 ± 5°C</td></tr><tr><td>Time [min]</td><td>15</td><td>15</td></tr></table></td><td>The electrical characteristics prescribed in the individual specifications shall be satisfied.</td><td></td></tr>
</table>

Table 4-1 List of Standard Reliability Tests (IC)

Test item	Conditions	Failure criteria	Standard time
Lead strength	1) Tensile strength Apply the prescribed tensile force in the pin lead-out axial direction for 10 ± 1 s. • This test does not apply to packages with J-shaped leads or lead-less packages. • The load value shall be prescribed separately according to the pin cross-sectional area and wire diameter.	There shall be no pin severance, breakage or other mechanical damage.	
	2) Bending strength Hold the sample so that the pin lead-out axis is vertical, and attach the prescribed load to the tip of the pin. Rotate the sample 90° and then return it to the original position over a period of 2 to 3 s. Count this as one time. Next, rotate the sample at the same speed so that the lead pin is facing 90° in the opposite direction (in the same direction for flat pins), and then return it to the original position. Count this as the second time. • The load value shall be prescribed separately according to the pin cross-sectional area and wire diameter. • This test shall be performed two times. • The bending test shall not apply to SMD. • The twisting strength test is not prescribed.	There shall be no pin severance, breakage or other mechanical damage.	
Solderability	Dip the sample pins into a solder bath and visually judge (up to 30 × magnification) the degree of solder adhesion to the judgment portion. Solder plated → S-Pd PPF* Solder temperature → Sn/Pb : 230°C for 3 s; Sn/Ag/Cu: 245°C for 3 s Dipping time → 3 ± 0.5 Preconditions → 105°C100%RH 4h • The valid judgment portion shall be prescribed individually for each pin shape. *Sony specification palladium PPF	95% or more of the judgment portion shall be smoothly covered with solder, and pinholes, voids and other defects shall not be clustered in a single location or exceed 5% of the entire judgment area.	
Electrostatic strength	1) Machine Model (C = 200 pF, R = 0 Ω) • The number of applications shall be 1 time each, and the discharge current waveform shall be prescribed separately.	According to the individual specifications.	
	2) Human Body Model (C = 100 pF, R = 1.5 kΩ) • The number of applications shall be 3 times. • The discharge current waveform shall be prescribed separately.	According to the individual specifications.	
	3) Charged Device Model Maintain the potential of all the sample pins at the test voltage value via resistors, then contact the pin to be tested to a discharging metal object to discharge the pin. Carry out this procedure for each test pin. • All sample pins shall be tested. • The number of discharges shall be one time per test pin. • The discharge current waveform shall be prescribed separately.	According to the individual specifications.	

Table 4-1 List of Standard Reliability Tests (IC) 5/5

Test item	Conditions	Failure criteria	Standard time
Latch-up	1) Pulse current injection method Apply the supply voltage to the sample, fix the input pins to high or low, leave the output pins open, and then apply the prescribed constant current pulse to the test pin. Measure the supply current fluctuation at this time to determine whether latch-up has occurred. • The trigger pulse current waveform shall be prescribed separately. • The latch-up failure criteria current value shall be prescribed individually. • The tested pins shall be all pins other than power supply, GND and NC pins. • The trigger pulse shall be applied one time per test current value.	According to the individual specifications.	
	2) Power supply overvoltage method Apply the supply voltage to the sample, fix the input pins to high or low, leave the output pins open, and then raise the supply voltage value to the trigger pulse voltage value. Measure the supply current fluctuation at this time to determine whether latch-up has occurred. • The trigger pulse shall be applied one time. • The latch-up failure criteria current value shall be prescribed individually. • The trigger pulse voltage waveform shall be prescribed separately.	According to the individual specifications.	

4.2.3 Failure Criteria

When attempting to handle reliability characteristics values in a quantitative manner, it is important to clearly prescribe the operating environment and time-dependent conditions and the failure mode.

Conditions such as complete function failure or loss of important functions are generally easily clarified, but quantitative standards must also be set for drops in output, function deterioration and other failures occurring as gradual changes over time. In addition, failure criteria must take into account possible differences due to product users and customers.

The Sony Semiconductor Network Company states that in principle, electrical characteristics should be within the basic standard value range prescribed individually in the specifications for each product.

In this case, appropriate margins are set in the standard values themselves, so these do not indicate limit values at which products will absolutely fail as soon as these values are deviated from during actual use. In addition to standard values, there are also criteria which focus on the rate of change from the initial value. However, both types of criteria are set to detect changes and deterioration trends at an early stage, and to increase test efficiency. Table 4-2 shows example failure criteria for variable capacity diodes which are discrete semiconductors.

Table 4-2 Example Failure Criteria

Item	Measurement conditions	Specification	Failure criteria
I_R (Leak current)	V_R = 28V	10 nA or less	USL×2 (Upper limit)
V_F (Forward voltage)	I_F = 10mA	———	IVD×1.30
V_R (Reverse voltage)	I_R = 500 A	30 V or more	|IVD|×1.20

USL: Upper Specification Limit IVD: Initial value

4.3 Accelerated Life Tests

4.3.1 Purpose of Accelerated Life Tests

Innovations in semiconductor process technology are advancing at a blinding pace in recent years. Furthermore, given recent demands for shorter product development times, product reliability has been placed in the same situation as product development, and reliability characteristics must also be understood in a short time.

Based on these circumstances, accelerated life tests are methods for understanding reliability with the minimum sample size and the shortest test time. The JIS standard defines “accelerated tests” as “tests carried out under conditions more severe than standard conditions for the purpose of shortening the test time.”

Conducting tests under these severe conditions makes it possible to predict market failure rates in a short time using few samples, thus reducing both the time and cost required to confirm reliability.

4.3.2 Acceleration by Temperature

Semiconductor life is extremely sensitive to temperature, so life acceleration by temperature is almost always used as an accelerated test.

This temperature stress-based reaction was standardized by Arrhenius, and the Arrhenius model is widely used to predict semiconductor product life.

This Arrhenius model formula is expressed as follows.

$$\tau = A \cdot \exp\left(\frac{Ea}{kT}\right)$$

Where,
τ : Life
Ea : Activation energy (eV)
T : Absolute temperature (K)
A : Constant
k : Boltzmann’s constant

The above formula shows that semiconductor life depends on the temperature to which the semiconductor is exposed. Accelerated tests which utilize this characteristic are called temperature acceleration tests.

However, some failures such as those caused by hot carrier effects (the phenomenon where high energy carriers generated by electric fields are captured by the gate oxide film) may have negative activation energy values. When accelerating these types of failures, the test effectiveness increases as the test temperature is reduced.

4.3.3 Acceleration by Temperature and Humidity

LSI are tested under high temperature and high humidity environments to understand semiconductor life when exposed to high temperature and high humidity.

The high temperature and high humidity bias test, pressure cooker test, highly-accelerated temperature and humidity stress test (HAST), etc. are generally used as accelerated tests for humidity.

Humidity is rarely applied as the sole accelerating factor to confirm moisture resistance, and instead a combination of temperature and humidity stress is generally applied. This is done to promote the reaction to humidity (water), and leads to increased acceleration of the humidity life.

The general formula for humidity-related life is expressed as follows.

$$\tau = A \cdot P_{H_2O}^{-n}$$

Where,
τ : Life A, n : Constants

There is still no standardized formula for humidity-related life, and each manufacturer evaluates accelerated life using their own characteristic constants.

Particularly with humidity acceleration, increasing the relative humidity to around 100% for acceleration purposes may cause condensation to form on the sample, making it impossible to determine the original moisture resistance life. Therefore, sufficient care must be given to temperature and humidity control.

4.3.4 Acceleration by Voltage

Voltage acceleration tests differ greatly according to the device characteristics (MOS, bipolar and other processes, and circuit configuration).

Voltage acceleration tests are said to be effective for MOS LSI, and are often used to evaluate the resistance of gate oxide films. However, voltage acceleration is said to be difficult for bipolar LSI. The voltage acceleration life is expressed as follows.

$$\tau = A \cdot \exp(-V \cdot \beta)$$

Where,
τ : Life A, β : Constants V : Voltage

4.3.5 Acceleration by Temperature Difference

Semiconductors are comprised of combinations of various materials, and the coefficients of thermal expansion of these materials also vary widely. The difference between the coefficient of thermal expansion of each material causes damage (internal force) to accumulate (or sudden breakdown) each time the device experiences a temperature difference, which may lead to eventual failure. Accelerated tests based on temperature differences are carried out to understand this life.

Temperature cycle tests which apply a greater temperature difference than those normally experienced by the device are effective as accelerated tests for evaluating damage caused by temperature differences. Temperature cycle tests refer to tests used to evaluate the device resistance when exposed to high and low temperatures, and also the resistance when exposed to temperature changes between these two temperature extremes. These tests allow confirmation of semiconductor product resistance to temperature stress in the market (for example, the temperature change experienced by a device mounted or left inside an automobile from daytime to nighttime, or when a device cools from high temperature due to self heating when the power is on to room temperature when the power is turned off).

Life related to these temperature differences has been modeled by Coffin-Manson, and is expressed as follows.

$$\tau = A(\Delta T)^m$$

Where,
τ : Life A, m : Constants

This formula shows that accelerated tests can be established for temperature cycle life by providing a large ΔT (temperature difference).

4.4 Reliability Evaluation by TEG

4.4.1 Test Element Group (TEG)

TEG are test patterns designed to allow evaluation of characteristics and shapes by cutting out and focusing on a certain section when testing with the actual device pattern is difficult.

The Sony Semiconductor Network Company performs evaluation using the dedicated TEG shown in Fig. 4-3 to confirm the basic reliability of structures and materials.

Process evaluation TEG	Pattern shape and machining control TEG	Wire width, film thickness, contact shape, cross-sectional shape, wiring step coverage
	Physical property and basic characteristics evaluation TEG	Endurance voltage, sheet resistance, impurity profile, C-V characteristics, interface state, Vth
	Electrical characteristics evaluation TEG	MOS transistors (Vth, gm), memory cells, BIP transistors, capacitors, polysilicon resistors
Circuit characteristics evaluation TEG	Cell evaluation TEG	I/O cells, ESD protection circuits
	Function block evaluation TEG	DRAM, SRAM, logic circuits, A/D converters
Reliability evaluation TEG	Process TEG	Hot carrier, electromigration, time-dependent dielectric breakdown, plasma damage
	Circuit TEG	DRAM, SRAM and logic circuits
	BIP discrete TEG	Transistors, resistors, capacitors
	Package evaluation TEG	Mechanical stress, aluminum sliding, moisture resistance, soldering heat resistance

Fig. 4-3 TEG Types and Purposes

4.4.2 TEG for Reliability Evaluation

4.4.2.1 Process TEG

Reliability is evaluated in the process development stage using process TEG for each element process to start up and confirm basic reliability.

Evaluation items include gate oxide film reliability, transistor hot carrier degradation, wiring electromigration, stress migration, and so on. These items are evaluated in the assembled package and/or on the wafer.

Table 4-3 Failure Mechanisms and TEG Specifications

Failure mechanism	TEG specifications
Electromigration	Wiring length and width Base grade differences Contact chain
Stress migration	Base grade differences Wiring length
Hot carrier	Transistors (gate length and width) Ring oscillators
Time-dependent dielectric breakdown (TDDB)	MOS capacitors (gate oxide film)

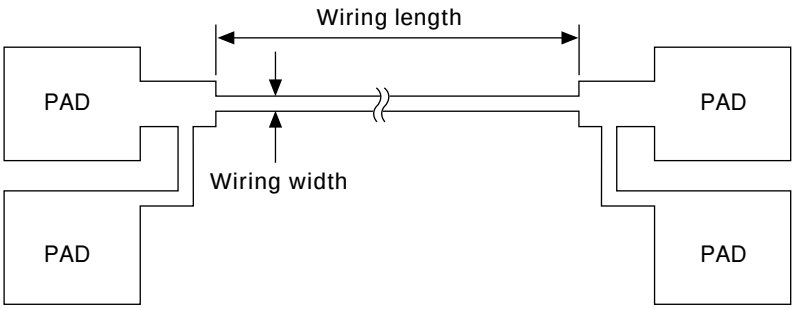


Fig. 4-4 Electromigration Evaluation TEG (Wiring length and width)[1)]

4.4.2.2 Circuit TEG

MOS IC in particular are becoming more complex with increasing circuit scales and mixed mounting of DRAM, and reliability evaluation using actual devices is becoming difficult.

Therefore, during the course of product development, dedicated circuit TEG are created for each logic, DRAM, analog and other circuit, and efficient reliability tests are conducted by dividing devices into elements.

For example, logic circuit reliability is evaluated using SRAM circuit TEG created with the same combination of block elements, and the design is modified to allow easy failure analysis and testing.

4.4.2.3 Bipolar Discrete TEG

When developing a new bipolar process, the reliability of each discrete block element comprising the IC is evaluated. The actual process reliability and problems when integrated into an IC can be understood at an early stage by carrying out this evaluation before IC reliability evaluation.

Discrete TEG include various types of transistors, resistors, capacitors, diodes and so on, and evaluation is possible in a short time by applying high temperature and high humidity bias voltages.

4.4.2.4 Package Evaluation TEG

(1) Development aim

The reliability of mold resin packages has been confirmed to decrease as the mounted chip becomes larger.

The Sony Semiconductor Network Company makes use of this tendency to develop and introduce package evaluation TEG (test element group) chips. These TEG chips allow evaluation with the maximum mountable chip size during new package development, and aim to shorten development and evaluation times and streamline these processes.

(2) TEG specifications

The failure mechanisms that must be confirmed when evaluating package reliability and the corresponding package evaluation TEG specifications are summarized in Table 4-4. In addition, Fig. 4-5 shows an actual layout image.

These TEG allow basic evaluation of package cracking, assembly performance, and the effects of various package-induced damage on chips.

Table 4-4 Failure Mechanisms and TEG Specifications

Failure mechanism		TEG specifications
Package cracking	Resin cracking, gold wire open connections and package expansion caused by the package size and mold resin moisture absorption characteristics	Evaluate at different sizes according to the chip size and package.
Passivation film cracking	Metallic wiring corrosion and migration caused by filler attack, scratches and rubbing	Position wide aluminum wiring in the center of the chip, and check for electrical open or short defects between metallic wiring caused by damage to the passivation or interlayer films.
Aluminum sliding	Metallic wiring open connections and migration caused by mold resin stress	Position aluminum wiring in the chip corners which are susceptible to resin stress, and check for electrical open or short defects between metallic wiring.
Moisture penetration between layers	Wiring open connections, corrosion and ion contamination caused by the penetration of water between the passivation film and metallic wiring or between metallic wiring layers	Position aluminum wiring at the chip edges which are susceptible to moisture penetration and check for electrical open or short defects between metallic wiring.
Chip cracking	Short circuit and leakage defects caused by chip cracking	
Aluminum corrosion	Aluminum wiring corrosion caused by the penetration of water between the passivation film and metallic wiring or between metallic wiring layers	Remove the passivation film from a certain area and check for electrical open defects in the outermost layer of wiring in this area.
Assembly fluctuation	IC characteristics fluctuation before and after encapsulation in mold resin	Position polysilicon resistors in the chip corners which are susceptible to plastic stress, and check the resistance value fluctuation. Also check the transistor operation.
Bonding defects	Wire bonding conditions Cratering, purple plague and bonding peeling caused by the structure under the pad	Evaluate each of these items individually in the die bonding and wire bonding processes.

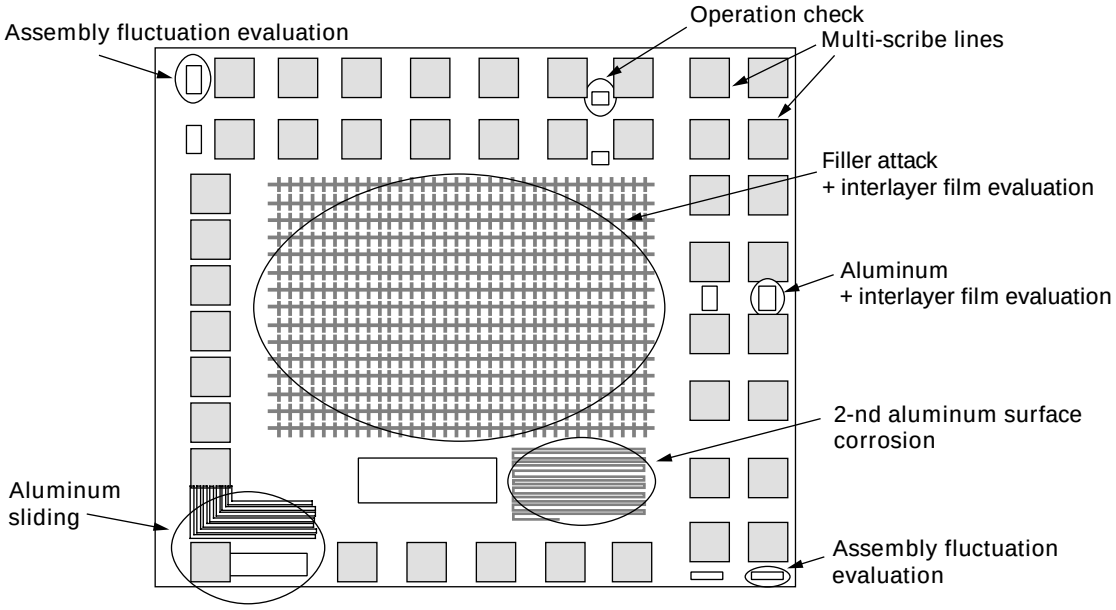
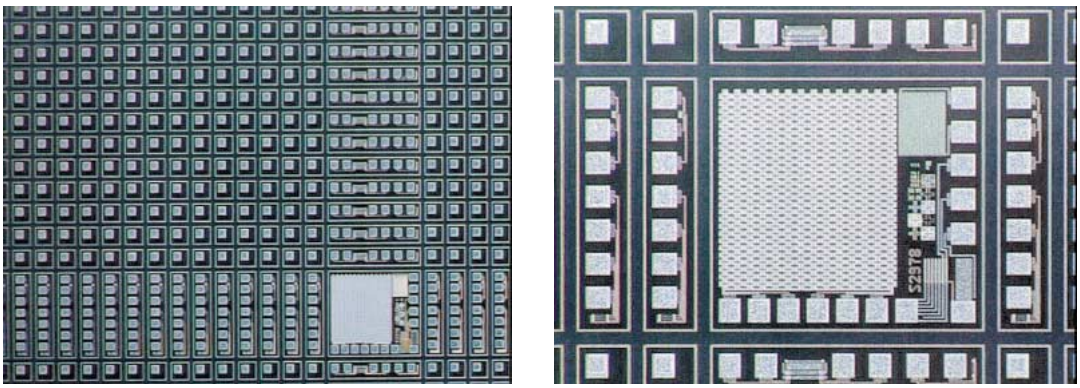


Fig. 4-5 Layout Image

(3) TEG

Photos 4-1(a) and (b) show enlarged photos of a TEG.

This chip employs multi-scribe lines, and the size can be changed in 0.3 mm increments.



(a) Entire chip (b) TEG circuit block

Photo 4-1 Package Evaluation TEG

4.4.3 Reliability Evaluation Methods Using TEG

When evaluating the reliability of semiconductor devices, it is extremely difficult to narrow down reliability problems, particularly those rooted in processes, by evaluating complex integrated circuits such as products. Therefore, detecting reliability problems which may occur at the product stage as early as possible and providing feedback to design and the processes is absolutely essential for establishing high reliability processes and ensuring high product reliability.

Various methods are employed using TEG to quickly clarify failure mechanisms, calculate life prediction parameters, and evaluate mass production process stability, etc.

4.4.3.1 Wafer Level Reliability (WLR)

This method allows easy and speedy evaluation of process reliability at the wafer level for reliability tests using products assembled into packages and TEG.

(1) Features:

TEG are created beforehand for each conceivable failure mechanism, and evaluated using a dedicated measurement program. The advantages of this method are as follows.

- Large amounts of data can be acquired in a short time with the dedicated measuring system.
- The evaluation time can be shortened by carrying out high acceleration tests.
- The reliability of element processes can be evaluated without time-consuming failure analysis.

(2) Applications:

① **Process development stage**

Possible applications as tools supporting the quick start-up of high reliability processes are as follows.

(Examples)

- Evaluation of process reliability before product and TEG reliability tests
- Evaluation of reliability stability and variance during the course of process development
- Relative evaluation and confirmation evaluation when selecting processes, etc.

② **Production stage**

Possible applications as tools for monitoring reliability in the production process are as follows.

(Examples)

- Preemptive detection of reliability problems
- Monitoring of process reliability stability at the production stage
- Go/No Go evaluation of production process changes, etc.

(3) TEG types:

Typical WLR TEG types are as follows.
DRAM cell capacitor film reliability evaluation TEG
Gate oxide film reliability evaluation TEG
Electromigration evaluation TEG
Stress migration evaluation TEG
Hot carrier degradation evaluation TEG
Process charge damage evaluation TEG, etc.

<References>

1) "Standard Guide for Design of Flat, Straight-Line Test Structures for Detecting Metallization Open-Circuit or Resistance-Increase Failure Due to Electromigration", Annual Book of ASTM Standards, Vol.10.04 F1259 (1989).

4.5 Reliability Prediction

4.5.1 Semiconductor Device Failure Rate

In general, the semiconductor device failure rate distribution over time is governed mainly by the initial failure and wear-out failure rates as mentioned in section 4.1. This section provides a detailed description of the Sony Semiconductor Network Company's approach toward semiconductor device failure rates.

4.5.1.1 Semiconductor Device Failure Regions

Fig. 4-6 shows the time-dependent change in the semiconductor device failure rate. Like general electronic equipment, discussions on semiconductor device failure regions often classify failure regions into the three types of initial, random and wear-out failure regions. However, there is no clear definition for determining the boundary between these regions. When drawing time-dependent failure rate curves, the sum of the initial, random and wear-out failure rates can be thought to indicate the transition in the semiconductor device failure rate as shown in Fig. 4-6.

The reliability index used when discussing semiconductor device failure rates thus far has been the average failure rate (FIT value (10^{-9}/device hours)) which follows an exponential distribution with the constant failure rate generally used for system reliability. However, semiconductor devices are manufactured by highly controlled processes, and the failure modes and degradation mechanisms have been clarified to a certain degree. Therefore, viewed in terms of failure mechanisms, randomly occurring failures which are thought to be due to failure modes are virtually nonexistent. Based on the symptoms and results of failure analysis, most failures occurring in reliability tests or in the market can be presumed to be initial failures caused by initial defects or wear-out failures. Therefore, the initial and wear-out failure rates are thought to be important indices in current failure rate prediction for semiconductor devices.

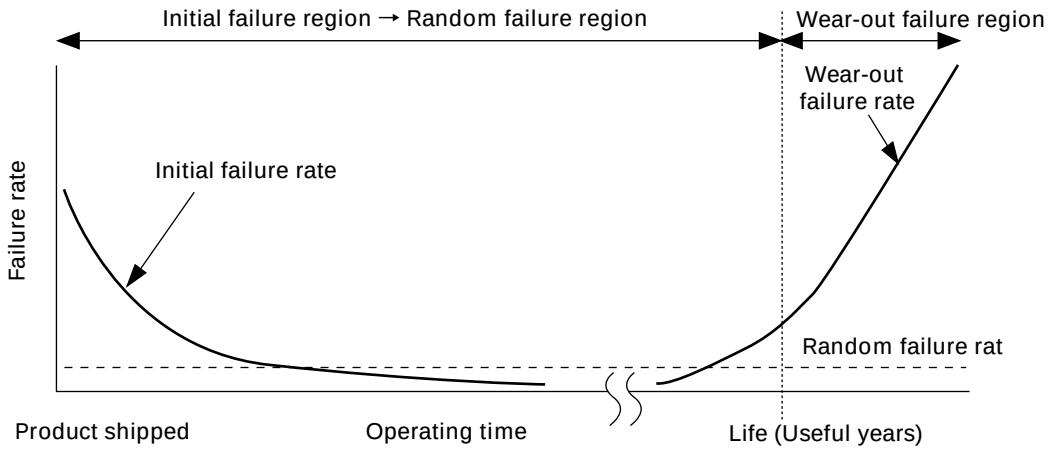


Fig. 4-6 Time-Dependent Change in Semiconductor Device Failure Rate

4.5.1.2 Initial Failures

The failure rate in the initial failure period is called the early failure rate (EFR), and exhibits a shape where the failure rate decreases over time. The vast majority of semiconductor device initial defects are caused by defects built into devices mainly in the wafer process. The most common causes of these defects are dust adhering to wafers in the wafer process and crystal defects in the gate oxide film or the silicon substrate, etc.

Most devices containing defects rooted in the manufacturing process fail within the manufacturing process and are eliminated as defective in the final sorting process. However, a certain percentage of devices with relatively insignificant defects may not have failed when making the final measurements and may be shipped as passing products. These types of devices which are inherently defective from the start often fail when stress (voltage, temperature, etc.) is applied for a relatively short period, and exhibit a high failure rate in a short time within the customer's mounting process or in the initial stages after being shipped as products. However, these inherently defective devices fail and are eliminated over time, so the rate at which initial failures occur decreases.

Eventually, when most of these defective devices have failed and been eliminated, the initial failure rate drops to a level which can be ignored. The failure rate at this stage decreases gradually as an extension of the initial failure rate, but since there are almost no failures, the failure distribution takes the appearance of a random failure region where failure rate does not change.

This property of semiconductor devices where the failure rate decreases over time can be used to perform screening known as "burn-in" where stress is applied for a short time in the stage before shipping to eliminate devices containing initial defects. Product groups from which devices with inherent initial defects have been removed to a certain degree by burn-in not only improve the initial failure rate in the market, but also make it possible to maintain high quality over a long period as long as these products do not enter the wear-out failure region.

(1) Methods for estimating the initial failure rate

Time-dependent changes in the initial failure rate can be estimated by processing failure data obtained by the burn-in study method using a Weibull probability distribution. Burn-in study refers to the method where burn-in is performed consecutively multiple times in a short period under highly accelerated conditions using a sample quantity on a scale which is certain to contain devices with inherent initial devices (normally several thousand to ten thousand pieces). After that the failure data for each measurement time is used to obtain the time-dependent changes in the initial failure rate.

When multiple initial failure rate data obtained through the burn-in study are applied to the following Weibull distribution failure distribution function,

$$F(t) = 1 - \exp\left\{-\left(\frac{t}{\eta}\right)^{m}\right\}$$

the values of shape parameters m and $\ln(t_0)$ can be obtained from the regression line derived from the multiple data as shown in Fig. 4-7. (See Appendix 4-3.)

Furthermore, the cumulative initial failure rate up to the desired time in the market environment can be obtained from the burn-in study conditions and the market environment conditions. (Fig. 4-8)

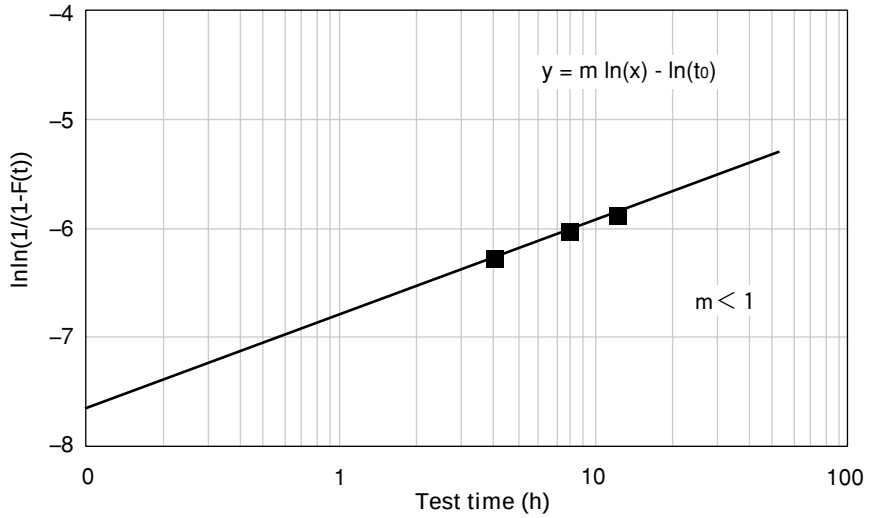


Fig. 4-7 Regression Line Obtained from the Weibull Plot of the Burn-in Study Results

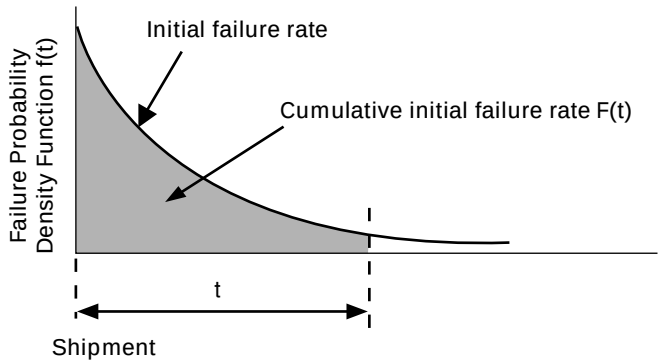


Fig. 4-8 Initial Failure Rate Curve and Cumulative Failure Rate up to Time t

(2) Determining the burn-in conditions

The screening (burn-in) conditions required to reduce the initial failure rate after shipment to the target value can be determined using the failure distribution function F(t) obtained from the burn-in study.

Labeling the burn-in time as t_0 and the coefficient of acceleration for the burn-in conditions and the market environment as K, the cumulative initial failure rate that can be eliminated by burn-in is given as $F(K \cdot t_0)$, and the new cumulative initial failure rate F(t) up to time t after burn-in can be obtained by the following formula.

$$F(t) = F(K \cdot t_0 + t) - F(K \cdot t_0)$$

This relationship can be expressed in graph form as shown in Fig. 4-9.

The burn-in conditions are selected according to the combination of the acceleration conditions and time that will reduce this value to the target initial failure rate or lower.

Normally, initial defects which are the cause of initial failures occur at the highest rate in the initial stages of process development, and then decrease thereafter due to process improvements and process mastery. The initial failure rate decreases in proportion to these initial defects, so the burn-in time is reviewed as appropriate in accordance with process improvements.

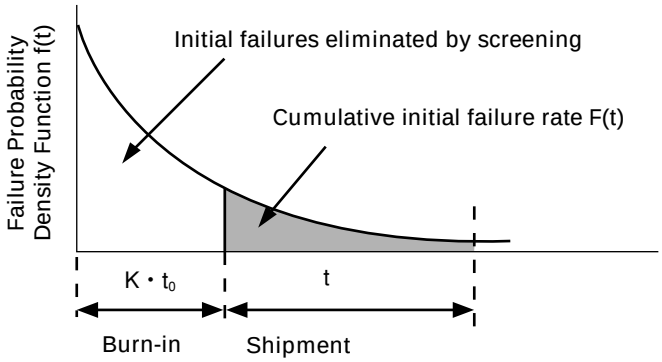


Fig. 4-9 Initial Failure Screening by Burn-in

4.5.1.3 Random Failures

When devices containing initial defects have been eliminated to a certain degree, the initial failure rate becomes extremely small, and the failure rate exhibits a gradually declining curve over time. In this state, the failure distribution is close to an exponential distribution, and this is called the random failure period. The semiconductor device failure rate during this period is an extremely small value compared to the initial failure rate immediately after shipment, and is normally a level which can be ignored for the most part. Viewed in terms of failure mechanisms, there are extremely few semiconductor device failures that can be clearly defined as random failures. However, memory software errors and other phenomena caused by α rays and other high energy particles are sometimes classified as randomly occurring failure mechanisms.

When predicting semiconductor device failure rates, failures occurring sporadically after a certain long time has passed since the start of operation and failures for which the failure cause could not be determined are treated as random failures in some cases. However, most of these failures are thought to be devices containing relatively insignificant initial defects (dust or crystal defects) which fail after a long time, and should essentially be positioned on the initial failure rate attenuation curve. This type of failure rate cannot be estimated from the results of tests performed with few samples such as reliability tests.

There are also phenomena such as ESD breakdown, overvoltage (surge) breakdown (EOS) and latch-up which occur at random according to the conditions of use. However, these phenomena are all produced by the application of excessive stress over the device absolute maximum ratings, so these are classified as breakdowns instead of failures, and are not included in the random failure rate.

4.5.1.4 Wear-out Failures

Wear-out failures are failures rooted in the durability of the materials comprising semiconductor devices and the transistors, wiring, oxide films and other elements, and are an index for determining the device life (useful years). In the wear-out failure region, the failure rate increases with time until ultimately all devices fail or suffer characteristic defects. (Fig. 4-10)

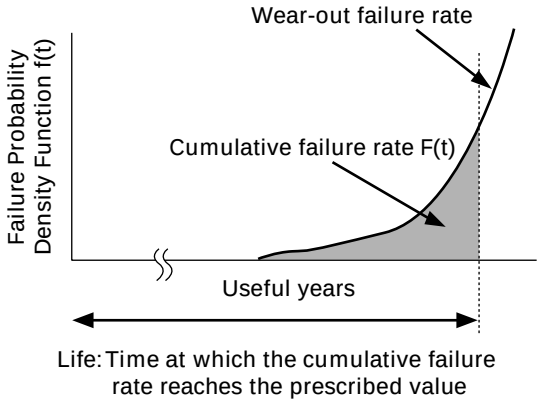


Fig. 4-10 Wear-out Failure Rate Curve and Life

The main wear-out failure mechanisms for semiconductor devices are as follows.

- Electromigration
- Hot carrier-induced characteristics fluctuation
- Time-dependent dielectric breakdown (TDDB)
- Laser diode luminance degradation

Semiconductor device life is defined as the time (or stress) at which the cumulative failure rate for the wear-out failure mode reaches the prescribed value, and can be estimated using the results of reliability tests and test element group (TEG) evaluation. Semiconductor device life is often determined by the reliability of each element (wiring, oxide film, interlayer film, transistor) comprising the device, and these reliabilities are evaluated using discrete element TEG in the process development stage. These TEG evaluation results are incorporated into design rules in the form of allowable stress limits (electric field strength, current density, etc.) to suppress wear-out failures in the product stage and ensure long-term reliability. As a result, semiconductor devices experience almost no wear-out failures within the reliability test time (stress) range in the product stage.

(1) Life estimation method

Semiconductor device life can be obtained as follows based on the wear-out failure data generated by TEG evaluation and reliability tests. First linear regression is performed for the time-dependent cumulative failure rate using a Weibull probability distribution or logarithmic normal probability distribution, then the life is obtained from the time (or stress) at which the reference cumulative failure rate is reached and the acceleration multiple of the accelerated test conditions (Fig. 4-11).

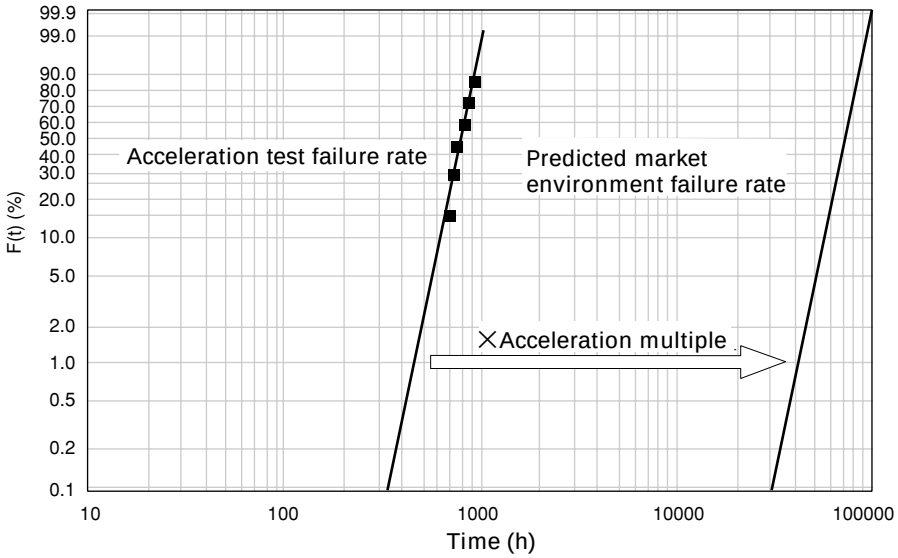


Fig. 4-11 Failure Rate Prediction Method Using Weibull Probability Plotting Paper

4.5.2 Acceleration Theory

Semiconductors experience characteristics degradation and failure due to temperature, humidity and other external environmental conditions and stress such as heat generation, voltages and currents during operation, etc. This section derives acceleration factors from the basic formulas stating how life is affected by the size of each stress. Acceleration factors represent the ratio of the life in the customer's operating stress environment to the life in the reliability test, burn-in or other stress environment. For example, if the life in the customer's operating stress environment is 10 years and the life in the reliability test stress environment is 0.1 year, the acceleration factor is 10 years/0.1 years = 100 times.

(1) Temperature acceleration

Generally, most failure mechanisms are promoted by exposure to high temperatures. The life temperature acceleration factor K at this time can be obtained from the Arrhenius model using the following formula.

$$K \equiv \frac{\tau_F}{\tau_E} = \exp\left\{\frac{Ea}{k}\left(\frac{1}{T_F} - \frac{1}{T_E}\right)\right\}$$

Where,

τ_F : Market life
τ_E : Reliability test life
T_F : Market operating temperature
T_E : Test temperature

(2) Acceleration factors other than temperature

The actual semiconductor life also changes according to stress factors other than temperature such as temperature and humidity, temperature and voltage, and temperature and current. These cases use the following life formula which adds another stress item to the above mentioned temperature item.

$$\tau = A\exp(-\beta \cdot S)\cdot\exp\left(\frac{Ea}{kT}\right)$$

Where,
β : Constant
S : Non-temperature stress

Note that the following formulas may be used, but these formulas are mathematically equivalent.

When $\gamma \equiv \beta/\ln(10)$

$$\tau \propto 10^{-\gamma S}\cdot\exp\left(\frac{Ea}{kT}\right)$$

When $S' \equiv \exp(S)$

$$\tau \propto S'^{-\beta}\cdot\exp\left(\frac{Ea}{kT}\right)$$

Like the Arrhenius model, labeling the operating or storage stress as S_F, the reliability test stress as S_E, and the respective lives as τ_F and τ_E, the acceleration factor K is given by the following formula.

$$\begin{aligned} K &\equiv \frac{\tau_F}{\tau_E} \\ &= \exp\{-\beta(S_E - S_F)\}\cdot\exp\left\{\frac{Ea}{k}\left(\frac{1}{T_F}-\frac{1}{T_E}\right)\right\} \\ &= 10^{-\gamma(S_E-S_F)}\cdot\exp\left\{\frac{Ea}{k}\left(\frac{1}{T_F}-\frac{1}{T_E}\right)\right\} \\ &= \left(\frac{S'_E}{S'_F}\right)^{-\beta}\cdot\exp\left\{\frac{Ea}{k}\left(\frac{1}{T_F}-\frac{1}{T_E}\right)\right\} \end{aligned}$$

Assuming $\beta_1 = \beta$, $S_1 = S$, $\beta_2 = \frac{Ea}{k}$, $S_2 = \frac{1}{T}$ the life formula can be transformed into a formula for general stress as follows.

$$\tau = A\exp(-\beta_1 \cdot S_1)\cdot\exp(-\beta_2 \cdot S_2)$$

When there are n stress factors, an even more general formula is obtained.

$$\tau = A\exp(-\beta_1 \cdot S_1)\cdot\exp(-\beta_2 \cdot S_2)\cdot\cdots\cdot\exp(-\beta_n \cdot S_n)$$

Labeling the operating or storage stress as S_{iF} (i = 1,..., n), the reliability test stress as S_{iE} (i = 1,..., n), and the respective lives as τ_F and τ_E, the acceleration factor is given by the following formula.

$$K \equiv \frac{\tau_F}{\tau_E} = \exp\{-\beta_1(S_{1E}-S_{1F})\}\cdot\cdots\cdot\exp\{-\beta_n(S_{nE}-S_{nF})\}$$

4.5.3 Stress Acceleration Tests

In order to obtain acceleration factors, tests are carried out by varying stress and the acceleration factors are calculated based on these results.

Voltage acceleration is used here as an example.

Voltage acceleration is given by substituting n = 1 and voltage S = V to the general life formula.

$$\tau = A\exp(-V \cdot \beta)$$

If the constants A and β are known, the relationship between the voltage V and life τ can be clarified. Therefore, these constants can be calculated by experimentally obtaining the life at multiple voltages.

Taking the natural logarithm ln, the above formula can be transformed as follows.

$$\ln\tau = \ln A - \beta \cdot V$$

β can be obtained from the slope when plotting this formula with the voltage V as the horizontal axis and the life τ as the vertical axis. (Fig. 4-12)

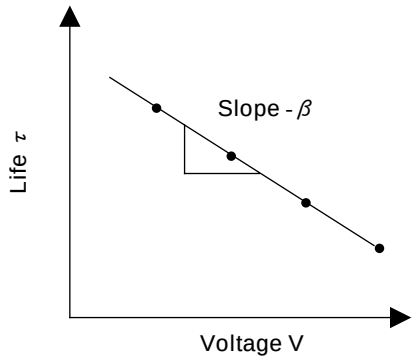


Fig. 4-12 Relationship between Voltage and Life τ

The life also contains variance which is not due to stress. This variance follows a Weibull or logarithmic normal distribution, but in consideration of the distribution with respect to individual stresses, η and μ are used in place of τ for the Weibull and logarithmic normal plots, respectively.

A typical stress acceleration test procedure is described below.

(1) Perform the stress acceleration test.

(2) Obtain the cumulative failure rate.

(3) Draw the Weibull or logarithmic normal plots. Fig. 4-13 shows the plots for the four voltage conditions of V_1, V_2, V_3 and V_4.

(4) Read η or μ from the plots.

(5) Plot the relationship between the stress and η or μ.

(6) Read the constant from the plotted slope.
In this voltage acceleration example, read β from the graph. (Fig. 4-14)

(7) Obtain the acceleration factor.
For example, the acceleration factor between the test voltage and the market voltage is as follows.

$$K = \exp\{-\beta(V_E - V_F)\}$$

Where,
V_E: Test voltage V_F: Market operating voltage

(8) The acceleration factor is useful for determining the burn-in time or estimating the life.

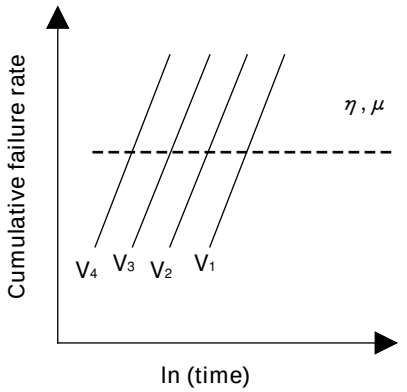


Fig. 4-13 Weibull Plots for Different Voltage Conditions

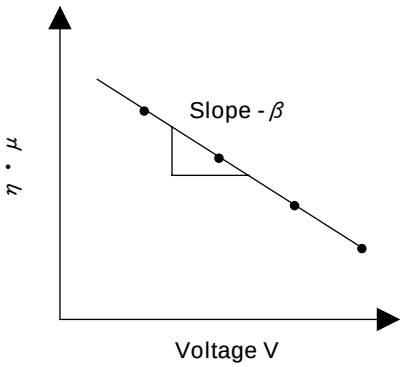


Fig. 4-14 Relationship between Voltage and Life $\eta \cdot \mu$

4.5.4 Failure Rate Prediction Case Studies

(1) Estimation of hot carrier degradation life for a high speed CMOS logic IC

Subject: C6 series (0.25 μm) logic IC with a system clock of approximately 600 MHz
Failure mechanism: Drain avalanche hot carrier (DAHC)

$$\tau \propto V^{-n} \cdot \exp\left(\frac{Ea}{kT}\right)$$

Where,
V : Supply voltage T : Temperature

Acceleration factor $$K = \left(\frac{V_E}{V_F}\right)^n \cdot \exp\left\{\frac{Ea}{k}\left(\frac{1}{T_F} - \frac{1}{T_E}\right)\right\}$$

Where,
T_E : Test temperature T_F : Market operating temperature

Reliability test: Low temperature operation and high temperature operation tests with the system clock held constant at approximately 600 MHz regardless of the supply voltage and temperature

Fig. 4-15 shows the reliability test results.

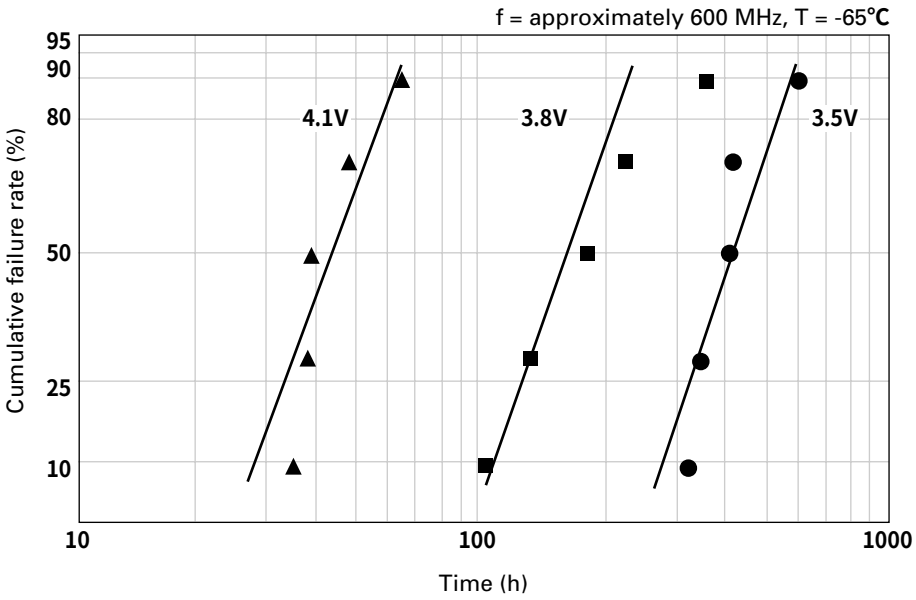


Fig. 4-15 Logarithmic Normal Plot of Hot Carrier Failure

Logarithmically plotting both the average failure rate μ and the voltage V from this logarithmic normal plot yields the results shown in Fig. 4-16. The constant n which represents the voltage acceleration characteristics can be obtained from this slope.

n = 14.1

Regarding temperature acceleration, the activation energy Ea = -0.049 [eV] was obtained from the test results at T = -65°C to +125°C. At this point, the test acceleration characteristics are obtained as follows using the voltage acceleration factor for an actual IC operating voltage V_F = 2.5 V and reliability test condition V_E = 3.5 V, and the temperature acceleration factor for an actual IC operating temperature T_F = 55°C and reliability test condition T_E = -65°C.

$$K=\left(\frac{V_E}{V_F}\right)^{14.1}\cdot\exp\left\{\frac{-0.049}{k}\left(\frac{1}{T_F}-\frac{1}{T_E}\right)\right\}$$

$$= 312 \text{ times}$$

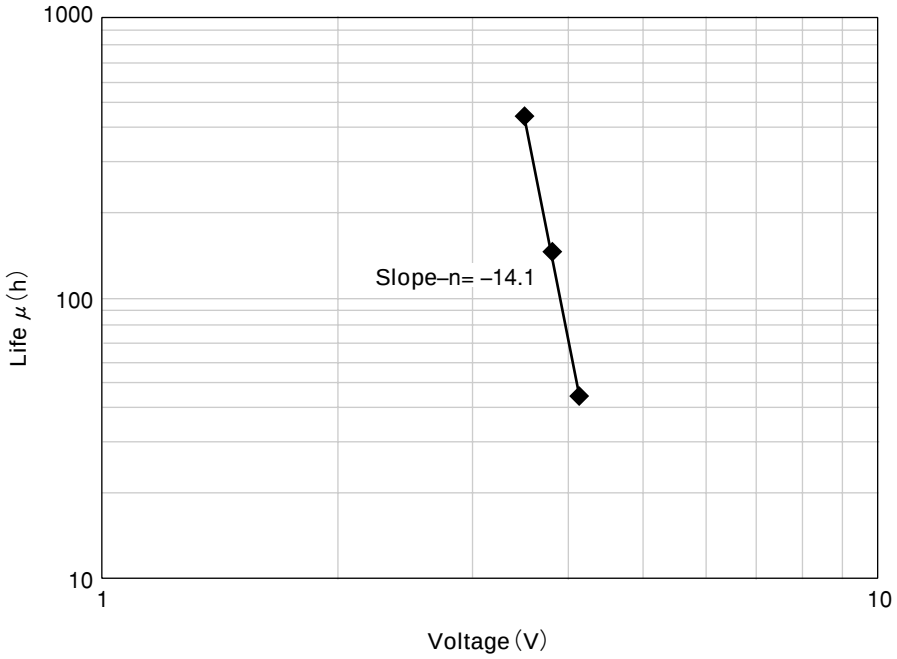


Fig. 4-16 Hot Carrier Voltage Acceleration Characteristics

The failure rate graph under actual operating conditions can be obtained by multiplying the average life μ obtained from the logarithmic normal plot of the test results at T = -65℃ and V = 3.5 V with the acceleration factor K = 423 times, and drawing a straight line with the same slope through this value. (Fig. 4-17) The life t_{50} at which half of these devices will fail can be estimated from this graph as 1.8×10^5 [h] = 20.5 years.

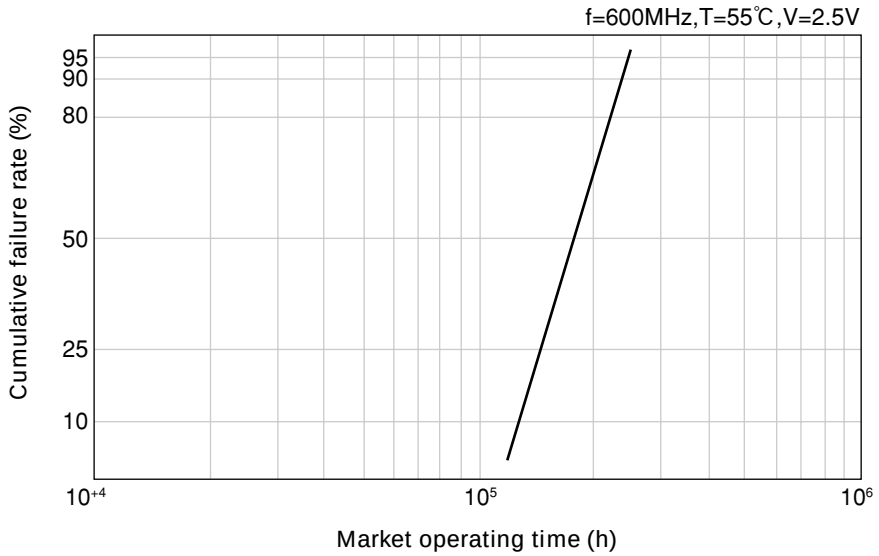


Fig. 4-17 Logarithmic Normal Plot of Hot Carrier Failure

(2) Estimation of BGA thermal stress reliability life

Subject : BGA package for system LSI

Failure mechanism : BGA wiring substrate open connection failure caused by cracking when thermal stress is applied to the semiconductor mold resin

$$\tau \propto f^{m}(\Delta T)^{-n}\exp\left(\frac{Ea}{kT_{max}}\right)$$

Where,

ΔT : Temperature difference

n, m : Constants

Assuming the stress to be dependent only on the temperature difference ΔT,

$$\tau \propto (\Delta T)^{-n}$$

Accordingly, the acceleration factor K is:

$$K=\left(\frac{\Delta T_E}{\Delta T_F}\right)^{n}$$

Where

ΔT_E : Test temperature difference ΔT_F : Market temperature difference

Reliability test : Temperature cycle test with varying temperature differences ΔT

Fig. 4-18 shows the reliability test results.

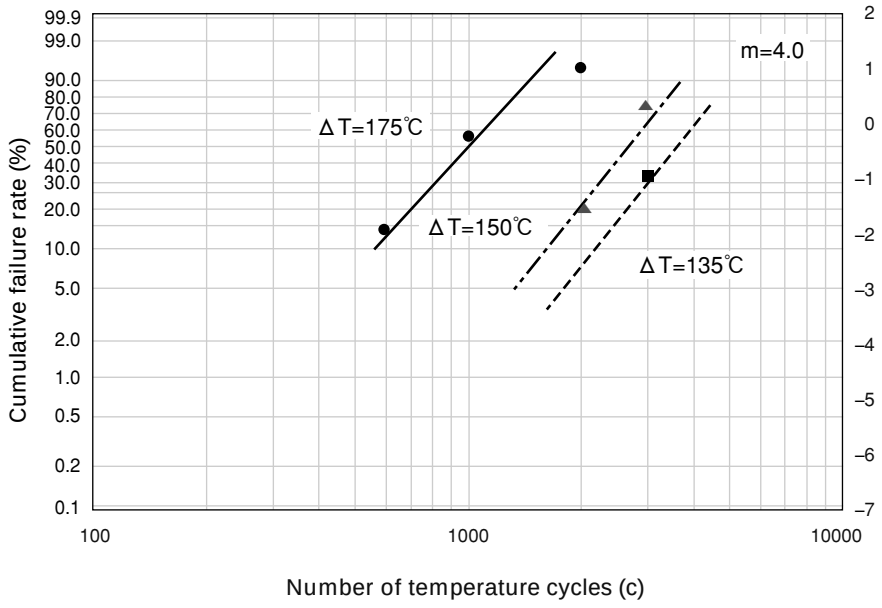


Fig. 4-18 BGA Package Temperature Cycle Test Results[1)]

Logarithmically plotting both the life η and the temperature difference ΔT from this Weibull plot yields the results shown in Fig. 4-19. The constant n which represents the temperature acceleration characteristics can be obtained from this slope.

n = 4.9

The acceleration factor for market condition $\Delta T_F = 50℃$ and test condition $\Delta T_E = 150℃$ is as follows.

$$K = \left(\frac{\Delta T_E}{\Delta T_F}\right)^{4.9}$$

$$= 217 \text{ times}$$

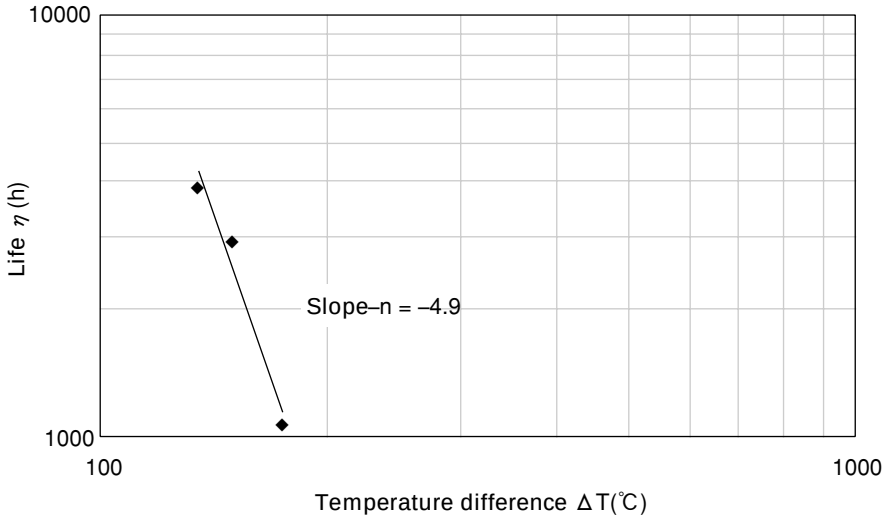


Fig. 4-19 Cracking Dependency on Temperature Difference

In addition, the actual operating environment life t_{50} is given as follows by multiplying the t_{50} value obtained from the test results at $\Delta T = 150℃$ by the acceleration factor K.

$$t_{50} = 2700 \text{ cycles} \times 217 \text{ times} = 5.9 \times 10^5 \text{ cycles}$$

These results correspond to a life of approximately 1,000 years or more assuming the usage where the product is turned on and off one time per day.

(3) Estimation of DRAM fuse moisture resistance life

Subject : 0.35 µm generation DRAM

Failure mechanism : Memory device fuse circuit element corrosion

$$\tau \propto P_{H_2O}^{-n}$$

Where,
P_{H_2O} : Steam pressure

Acceleration factor $K = \left(\frac{P_E}{P_F}\right)^n$

Where,
P_E : Test steam pressure
P_F : Market storage environment steam pressure

Reliability test : Pressure cooker test using three different steam pressures

Fig. 4-20 shows the reliability test results.

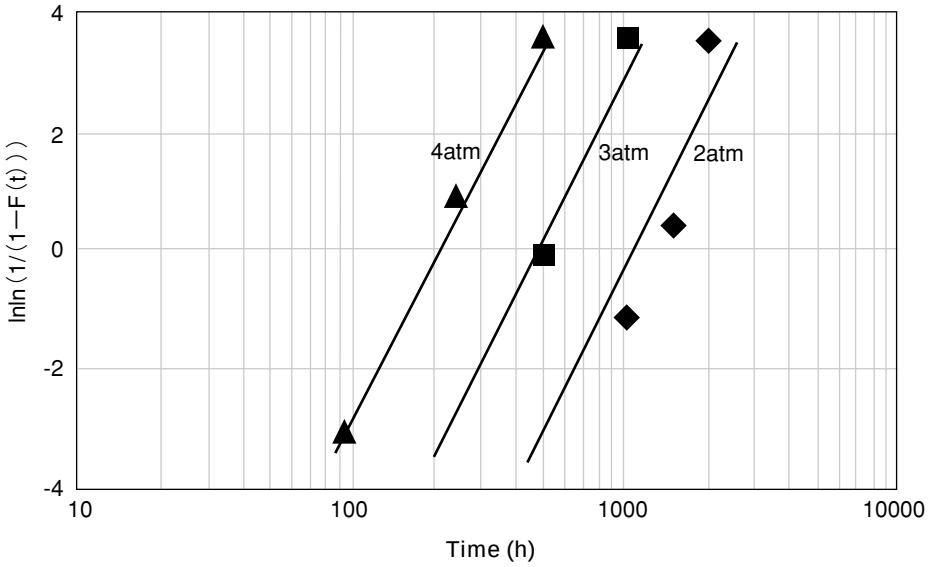


Fig. 4-20 Weibull Plot for Fuse Corrosion Failure

Reading the parameter η from the Weibull plot in Fig. 4-20, the steam pressure acceleration characteristics constant n can be obtained from the relationship between the average life η and the steam pressure shown in Fig. 4-21.

n = 2.82

When the actual operating environment conditions are 30℃ and 85% RH, the steam pressure is $P_F = 3.606 \times 10^3$ Pa, so the acceleration factor at the test condition $P_E = 2.03 \times 10^5$ Pa is given as follows.

$$K = \left(\frac{P_E}{P_F}\right)^{2.82}$$

$$= 8.74 \times 10^4 \text{ times}$$

In addition, the life t_{50} in the actual operating environment is given as follows by multiplying the t_{50} value obtained from the test results at PE = 2.03×10^5 Pa by the acceleration factor K.

$$t_{50} = 1.23 \times 10^3 \times 8.74 \times 10^4 = 1.08 \times 10^8 \text{ hours} = 12{,}300 \text{ years}$$

These results show that the life is semi-permanent even for storage at the high temperature and high humidity of 30℃ and 85% RH.

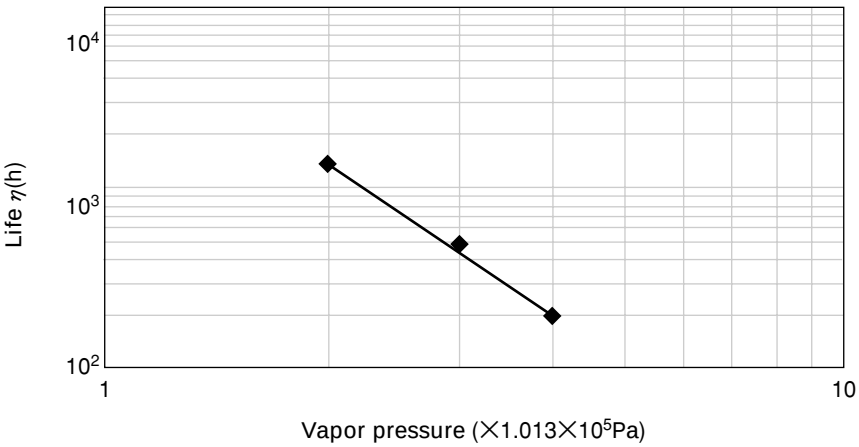


Fig. 4-21 Vapor Pressure Acceleration Characteristics

<References>

1) Shiraishi et al., “Investigation of a Life Model in Temperature Cycle Evaluation of BGA Packages”, Preliminary Manuscripts for the 9th RCJ Reliability Symposium, pp.43, (1999).

4.6 Test Coverage

Test coverage generally refers to the random gate test quality, and is defined as follows.

Test coverage [%] = 100 × Number of detected failures/Total number of failures

The number of failures here is normally the number of failures hypothesized by the simple degenerative failure model. The degenerative failure model is a failure model which simplifies various real failures into the two types of short circuits with GND (0 degenerative failures) and short circuits with V_{DD} (1 degenerative failures). The simple degenerative failure model is a further simplified model which assumes that these degenerative failures exist at only one location within a circuit. This simple degenerative failure model is used for failure simulations and automatic test pattern generation (ATPG) using scan path test facilitating designs. These simple degenerative failures assume that there are two 0 degenerative failures and two 1 degenerative failures in each of the input/output pins of all gates. This total number is used as the total number of failures, and of these the tested failures are used as the number of detected failures.

A different type of test coverage can be considered for memory cells and analog elements, etc.

In contrast to random gates, memory cells have a regular and highly integrated structure, and are designed using transistors and wiring. Therefore, test patterns which hypothesize more specific failures and have a test coverage of 100% are designed and used. Well-known test patterns of this type include matching patterns and checkerboard patterns.

When LSI manufacturers create test patterns using memory test facilitating designs (direct access from the chip pins, build-in self test (BIST), etc.), the test coverage need not be taken into account.

There is also no concept of test coverage for analog elements. This is because analog elements generally have irregular structures and are designed using various transistors and wiring, which makes simplifying potential failures or focusing on particular failures difficult. Therefore, analog elements are tested based on their individual specifications.

In addition to test coverage, the process yield is also related to LSI quality. Even with the same test coverage, higher quality can generally be obtained by manufacturing with a high yield process than a low yield process. Stated another way, when using the latest processes, test facilitating designs (scan path, memory build-in self test, etc.) should be actively applied to increase the test coverage as much as possible.

4.7 Reliability Related Standards

There are numerous standards related to semiconductor device reliability, and these standards can be broadly classified as shown in Table 4-5. Among these standards, activities have increased recently toward the adoption of international standards from the viewpoint of eliminating import-export barriers and technical obstacles for international trade. The Sony Semiconductor Network Company is an active participant in various standardization committees both domestically and in the U.S. and Europe, and promotes vigorous standardization activities.

Table 4-5 Reliability Related Standards

International standards	ISO, IEC
Regional standards	CEN, CENELEC (Europe)
National standards	JIS (Japan), ANSI (U.S.), BS (England),・・・
Public agency standards	MIL (U.S. Department of Defense),・・・
Industry standards, etc.	EIAJ, JASO, RCJ, EIA/JEDEC, UL, ・・・

ISO: International Standard Organization
IEC: International Electrotechnical Commission
JIS: Japanese Industrial Standard
BS: British Standard
MIL: Military Standard
EIAJ: Electronic Industries Association of Japan
RCJ: Reliability Center for Components of Japan
JEDEC: Joint Electron Device Engineering Council
EIA: Electronic Industries Association
UL: Underwriters Laboratories
ANSI: American National Standards Institute
CEN: Comite Européen de Normalisation
CENELEC: Comite Européen de Normalisation Électrotechnique
JASO: Japanese Automobile Standards Organization

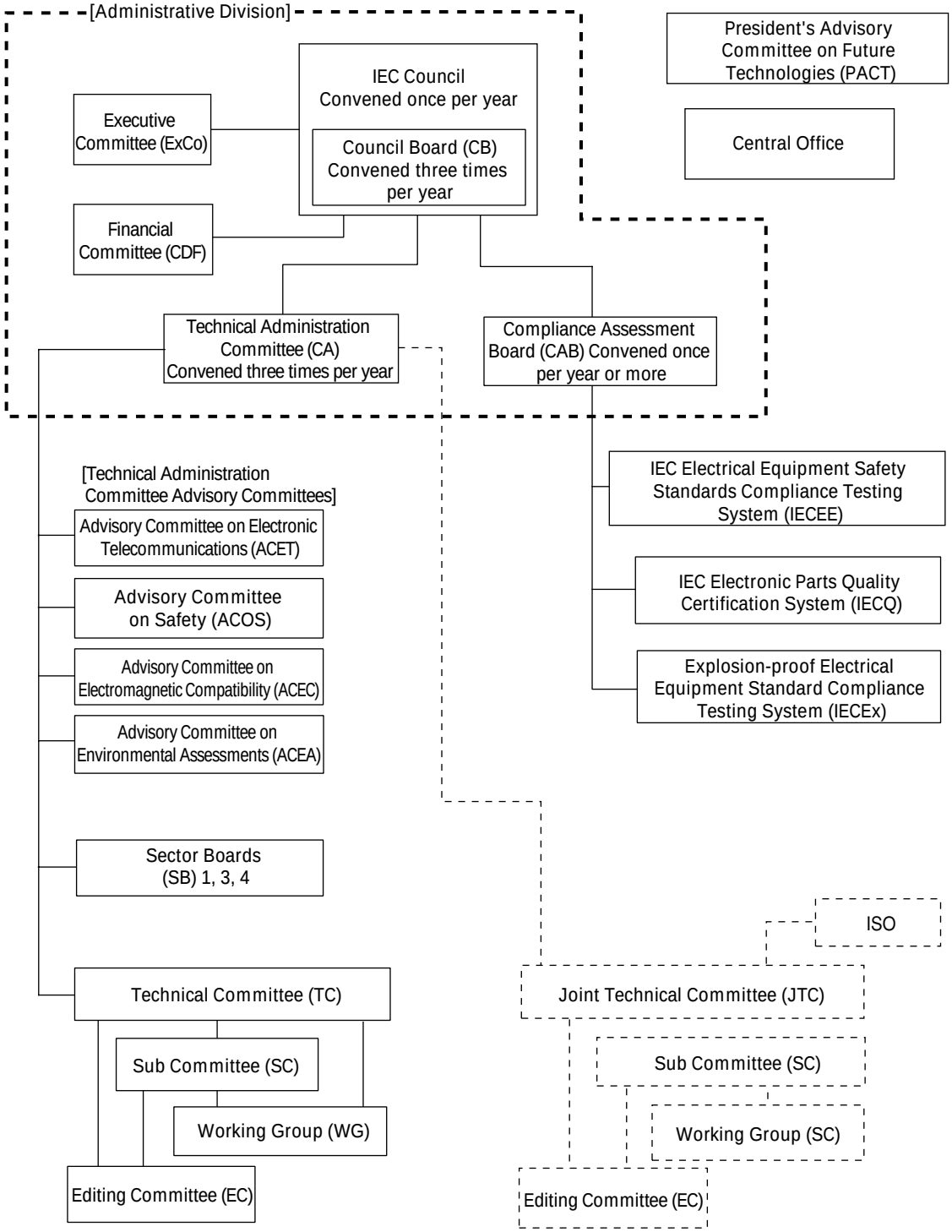
(1) IEC (International Electrotechnical Commission)

IEC was founded in 1908 as a private nonprofit foundation based on the Swiss Civil Code. However, it has currently reached a status where it is treated roughly on a par with the United Nations as an international standards organization, and is acknowledged as a world standard even in the Agreements of the World Trade Organization (WTO) technological Barrier for Trade (TBT).

IEC's stated purpose is to "promote international cooperation related to standardization in the electric and electronic technology fields, and to work toward a mutual international understanding." IEC establishes standards for terminology, symbols, ratings, various test methods and other items for all electric and electronic fields except information technology.

IEC has established technical committees (TC) and affiliated sub committees (SC) for each technical field, and institutes standards based on an “international consensus” after years of phased deliberations. The IEC organization diagram is shown in Table 4-6.

Table 4-6 IEC (International Electrotechnical Commission) Organization Diagram



Note that only one representative organization per country is qualified for IEC membership. In Japan this is the Japan Industrial Standards Committee (JISC) established under the Industrial Standards Act. The Standards Department of the Agency of Industrial Science and Technology, Ministry of International Trade and Industry serves as the JISC Secretariat.

Examples of IEC standards related to reliability are shown in Table 4-7 below.

Table 4-7 IEC Standards

IEC60695	Fire resistance testing methods for general parts
IEC60068	Environmental testing methods for general parts
IEC60747	Specifications by semiconductor device type
IEC60748	Specifications by semiconductor integrated circuit type
IEC60749	Mechanical and weather resistance testing methods for semiconductor devices

(2) EIAJ (Electronic Industries Association of Japan)

EIAJ is an industry body established in 1948 which deliberates and establishes standards to promote smooth business transactions in the fields of consumer and industrial use electronic equipment, electronic parts and devices. Together with the Japan Electronic Industry Development Association (JEIDA) and Japan Electrical Manufacturers' Association (JEMA), EIAJ activities fulfill essential standardization functions domestically within Japan. In addition, EIAJ promotes activities to advocate EIAJ standards (drafts) as IEC standard proposals, and functions as a liaison with EIA, JEDEC and other related overseas committees. The Sony Semiconductor Network Company is an active participant in various EIAJ committees, and deploys standardization activities.

JIS standards (JIS C 7021, 7022) concerning semiconductor device reliability were abolished in 1997, and currently EIAJ is the Japanese domestic standard which is most often used as a reference for determining actual test methods, etc. These contents are also extremely practical, and could be called advanced. Table 4-8 shows the EIAJ standards concerning semiconductor reliability.

Table 4-8 EIAJ Standard Types

ED-4701（1992）	Environmental and durability testing methods for semiconductor devices
ED-4701-1（1994）	Environmental and durability testing methods for semiconductor devices Supplement 1) ESD breakdown test (Human Body Model), etc.
ED-4701-2（1995）	Environmental and durability testing methods for semiconductor devices Supplement 2) Solderability test and other revisions
ED-4701-3（1997）	Environmental and durability testing methods for semiconductor devices Supplement 3) ED-4701 revision
ED-4701-4（1998）	Environmental and durability testing methods for semiconductor devices Supplement 4) Soldering heat resistance test (SMD)
ED-4702（1992）	Mechanical strength testing methods for surface mounted semiconductor devices
ED-4703（1994）	Process internal evaluation and structural analysis methods for semiconductor devices
ED-4703-1（1995）	Process internal evaluation and structural analysis methods for semiconductor devices Supplement 1) Scanning acoustic tomography (SAT), etc.
EDX-4702（1994）	ESD breakdown testing methods for semiconductor devices (Preliminary) (Charged device model CDM/ESD)
EDR-4701B（1996）	Semiconductor device handling guide
EDR-4702（1996）	Semiconductor device quality and reliability testing method and standard comparison table
EDR-4703（1999）	Quality assurance guidelines for bare dies including KGD

KGD：Known Good Die

(3) JEDEC

JEDEC is equivalent to the U.S. Electronic Industries Alliance (EIA) division concerned with semiconductor devices, and both JEDEC and EIA are affiliated with the American National Standards Institute (ANSI).

JEDEC spans a wide range of fields including JESD22 which summarizes various environmental testing methods, JESD78 which describes latch-up testing methods, package outline specifications, packing magazine specifications, statistical process control (SPC), etc.

(4) Standards comparison table

Table 4-9 shows part of a table comparing the reliability testing methods of major standards (including Sony Semiconductor Network Company standards).

Table 4-9 Reliability Test Standards Comparison Table

<table>
<tr><th></th><th>Sony</th><th>EIAJ</th><th>IEC</th><th>JEDEC</th></tr>
<tr>
<td>Temperature cycle (Gaseous phase)</td>
<td>
• Condition selection (according to the product specifications)
A: –65±5 / 150±5°C
B: –55±5 / 125±5°C
C: –40±5 / 100 $^{+5}_{-3}$°C
D: –30±5 / 85 $^{+5}_{-3}$°C
E: –30±5 / 75 $^{+5}_{-3}$°C
F: 0 $^{+5}_{-3}$ / 125±5°C
G: –25±5 / 125±5°C

• High/low temperature exposure time
A to E: 30 minutes, F: 15 minutes, G: 10 minutes
• The shelf time includes the time from when the sample is placed in the chamber until the temperature inside the chamber stabilizes.
• Normal temperature exposure time
A to E: 5 $^{+0}_{-1}$minutes
FG: 2-zone test (automatic damper opening and closing)
• The condition G test temperature is prescribed by the sample temperature.
• A to F prescribe the temperature near the test area blow-out opening.
• Normal temperature (T_N): 5 to 45°C
• 100 cycles unless otherwise specified

• Continue and perform the soldering heat resistance test.

• Electrical characteristics measurement
</td>
<td>
EIAJ ED-4701-3 (1997)
Test method B-131A

• Tstg min~Tstg max
• Allowable temperature difference
125°C or more: ±5°C
Less than 125°C: $^{+5}_{-3}$°C
–25°C or more: $^{+5}_{-3}$°C
Less than –25°C: ±5°C
• Normal temperature (T_N): 5 to 35°C
• The shelf time is selected according to the sample discrete mass (m).
<table>
<tr><th>m (g)</th><th>a, c</th><th>b, d</th></tr>
<tr><td>m≦15g</td><td>10 minutes or more</td><td>5 minutes or less</td></tr>
<tr><td>15<m≦150</td><td>30 minutes or more</td><td>15 minutes or less</td></tr>
<tr><td>150<m≦1500</td><td>60 minutes or more</td><td>30 minutes or less</td></tr>
<tr><td>1500<m</td><td colspan="2">Prescribed individually</td></tr>
</table>
a: Low temperature shelf time
c: High temperature shelf time
b, d: Transition time

• Prescribed temperature arrival time: t
The longer of 5 minutes or 10% of a and c
• If the sample does not reach the storage temperature within the prescribed time, count the time from when the sample reaches thermal equilibrium.
• 5 cycles unless otherwise specified.
</td>
<td>
IEC60749 (1996-10)
CHAPTER 3 1.1

• Minimum storage temperature (°C) T_A
–65, –55, –40, –25, –10, –5, +5°C
±3°C in all cases
• Maximum storage temperature (°C) T_B
200, 175, 155, 125, 100, 85, 70, 55, 40, 30°C
±2°C in all cases
• Shelf time: t_1
10 minutes when the sample temperature reaches the prescribed temperature in 3 minutes or less, 10 minutes from when the sample temperature achieves equilibrium in all other cases.
(The sample temperature shall achieve equilibrium in 20 minutes or less, in any case.)
• Transition time: t_2
2 to 3 minutes or less (standard), 1 minute or less (automated equipment)
• 5 cycles
• The thermal time constants of the sample and carrier are taken into account.
• Electrical characteristics measurement + visual inspection of the exterior
• Air circulation speed inside the chamber: 2 m/s or more
• Absolute humidity inside the chamber: 20 g/m^3 or less
• The time from when the sample is placed in the chamber until the temperature inside the chamber stabilizes shall be included in the shelf time, but shall comprise 10% or less of the shelf time.

[Reference standards]
IEC60068-2-14(1984-01)
IEC60068-2-14-am1(1986-01)
</td>
<td>
JESD22-A104-A (1989)

• Condition selection
A: –55 $^{+0}_{-10}$ / 85 $^{+10}_{-0}$°C
B: –55 $^{+0}_{-10}$ / 125 $^{+10}_{-0}$°C
C: –65 $^{+0}_{-10}$ / 150 $^{+10}_{-0}$°C
D: –65 $^{+0}_{-10}$ / 200 $^{+10}_{-0}$°C
F: –65 $^{+0}_{-10}$ / 175 $^{+10}_{-0}$°C
G: –45 $^{+0}_{-10}$ / 125 $^{+10}_{-0}$°C
H: –55 $^{+0}_{-10}$ / 150 $^{+10}_{-0}$°C

• Normal temperature exposure is not prescribed.
• Transition time: 1 minute or less
• The load temperature shall arrive at the prescribed temperature in 15 minutes or less.
• Exposure time: 10 minutes or more each
• 10 cycles or more at condition C unless otherwise specified

• Acceptance test: 10 cycles
Certification test: 100 cycles
</td>
</tr>
</table>

Table 4-9 Reliability Test Standards Comparison Table

<table>
<tr><th></th><th>Sony</th><th>EIAJ</th><th>IEC</th><th>JEDEC</th></tr>
<tr>
<td>Thermal shock (Liquid phase)</td>
<td>
• –65±5～150±5℃
• GALDEN^{R} D02 TS
(Perfluoropolyether)
Electronics test grade used
• Dipping time: 5 $^{+1}_{-0}$ minutes
• Transition time: 10 s or less
• Standard 100 cycles
• Start from normal temperature and count from the low temperature side.

• Continue and perform the soldering heat resistance test.
</td>
<td>
EIAJ ED-4701-3 (1997)
Test method B-141A

• Temperature condition selection (Condition A unless otherwise specified)
A: 0 $^{+5}_{-0}$～100 $^{+0}_{-5}$℃ Fresh water (city water)
B: –55±5～125±5℃ Appropriate medium
C: –65±5～150±5℃
D: –200±5～150±5℃
E: $T_{stg\ max}$±5～$T_{stg\ min}$±5℃

• Condition divisions according to sample discrete mass
<table>
<tr><th></th><th>Over 1.5 kg</th><th>1.5 kg or less</th></tr>
<tr><td>Dipping time</td><td>5 minutes or more</td><td>15 s to 5 minutes</td></tr>
<tr><td>Transition time</td><td>10 s or less</td><td>3 s or less</td></tr>
</table>
• 10 cycles
• Start from normal temperature and count from the low temperature side.
</td>
<td>
IEC60749 (1996-10)
CHAPTER 3 1.2

• Temperature condition selection
(* unless otherwise specified)
0 $^{+2}_{-0}$～100 $^{+0}_{-5}$℃ *
–55～125℃
–65～150℃
–200～150℃
$T_{stg\ max}$～$T_{stg\ min}$℃

• Severity divisions
<table>
<tr><th></th><th>I</th><th>II</th></tr>
<tr><td>Dipping time</td><td>5 minutes to less than 20 minutes</td><td>15 s to less than 5 minutes</td></tr>
<tr><td>Transition time</td><td>8±2s</td><td>2±1s</td></tr>
</table>
• 10 cycles
• Start from normal temperature and count from the low temperature side.
</td>
<td>
JESD22-A106-A (1995)

• Temperature condition selection
(Condition C unless otherwise specified)
A: –40 $^{0}_{-30}$～85 $^{+10}_{-0}$℃
B: 0 $^{+2}_{-10}$～100 $^{+10}_{-2}$℃
C: –55 $^{+0}_{-10}$～125 $^{+10}_{-0}$℃
D: –65 $^{+0}_{-10}$～150 $^{+10}_{-0}$℃

• Perfluorocarbon
(Water for the high temperature side only of condition A)
• Liquid dipping time: 2 minutes or more
* The load shall reach the prescribed temperature in 5 minutes or less.
• Transition time: Less than 10 s
• The test shall not be interrupted during one cycle.
• If the number of interruptions is 10% or more of the total number of cycles, the test shall be repeated.
• 15 cycles at condition C
</td>
</tr>
</table>

Table 4-9 Reliability Test Standards Comparison Table

	Sony	EIAJ	IEC	JEDEC
Saturated Pressure Cooker Test (PCT)	121±3°C 100 $^{+0}_{-5}$%RH 2.0×10^5±10% Pa ¥ No bias ¥ Continue and perform the soldering heat resistance test. ¥ Test time: 96, 240, 504 h	N/A	N/A	JESD22-A102-B (1991) 121±1°C 100%RH 15±1 psig* ¥ No bias ¥ Endurance time A: 24 $^{+2}_{-0}$ h B: 48 $^{+2}_{-0}$ h C: 96 $^{+5}_{-0}$ h D: 168 $^{+5}_{-0}$ h E: 240 $^{+8}_{-0}$ h F: 336 $^{+8}_{-0}$ h *pounds per square inch 1psi=6895Pa 15psi=6895×15 =1.0×10^{5}Pa Standard atmospheric pressure 1atm=101325Pa ∴15psig=2.0×10^{5}Pa

Table 4-9 Reliability Test Standards Comparison Table

	Sony	EIAJ	IEC	JEDEC
Unsaturated Pressure Cooker Test	130±2℃ 85±5%RH 2.3×10^5 Pa • Continue and perform the soldering heat resistance test. • Voltage application (prescribed individually) • Test time: 200 h	EIAJ ED-4701-3 (1997) Test method B-123A • Condition selection A 110±2℃, 85±5%RH, 1.2×10^5 Pa B 120±2℃, 85±5%RH, 1.7×10^5 Pa C 130±2℃, 85±5%RH, 2.3×10^5 Pa • Voltage application if prescribed • Test time prescribed individually	IEC 60749 (1996-10) CHAPTER 3 4C • Condition selection Severity selection A 110±2℃, 85±5%RH, 1.2×10^5 Pa — 408h, 192h, 96h B 120±2℃, 85±5%RH, 1.7×10^5 Pa — 192h, 96h, 48h C 130±2℃, 85±5%RH, 2.3×10^5 Pa — 96h, 48h, 24h • Voltage application if prescribed	JESD22-A110-B (1999) Highly-Accelerated Temperature and Humidity Stress Test (HAST) • Condition selection 110±2℃, 85±5%RH, 1.2×10^5 Pa — 264^{+2}_{-0} h 130±2℃, 85±5%RH, 2.3×10^5 Pa — 96^{+2}_{-0} h • Power-on guidelines - Minimum power consumption - Apply to alternating pins as much as possible. - Apply a potential difference to the entire metal wiring. - Apply the maximum allowable voltage. - Continuous power-on when the thermal loss is 200 mW or less or when the die pad temperature rise is 10℃ or less. - Intermittent cycles at 50% duty (Power-on:Power-off = 1:1) - 1 cycle period t ≥ 2 mm: 2 h or less t < 2 mm: 30 minutes or less (t: package thickness) • The temperature and humidity until arrival at the test conditions are prescribed. • Measure within 48 h after placing in and removing from the chamber, and reapply stress within 96 h. The time provision is relaxed to 3 times for storage using bags to prevent the escape of humidity.

Table 4-9 Reliability Test Standards Comparison Table

	Sony	EIAJ	IEC	JEDEC
Soldering heat resistance (SMD) (IR reflow)	• Temperature provisions - Peak temperature: 260°C max - Preheating temperature: 170 ±10°C - Preheating time: 90 ±30 s • Baking + Moisturizing + Heating + Heating + Heating (3 times as standard) • Baking: 125 ±5°C for 24 h • Processing intervals Baking to moisture absorption: 5 minutes or less Moisture absorption to heating: 2 h or less Heating to moisture absorption: 3 h or less • Applicable only to moisture proof packaged products • The moisture absorption conditions are prescribed individually for each package. • Visual inspection of the exterior • Scanning acoustic tomography (SAT) • Cross section observation	EIAJ ED4701-4 (1998) Test method A-133B method I • Temperature provisions (including air reflow heating) I-A [- Peak temperature: 235 $^{+5}_{0}$ °C - Heating time: 10 ±3 s] ▲Sample volume less than 2,000 mm^3 I-B [- Peak temperature: 220 $^{+5}_{0}$ °C - Heating time: 10 ±3 s] ▲Sample volume 2,000 mm^3 or more • Preheating: 140 to 160°C for 90 ±30 s • Baking + Moisturizing + Heating + Heating (2 times as standard) (Moisturizing times upper limit: 3 times) • Processing intervals Moisture absorption to heating: 4 h or less Heating to heating: Until cooled to 50°C or less • Moisture absorption conditions 1) Moisture proof packaged products Perform moisture absorption in two stages during packed storage and after unpacking. The detailed conditions are as prescribed by each company. 2) Non-moisture proof packaged products A 85±2°C、65±5%RH、168±24h 〃 336±24h B 85±2°C、85±5%RH、168±24h • Visual inspection of the exterior • Scanning acoustic tomography (SAT) • Cross section observation • Electrical characteristics measurement	IEC60749 (1996-10) CHAPTER 2 2.3 • Temperature provisions - Peak temperature: 235 ±5°C - Heating time: 10 ±1 s - Preheating temperature: 150 ±10°C - Preheating time: 1 to 2 minutes (The temperature is the sample surface temperature.) • Baking + Moisturizing + Heating (IR reflow) • Baking: 125 ±5°C 6 h or more for baking at less than 125°C (The baking time at 125°C is not prescribed.) • Moisturizing conditions A 85°C30%RH 168h B 85°C65%RH 168h C 85°C85%RH 24h • Visual inspection of exterior + electrical characteristics measurement	EIA/JESD22-A-112-A (1995) • Temperature provisions - Peak temperature: 220 $^{+5}_{0}$°C - Heating time: 10 to 40 s (180°C or more for 120 to 180 s) - Temperature gradient: 6°C/s or less - Preheating temperature: 125 ±25°C - Preheating time: 2 minutes • Baking + Moisturizing + Heating + Heating • Baking: 125 $^{+5}_{0}$ °C for 24 h or more • Processing intervals Moisture absorption to heating: 15 minutes to 4 h Heating to heating: 5 minutes or more • Moisturizing conditions (susceptibility level divisions) 1) 85°C85%RH 168h 2) 85°C60%RH 168h 3) 30°C60%RH 192h 4) 30°C60%RH 96h 5) 30°C60%RH 72h 6) 30°C60%RH 48h 7) 30°C60%RH 6h • Visual inspection of the exterior • Scanning acoustic tomography (SAT) • Cross section observation • Electrical characteristics measurement

CHAPTER 5 - NOTES ON THE USE OF SEMICONDUCTOR DEVICES

5

CHAPTER 5 - NOTES ON THE USE OF SEMICONDUCTOR DEVICES

5.1 Evaluation and Assurance of Soldering Heat Resistance

Surface Mount Devices (SMD) have become widely used in recent years due to their advantages for high density mounting. However, SMD package cracking caused by thermal stress during mounting has also become a problem.

To prevent this problem, the Sony Semiconductor Network Company improves package materials and structures, and also ranks each product according to the actual package cracking resistance (Surface Mount Device rank) in order to assure the mounting conditions to customers.

This section describes the package cracking mechanism, package moisture absorption characteristics, mounting rank evaluation and assurance contents, and cracking models.

5.1.1 Package Cracking Mechanism

5.1.1.1 Package Cracking Mechanism

As shown in Fig. 5-1, IC package cracking occurs when the package absorbs moisture, the heat during solder mounting causes moisture reaching the boundary between the chip or die pad and the molded resin to gasify and expand, and stress concentrating on the edge of the chip or die pad exceeds the resin strength.

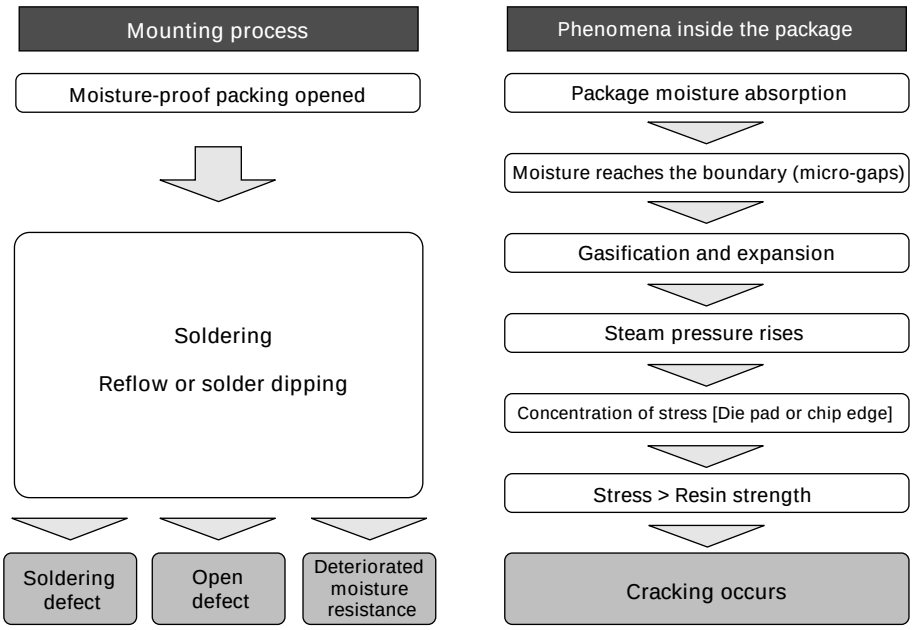


Fig. 5-1 Package Cracking Mechanism and Trouble Contents

5.1.1.2 Factors Causing Package Cracking

Package cracking generally occurs when delamination occured between the chip or die pad and the resin, and the maximum stress σ produced by the vapor pressure P inside this gap and concentrated on the midpoint of the long edge exceeds the bending strength η (T) of the resin. The uniform load model for rectangular boards with fixed edges is applied as the analysis model at this time, and the cracking conditions are expressed by Equation 5-1.

$$\eta(T) \leqq \sigma = 6k\left(\frac{a}{h}\right)^2 P \qquad 5\text{-}1$$

Where,
a: Chip or die pad short edge length
b: Chip or die pad long edge length
h: Resin thickness
k: Shape coefficient determined by b/a

Table 5-1 shows the structural, material and mounting factors corresponding to Equation 5-1.

For example, as the chip or die pad size increases, the stress increases proportionally to this square. In addition, the stress is also increased by increases in the amount of moisture absorption due to the storage environment and time after opening the moisture-proof packing.

Various methods are employed to improve package cracking resistance, such as making slits in the die pad of the lead frame, increasing the adhesive force, and using resin with low moisture absorption.

Table 5-1 Factors Causing Package Cracking

Structure	Die pad or chip size Resin thickness under the die pad or over the chip Slits	k, a h Adhesive force, dispersion of maximum stress (σ)
Materials (mold resin)	Strength (bending strength, fracture toughness value) Adhesive force Moisture absorption characteristics	$< \sigma \Rightarrow$Cracking P
Mounting	Storage atmosphere and time Soldering temperature	P P, strength, adhesive force

5.1.2 Moisture Absorption Characteristics

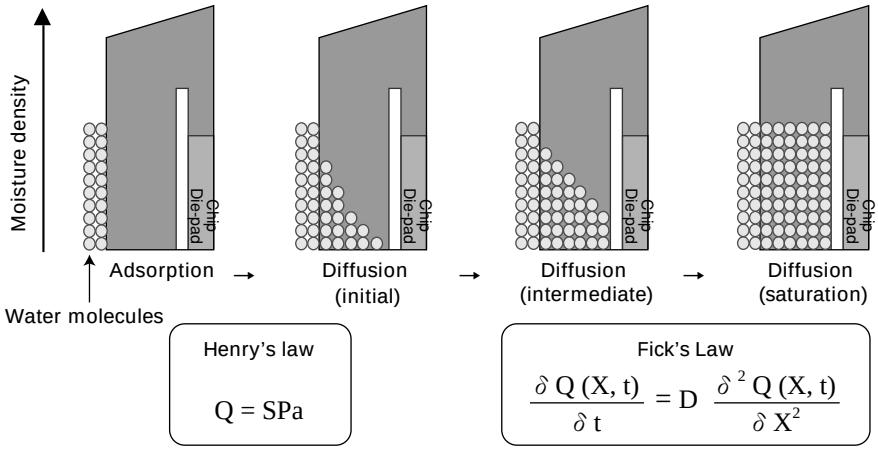
5.1.2.1 Package Moisture Absorption Mechanism

Fig. 5-2 shows the package moisture absorption image and model.

Fig. 5-2 shows the images during the course of moisture absorption. After water vapor in the air is adsorbed to the resin (Henry's Law), this moisture diffuses to the inside of the package (Fick's Law) until the moisture density inside the package reaches the saturated state.[1) 2) 3)]

Fick's Law which is applied as this diffusion model is obtained as Equation 5-2 by giving the initial and boundary conditions shown below and solving.

The moisture density at the boundary between the chip or die pad and the resin can be obtained using Equation 5-2.

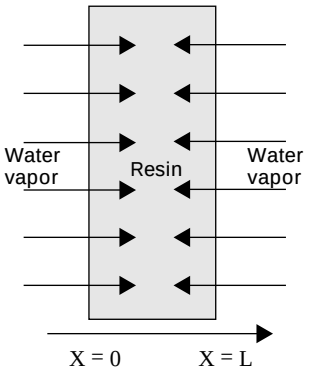


Q : Moisture density
S : Solubility coefficient
Pa: Water vapor pressure
X: Depth from the package surface
t : Time
D: Diffusion coefficient

Fig. 5-2 Package Moisture Absorption Model

Initial conditions: $Q = Q_O\ (0 \leqq X \leqq L,\ t = 0)$

Boundary conditions: $Q = Q_S\ (X = 0, L, t > 0)$
$= SPa$
$= SO \exp(Es/k \cdot T) \times Pa$



Q_O: Initial moisture density
Q_S: Saturation moisture density
S_O: Constant
E_S: Activation energy
k : Boltzmann's constant
T : Absolute temperature

Note) X=L/2; resin thickness under the die pad or over the chip

Moisture density

$$Q(X,t) = Q_O + (Q_S - Q_O)\left\{1 - \frac{4}{\pi}\sum_{n=0}^{\infty}\frac{1}{(2n+1)}\sin\left(\frac{(2n+1)\pi}{L}X\right)\exp\left(-\frac{(2n+1)^2\pi^2}{L^2}Dt\right)\right\} \quad 5\text{-}2$$

$$D = D_O \exp\left(\frac{Ed}{k \cdot T}\right)$$

D : Diffusion coefficient
D_O: Constant
Ed: Activation energy
k : Boltzmann's constant
T : Absolute temperature

Note) The activation energy symbol is normally Ea.
When obtaining the solubility coefficient: defined as Es
When obtaining the diffusion coefficient : defined as Ed

5.1.2.2 Verification of Moisture Density (Theoretical Value)

It is impossible to directly measure the moisture density inside a package. Therefore, the theoretical value obtained from Equation 5-2 is verified using the moisture absorption amount (rate) as shown below.

The package moisture absorption amount M(t) is obtained by integrating the moisture density shown in Equation 5-2 by X for [0,L],

$$M(t) = L\{Q_O + (Q_S - Q_O)(1 - \frac{8}{\pi^2} \sum_{n=0}^{\infty} \frac{1}{(2n+1)^2} \exp(-\frac{(2n+1)^2 \pi^2}{L^2} Dt))\} \qquad 5\text{-}3$$

Note that Equation 5-3 shows the amount of moisture absorbed per unit area.

Fig. 5-3 shows an example comparing theoretical moisture absorption rate values obtained using Equation 5-3 with actually measured values. The theoretical and actual values match closely, indicating that the moisture density obtained from Equation 5-2 can be accurately applied to the package moisture absorption amount.

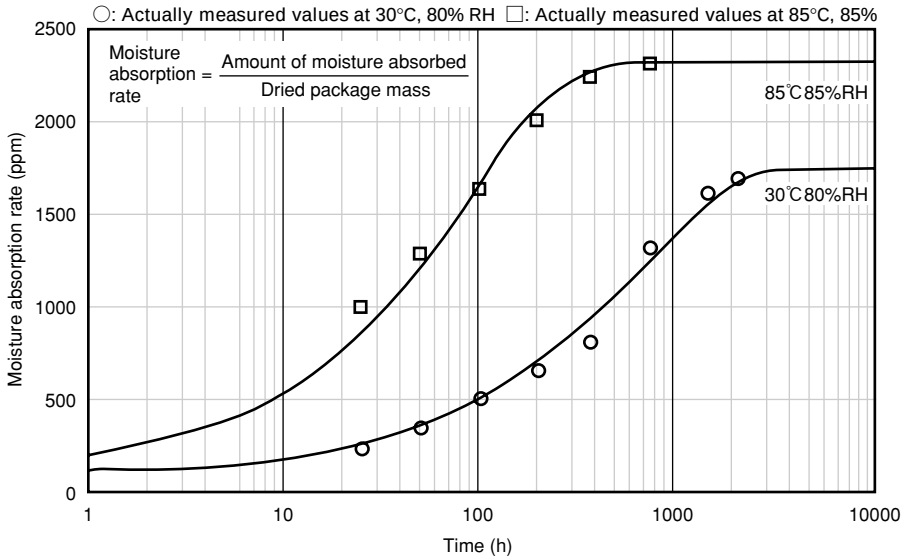


Fig. 5-3 Comparison of Theoretical Package Moisture Absorption Rate Curves with Actually Measured values for an 80-pin QFP

5.1.2.3 Package Moisture Absorption Simulations

Package cracking is determined by the moisture density at the boundary between the chip or die pad and the mold resin shown in Fig. 5-4.

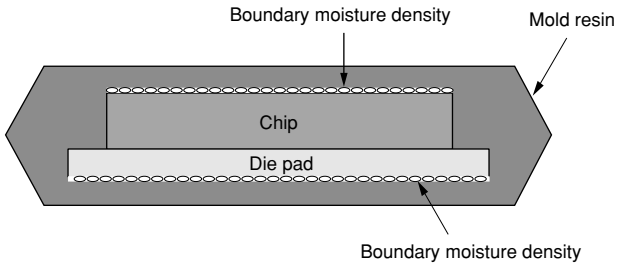


Fig. 5-4 Boundary Moisture Density Image Drawing

This boundary moisture density is obtained through simulations using equation 5-2.

Fig. 5-5 and Fig. 5-6 show simulated boundary moisture density curves for a QFP package with relatively thick resin and a TSOP package with relatively thin resin.

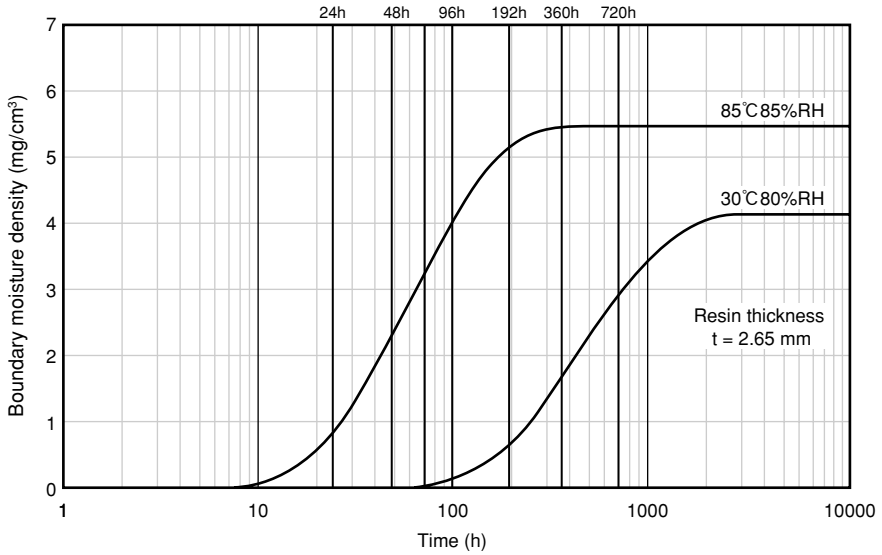


Fig. 5-5 Simulated Boundary Moisture Density Curves for an 80-pin QFP

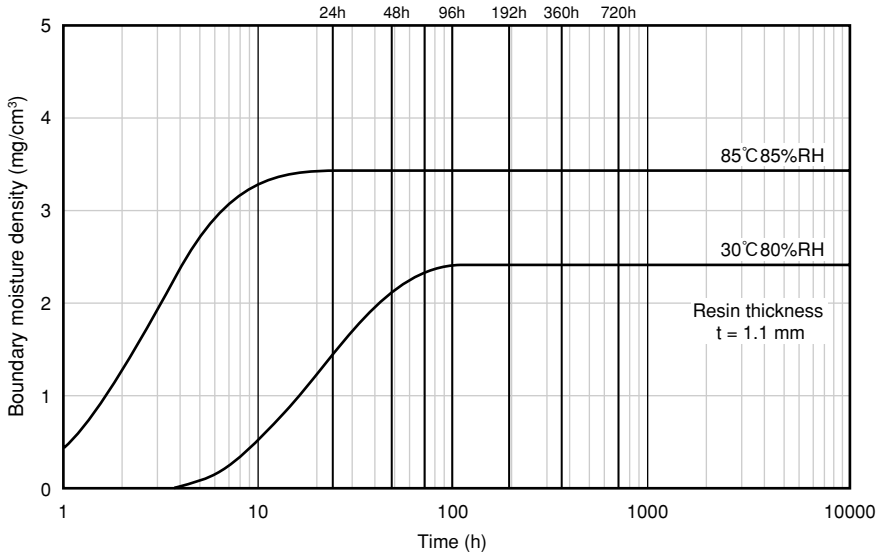


Fig. 5-6 Simulated Boundary Moisture Density Curves for a 28-pin TSOP

5.1.3 Evaluation Methods

5.1.3.1 Moisture Absorption Amount in Each Environment

Package moisture absorption environments are classified into three types as shown in Table 5-2. The first type is moisture absorption in the LSI assembly process; the second type is moisture absorption inside the moisture-proof packing, and the third type is moisture absorption in the mounting environment after opening the moisture-proof packing.

The Sony Semiconductor Network Company's LSI assembly process indoor environment is controlled to 25℃±3℃ and 50% RH±10% RH. Therefore, moisture absorption simulations use the worst conditions of 28℃ and 60% RH.

The atmosphere inside moisture-proof packing is in a balanced state due to moisture exchange between the tray, package and desiccant. The moisture-proof packing used by the Sony Semiconductor Network Company is designed to achieve an internal relative humidity of 30% RH or less when placed in an ambient temperature of 30℃. Therefore, moisture absorption simulations assume conditions of 30℃ and 30% RH inside the moisture-proof packing.

Customer mounting environments cannot be unconditionally determined, so 30℃ and 70% RH are used as the worst environment.

Table 5-2 Atmospheres and Simulation Setting Conditions

	Assembly process	Inside moisture-proof packing	Mounting environment
Atmosphere	25°C±3°C 50%RH±10%RH	30°C 30% RH or less	30°C 70% RH or less
Simulation conditions	28°C 60% RH	30°C 30% RH	30°C 70% RH
Evaluation conditions	28°C 60% RH	30°C 30% RH	30°C 80% RH

5.1.3.2 Moisture Absorption Amount Concepts and Settings for Evaluation

In the Sony Semiconductor Network Company's assembly process, the moisture absorption time is controlled or baking is performed before shipment in accordance with the actual package cracking resistance of the device.

Fig. 5-7 and Fig. 5-8 show examples of boundary moisture density simulation curves used to evaluate these two cases.

There is significant variance in the time stored inside the moisture-proof packing, so the boundary moisture density after opening the moisture-proof packing is assumed to be the worst case. That is to say when the maximum boundary moisture density at the assembly process moisture absorption control time is greater than the saturation moisture density inside the moisture-proof packing, the value (1) in Fig. 5-7 is used as the initial value in the customer mounting environment. When baking is performed before shipment, the value (2) in Fig. 5-8 is used as the initial value.

Furthermore, 30℃ and 70% RH are assumed to be the worst customer mounting environment, but the evaluation reference uses the boundary moisture density simulation curve for 30℃ and 80% RH which provides a humidity margin of 10% RH.

The boundary moisture density simulation curves in the mounting environment in Fig. 5-7 and Fig. 5-8 are used as the evaluation reference.

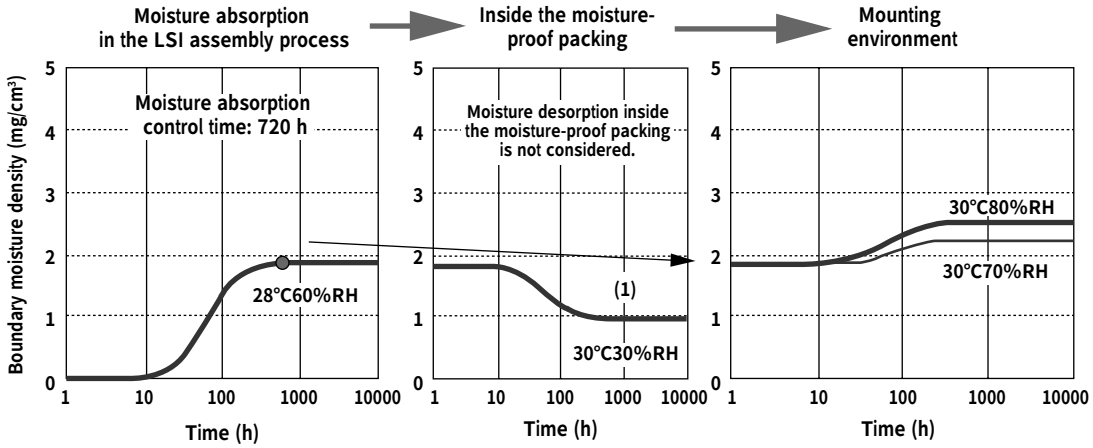


Fig. 5-7 100-pin LQFP Simulation Curve

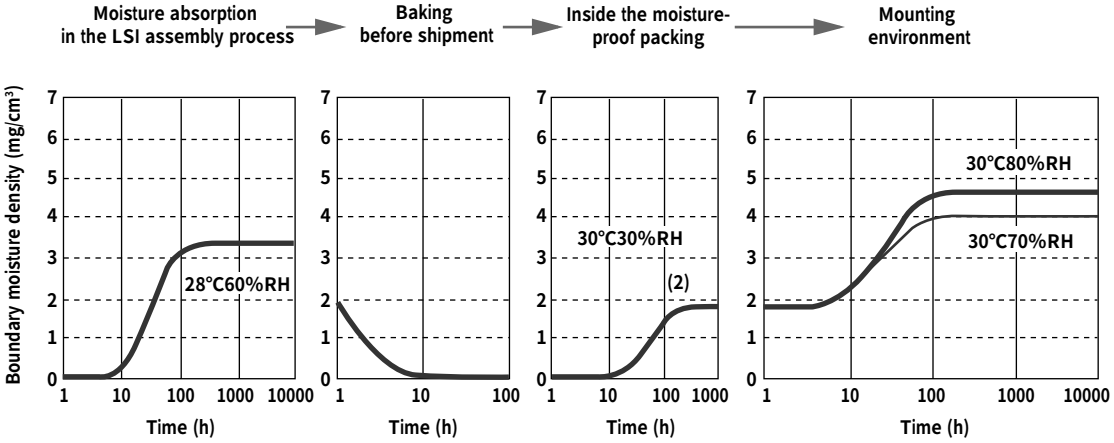


Fig. 5-8 20-pin SSOP Simulation Curve

5.1.3.3 Moisture Absorption Conditions for Evaluation

The moisture absorption conditions for evaluation sometimes use methods which accelerate moisture absorption at 85°C to shorten the evaluation time. In addition, five relative humidity conditions from 45% RH to 85% RH are prepared to realize various boundary moisture densities, and acceleration is performed at the closest condition. Fig. 5-9 shows an example of this acceleration.

Table 5-3 shows the evaluation conditions for a 64-pin QFP package as an example.

For example, 8 days×3 times is the condition where reflow is performed three times in 8 days or less. Here, moisture absorption at 30°C and 80% RH for 192 h corresponds to moisture absorption at 85°C and 55% RH for 48 h.

Also, Free×3 times indicates evaluation which assumes three times in the saturation moisture absorption state in the mounting environment after opening the moisture-proof packing. Here, the moisture absorption conditions are 85°C/75% RH/96 h, which are equivalent to the saturation moisture density of 30°C and 80% RH or more.

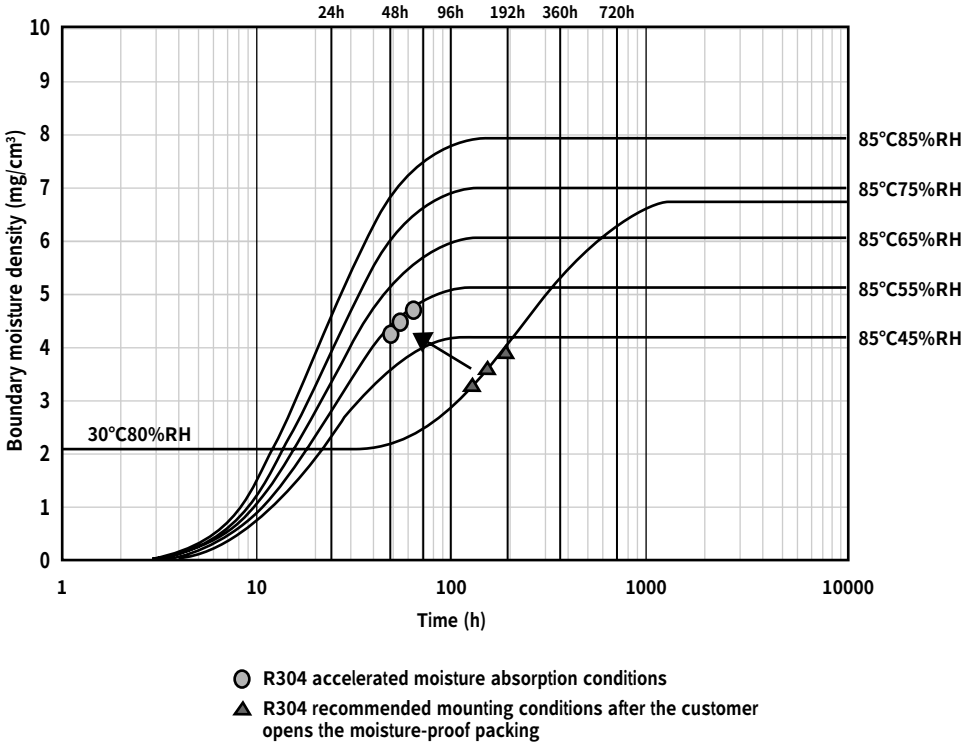


Fig. 5-9 64-pin QFP Moisture Absorption Condition Setting Simulation Curves

Table 5-3 Moisture Absorption Conditions for 64-pin QFP Evaluation

Operation limit	Moisture absorption conditions for evaluation	
	Temperature/Humidity	Time
2days × 3times (48h × 3times)	85°C／55%RH	24h
4days × 3times (96h × 3times)	85°C／55%RH	24h
8days × 3times (192h × 3times)	85°C／55%RH	48h
90days × 3times (2160h × 3times)	85°C／75%RH	96h

* The operation limit time is the time after opening the moisture-proof packing.

5.1.3.4 Evaluation Procedure

(1) Baking

The samples to be evaluated are first dried by baking, then moisture absorption is performed. Baking at 125°C for 24 h or 125°C for 48 h is selected according to the package to ensure complete drying.

(2) Moisture absorption

Moisture absorption is performed using the moisture absorption acceleration conditions set for each package and mounting rank.

(3) Heating

Fig. 5-10 shows the temperature profile for reflow heating. With the change to lead-free products, the reflow peak temperature was set at 260°Cmax with three consecutive reflow times. The assured temperature and evaluation temperature are the same, but relative humidity is provided with a 10% margin. (assured humidity: 30°C and 70% RH, evaluation humidity: 30°C and 80% RH)

Also, the evaluation conditions for solder dipping are set at three consecutive dippings at 260°C for 10 seconds to provide a relative humidity margin of 10% with respect to the assured conditions of 30°C and 70% RH.

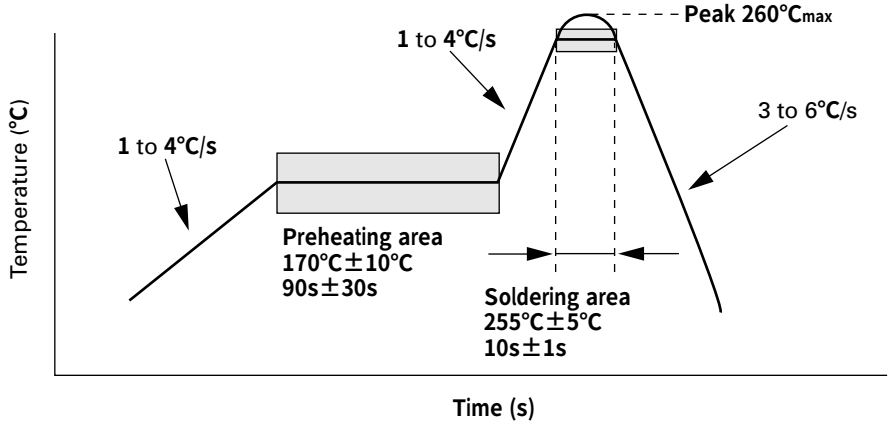


Fig. 5-10 Temperature Profile

(4) Judgment

The failure criteria are “significant delamination shall be not be confirmed with scanning acoustic tomography (SAT),” “external and internal cracking shall not be confirmed in visual inspection of the exterior or cross section polishing,” and “failures shall not occur in continued reliability tests.”

5.1.4 Surface Mount Device Rank Assurance

The evaluation results in item 5.1.3 can be broadly grouped into 4 reflow ranks and 4 solder dipping ranks, and the mounting rank (package capability) is assured according to the combination of these ranks.

These mounting ranks are codified in the following manner and presented to customers as mounting codes.

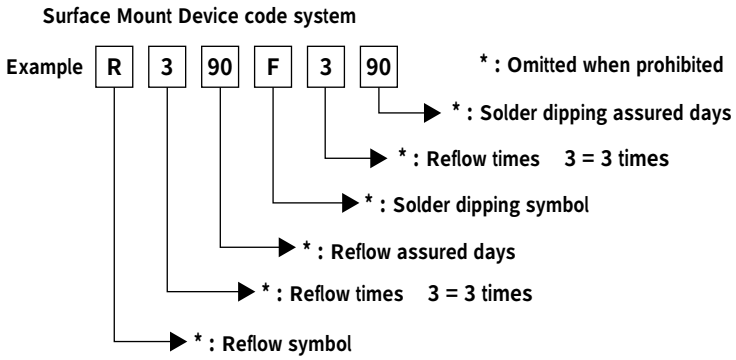


Table 5-4 shows a list of mounting codes. Note that the above example assures a storage limit of 90 days until the third reflow time after opening the moisture-proof packing. For solder dipping, the storage limit after opening the moisture-proof packing is 90 days.

Table 5-4 Surface Mount Device Code List

	SMD code		SMD code
1	R390F390	11	R304F390
2	R390F308	12	R304F308
3	R390F304	13	R304F304
4	R390F302	14	R304F302
5	R390	15	R304
6	R308F390	16	R302F390
7	R308F308	17	R302F308
8	R308F304	18	R302F304
9	R308F302	19	R302F302
10	R308	20	R302

5.1.5 Package Cracking Model

Environmental factors concerned with package cracking include the moisture absorption atmosphere and time, the solder heating method and number of times, and the heating temperature and time. With the recent diversification of mounting formats, these environmental factors are also being presented from customers in the form of various quality demands. In addition, higher heating temperatures due to the introduction of lead-free solder are becoming a large problem.

Under these circumstances, evaluation has been performed for individual mounting conditions thus far. However, this section describes a cracking model which allows simulation of cracking conditions without evaluation, and the results of verifying this model.

5.1.5.1 Package Cracking Model Concepts

Possible factors causing package cracking in evaluation of soldering heat resistance include boundary moisture density, maximum package temperature (heating peak temperature), heating time, and the number of heating times.

Tests were carried out to confirm these factors, and these results showed that the boundary moisture density and maximum package temperature factors have the largest effect.

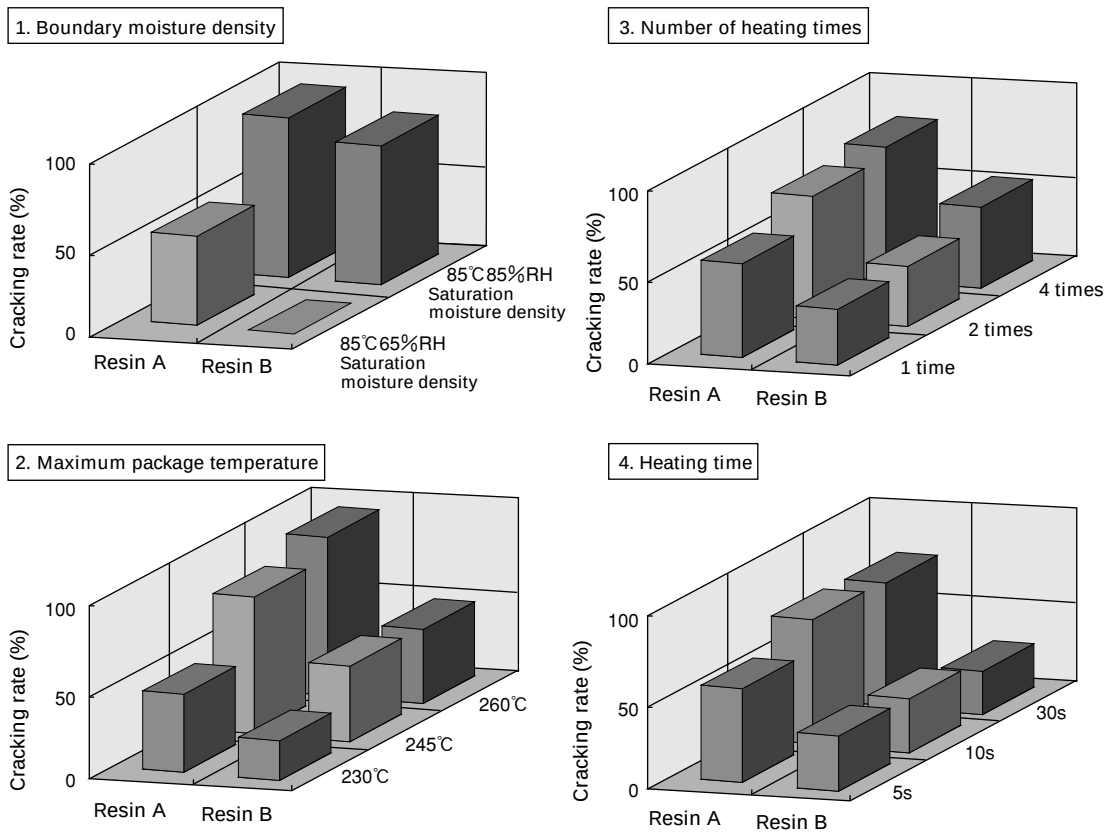


Fig. 5-11 Package Cracking Factor Confirmation Tests

As mentioned above, the main factors causing package cracking are the maximum package temperature and boundary moisture density. The package cracking conditions can be expressed by these two factors as shown in Equation 5-4.

$$Q > C \exp\left(\frac{Ea}{k \cdot T}\right) \qquad 5\text{-}4$$

Where,
Q : Boundary moisture density (mg/cm^3)
T : Maximum package temperature (K)
C : Cracking constant
Ea: Activation energy (0.4eV)
k : Boltzmann's constant

This equation is the cracking model which represents the package cracking conditions.

The cracking constant C is an inherent package constant which is determined by the package structure unit. The package cracking conditions can be obtained through simulations by obtaining this constant beforehand.

Fig. 5-12 shows the basis for deriving this model.

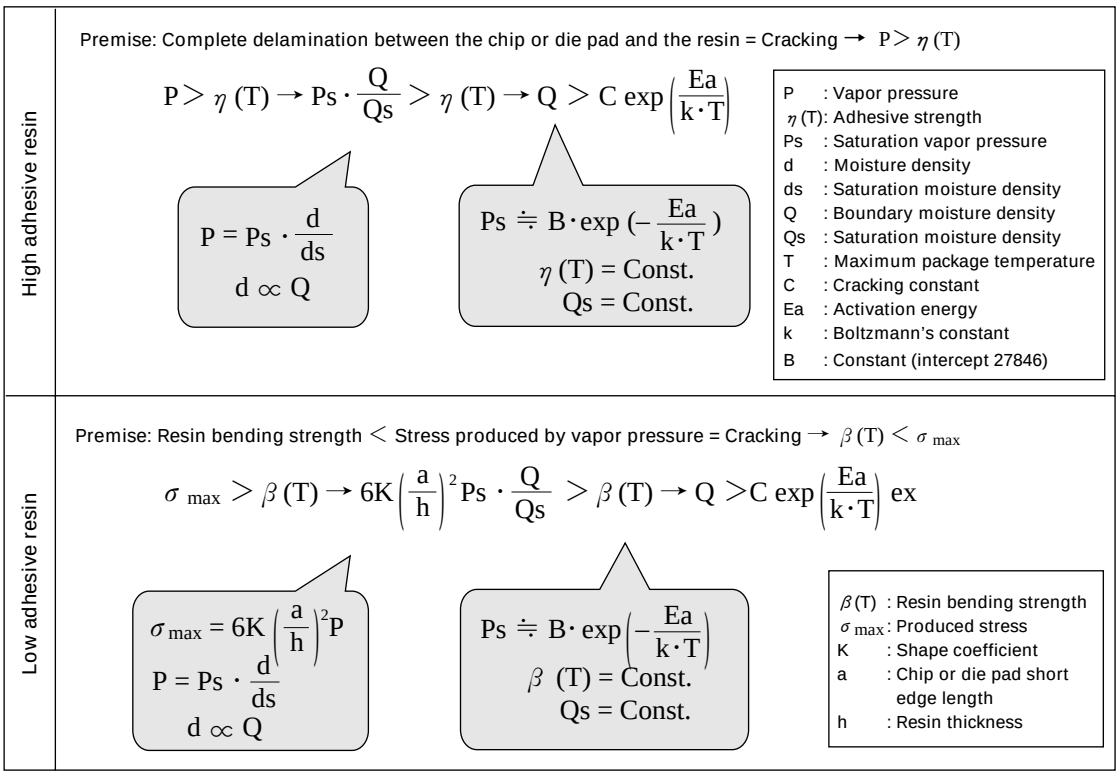


Fig. 5-12 Package Cracking Model

In addition, Fig. 5-13 and Fig. 5-14 show the results of verifying whether this model matches with the actual data. These figures show that this model can be accurately applied to actual data.

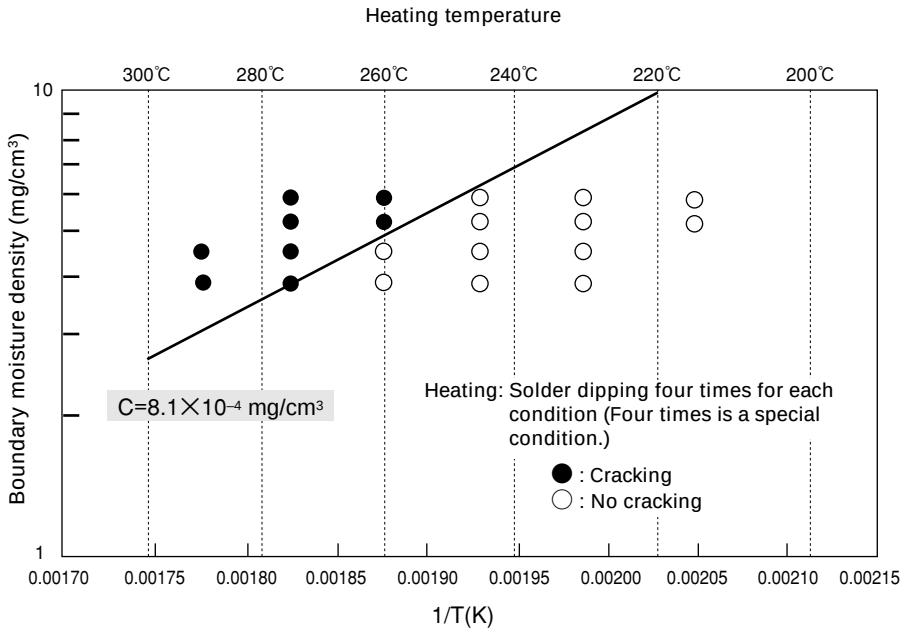


Fig. 5-13 100-pin LQFP (High Adhesive Plastic) Model Verification Test Results

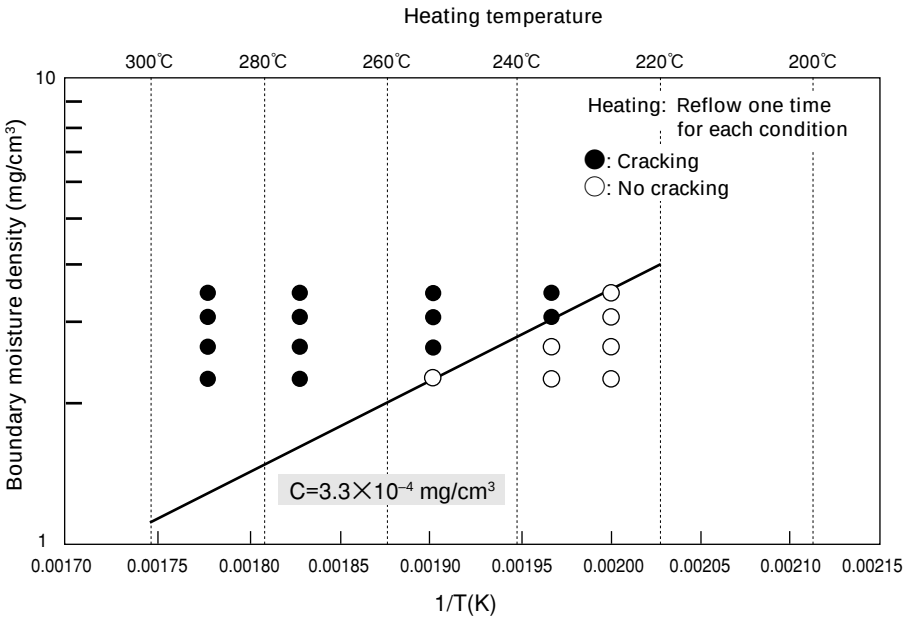


Fig. 5-14 100-pin QFP (Low Adhesive Plastic) Model Verification Test Results

5.1.5.2 Package Cracking Simulations

This section describes simulation of package cracking conditions using the package cracking model.

The cracking constant C for the 100-pin QFP package shown in Fig. 5-14 “100-pin QFP (Low Adhesive Plastic) Model Verification Test Results” is 3.3×10^{-4} mg/cm^3. For example, let us consider how far the moisture absorption conditions (boundary moisture density) must be lowered to prevent package cracking when the maximum package temperature during mounting is raised to 260℃ in order to change the soldering materials used during mounting to lead-free solder.

From Fig. 5-14, the limit boundary moisture density for a 100-pin QFP package at a maximum package temperature of 260℃ is 2.0 mg/cm^3. Thus, package cracking can be prevented by keeping the boundary moisture density below this limit.

Fig. 5-15 shows the moisture absorption simulation curve for this package.

The boundary moisture density can be kept to 2.0 mg/cm^3 or less and package cracking can be suppressed by mounting within 10 days after opening the moisture-proof packing.

In this manner, the package cracking conditions can be obtained using the package cracking model and moisture absorption simulations.

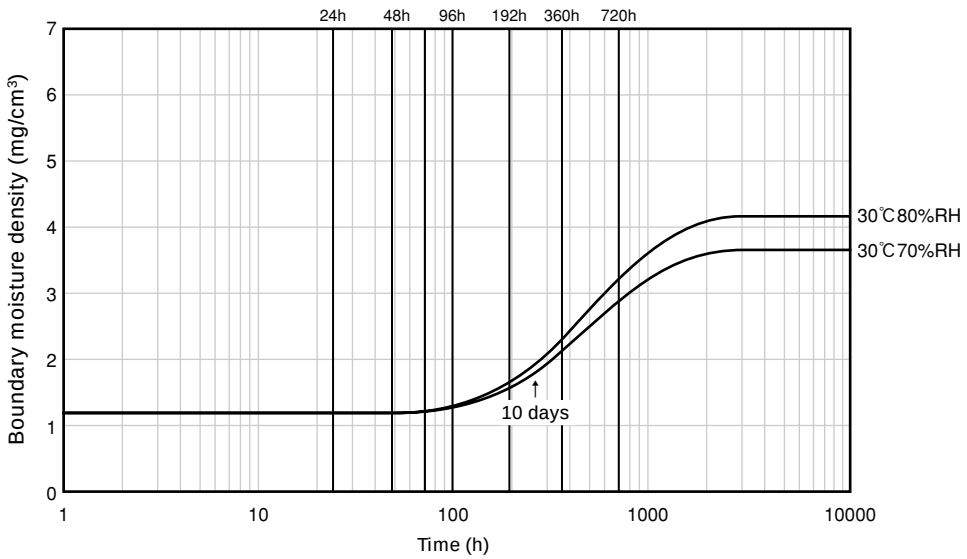


Fig. 5-15 100-pin QFP Moisture Absorption Simulation Curve

5.1.5.3 Evaluation of Capability

The package cracking capability is determined by the cracking constant C, and the capability evaluation procedure for obtaining this constant is as follows.

(1) Baking

The samples to be evaluated are first dried by baking, then moisture absorption is performed. Baking at 125℃ for 24 h or 125℃ for 48 h is selected according to the package to ensure complete drying.

(2) Moisture absorption

Moisture absorption is performed under the conditions shown in Table 5-5. The diffusion rate of moisture varies depending on the resin, so the saturation time for the two conditions shown in Table 5-5 may be set according to the diffusion and solubility coefficients.

Table 5-5 Moisture Absorption Conditions

Temperature and humidity	Moisture absorption time for each package thickness (t mm)		
	t ≦ 1.4	1.4 < t ≦ 2.0	2.0 < t
Condition 1: **85°C65%RH**	**48h**	**96h**	**168h**
Condition 2: **85°C85%RH**	**48h**	**96h**	**168h**

(3) Heating

Heating is performed by reflow or solder dipping. The respective conditions are shown below.

Reflow: Profile → Conforms to Fig. 5-10.

Peak temperature → Five conditions of 240°C, 250°C, 260°C, 270°C and 280°C

Solder dipping: Dipping time for each package thickness →

t≦1.4mm	15s
1.4mm<t≦2.0mm	30s
2.0mm<t	40s

Solder temperature → Five conditions of 240°C, 250°C, 260°C, 270°C and 280°C

The number of samples is n = 10 for each temperature condition.

(4) Judgment and calculation of cracking constant C

The failure criteria are “significant delamination shall not be confirmed with scanning acoustic tomography (SAT),” “external and internal cracking shall not be confirmed in visual inspection of the exterior or cross section polishing,” and “failures shall not occur in continued reliability tests.”

Note that cracking constant C is calculated using Equation 5-4 based on the worst conditions under which cracking does not occur.

<References>

1) Kansai Electronic Industry Development Center, Reliability Subcommittee, “Survey Report of Documents Concerning the Pressure Cooker Test” (1983)
2) Nanjo, “Materials and Moisture Handbook”, Society of Polymer Science, Polymer and Moisture Absorption Committee (1968)
3) J.Krank: “The Mathematics of Diffusion”, Oxford Univ. Press, London, (1956).
4) Etoh, Kayama, Sasaki, “A Study on SMD Soldering Heat Resistance Evaluation Methods”, RCJ Reliability Symp. (1997)

5.2 Notes on Handling for Electric Breakdown

The resistance of semiconductor devices to overvoltages, overcurrents, noise and other electrical stress is dropping due to the miniaturization of elements and wiring. Even slight voltage fluctuations or noise which were not a problem thus far are becoming increasingly likely to cause device misoperation or breakdown. This section describes countermeasures to prevent semiconductor devices from misoperating or breaking down due to electrical stress.

5.2.1 Electrostatic Breakdown

The gate oxide film thickness of MOS transistors manufactured using the latest processes has already been reduced to 5 nm or less, and the endurance voltage of these oxide films is only several voltage. Semiconductor devices employ countermeasures such as circuits to protect against the entry of external static electricity for each input/output pin to prevent static electricity from being applied to the internal transistors. However, if the transistor endurance voltage drops to several voltage or less, it becomes extremely difficult to reduce external static electricity in excess of several 100 V to the transistor endurance voltage or less using only protection circuits.

Furthermore, as device operating speeds increase, the effect of the parasitic impedance of protection circuits on operating speed cannot be ignored, and an increasing number of pins are unable to obtain the required characteristics without reducing the size of these protection circuits or eliminating them altogether. As device miniaturization and increases in operating speed progress further, it is thought that the electrostatic endurance voltage of the devices themselves will drop rapidly.

Against this background, countermeasures for preventing electrostatic breakdown are becoming even more important in processes where semiconductor devices are handled. General knowledge required to protect semiconductor devices from electrostatic breakdown during handling, methods for controlling static electricity within processes, and countermeasures against electrostatic breakdown are described below.

5.2.1.1 Basic Electrostatic Discharge Control Concepts

Basic concepts for electrostatic discharge controls in processes where semiconductor devices are handled are as follows.

(1) Designing processes and facilities which do not generate static electricity
(2) Not bringing items which are easily charged by static electricity into processes
(3) Quickly dispersing static electricity which does occur to prevent discharge
(4) Periodically checking electrostatic discharge control conditions and maintaining countermeasure effects
(5) Instilling an awareness of the need for electrostatic countermeasures in workers and process controllers

(1) Designing processes and facilities which do not generate static electricity

During process design or when investigating the introduction of manufacturing facilities, processes with effective electrostatic discharge controls can be constructed by introducing electrostatic discharge control facilities (grounds, floors, environment, etc.) and building countermeasures for preventing the generation of static electricity by friction or contact into the equipment specifications.

(2) Not bringing items which are easily charged by static electricity into processes

Electrostatic breakdown due to triboelectric charging or inductive charging can be prevented by not bringing packing materials, paper, fixtures, office supplies or other insulated objects which easily generate static electricity into processes except when absolutely necessary.

(3) Quickly leaking static electricity which does occur to prevent electrostatic discharge

Chances for electrostatic discharge (ESD) to semiconductor devices can be reduced by quickly leaking generated static electricity using methods such as grounding equipment and jigs, controlling resistance values on floors and work surface, and neutralizing charges with an ionizer. In addition, charges can be gradually leaked without causing sudden discharge and electrostatic breakdown can be prevented by changing metal parts which contact devices to materials with appropriate resistance values.

(4) Periodically checking electrostatic discharge control conditions and maintaining countermeasure effects

After implementing electrostatic countermeasures, the effects of these countermeasures cannot be maintained unless periodic checks are made and control is performed to ensure that the effects are reliably maintained.

(5) Instilling an awareness of the need for electrostatic discharge controls in workers and process controllers

Electrostatic discharge controls require knowledge and understanding of static electricity on the part of employees working in processes and process controllers. Electrostatic protective items can be even more effective at preventing electrostatic breakdown depending on the awareness of the person using them.

Electrostatic discharge controls are not a problem which can be solved simply by introducing electrostatic protective items. Ensuring thorough and consistent countermeasures and spreading general knowledge of electrostatic discharge control concepts can make process managers and workers aware of the risk of electrostatic breakdown, and is an effective means of reducing electrostatic breakdown problems within processes.

5.2.1.2 Approach toward Process Control References

In order to control electrostatic charge levels within processes, it is necessary to determine the charge level to use as the control criteria. This control reference is set based on the ESD withstand voltage of the devices handled in that process. However, among the electrostatic breakdown testing models for devices described in item 2.4.6.3, which testing method should be used to obtain the ESD withstand voltage employed as the process control reference guideline is an important issue in determining this control reference. Even if control criteria are set based on ESD phenomena which do not occur in the process, this does not necessarily mean that actual electrostatic breakdown can be effectively prevented.

Fig. 5-16 shows the relationship between charged objects present in processes and electrostatic capacity. Objects causing ESD within processes generally have different electrostatic capacity. For example, the electrostatic capacity of the human body is usually said to be approximately 80 to 200 pF [1) 2) 3) 4)], which is equivalent to the capacitance used by the human body model (HBM). In contrast to this, most items other than workers which may produce ESD with devices such as tweezers and metal parts on chip mounters such as device adsorption jigs and positioning stages have electrostatic capacity of only several pF to several 10 pF.[4)] In addition, the electrostatic capacity of most semiconductor devices is also mostly within the range of several pF to several 10 pF. (Table 5-6) When the electrostatic capacitance of charged objects becomes smaller in this manner, the accumulated electrostatic energy is lower even when charged to the same voltage, so semiconductor devices are less likely to experience electrostatic breakdown.

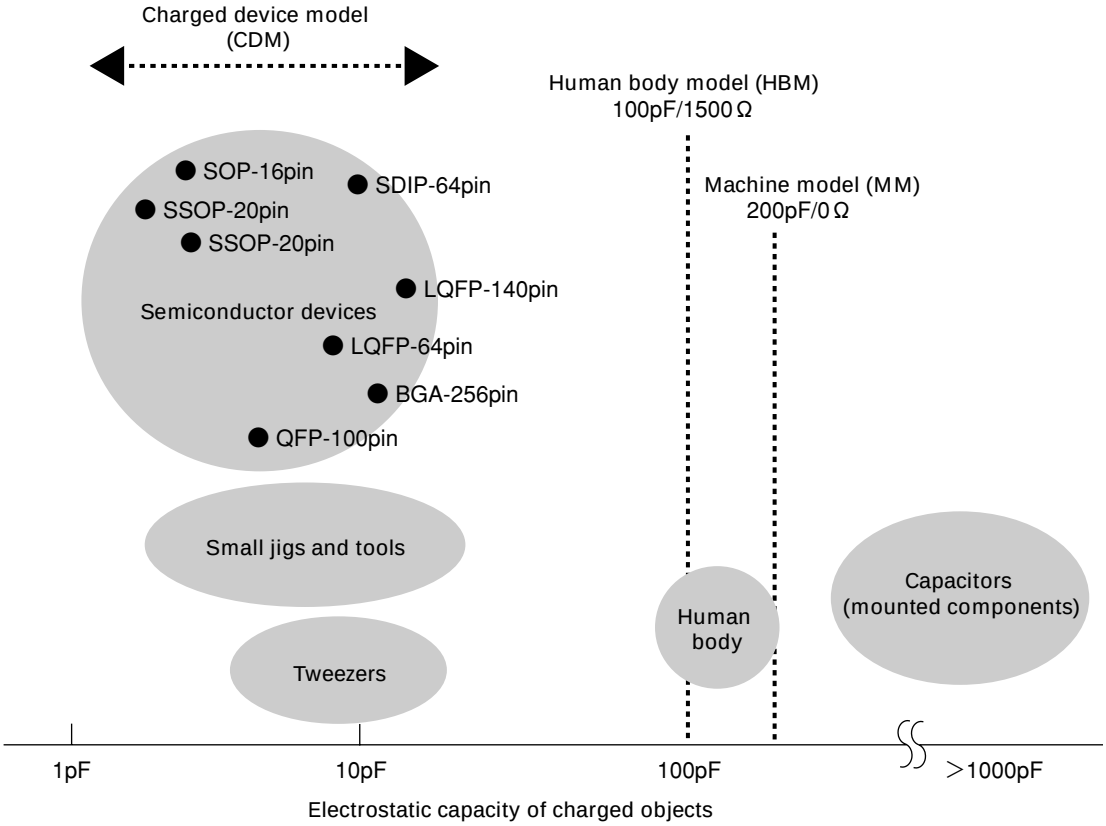


Fig. 5-16 Relationship between Charged Objects in Processes and Testing Methods from the Viewpoint of Electrostatic Capacity

Table 5-6 Device Package Electrostatic Capacity Measurement Results (when placed on a metal plate with the leads facing upwards)

Package	Electrostatic capacity (pF)	Package	Electrostatic capacity (pF)
SSOP-20pin	2.0	QFP-100pin	5.6
SOP-16pin	3.7	LQFP-140pin	13.2
LQFP-64pin	7.4	BGA-119pin	9.5
SDIP-64pin	10.5	BGA-256pin	10.6

It has been reported that failure modes produced by the discharge of static electricity accumulated in small electrostatic capacity clearly differ in most cases from failure modes when static electricity is discharged from the large capacitances (100, 200 pF) used in HBM and MM tests.[6) 7) 8)] As seen in Fig. 5-16, the charged device model (CDM) testing method which uses the parasitic capacitance of the device itself is thought to the be most suitable testing method for reproducing phenomena where static electricity is discharged from small capacitance charged objects within processes.[6) 8) 9) 10)]

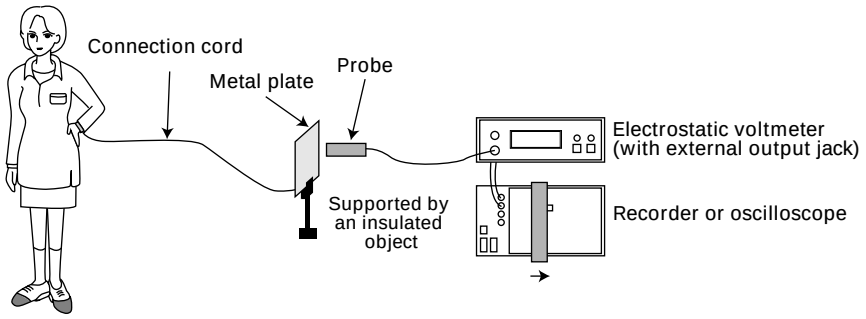
In this manner, an appropriate charge level control value for charged objects within processes should be set according to the type of charged object. Thus, it is thought that more realistic charge level control criteria can be achieved by using ESD withstand voltage data from the human body model (HBM) as a reference for workers (human bodies), and ESD withstand voltage data from the charged device model (CDM) as a reference for devices and jigs.

5.2.1.3 Basic Electrostatic Discharge Controls[11) 12)]

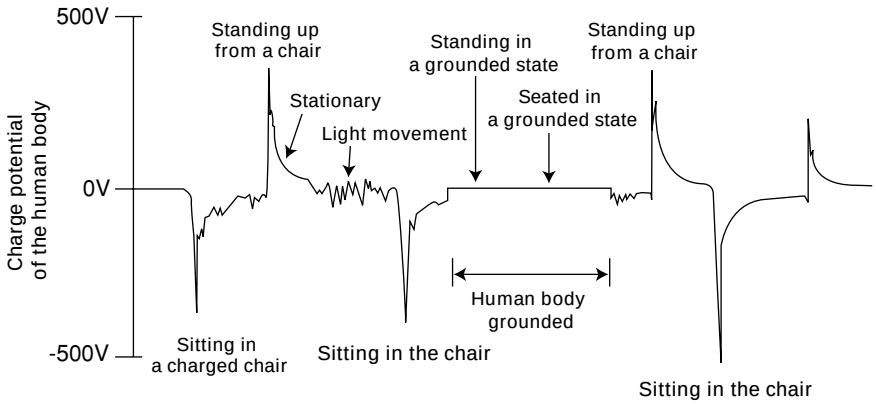
(1) Countermeasures for the human body

Workers who directly handle semiconductor devices or substrates on which devices have been mounted should wear both wrist straps and ESD protective shoes. The charge potential of the human body varies greatly according to worker movements, and the charge potential may rise sharply due to a motion such as standing up from a chair. (Fig. 5-17) Stable charge removal performance can be obtained by wearing a wrist strap adhered closely to bare skin, but the cord may be severed if a sudden load is placed on the cord during the work. If the soles of ESD protective shoes become dirty, the contact resistance between the human body and the floor increases and the prescribed leak resistance may not be obtained. Also, if a worker sitting in a chair places both feet on a footrest or other pedestal, conductivity between the floor and the human body is not obtained and the constantly required electrostatic leakage effects cannot necessarily be maintained. Therefore, safety can be most effectively assured by having workers who directly handle devices wear both wrist straps and ESD protective shoes.

Gloves and finger sacks with ESD protection should be used. In particular, the finger sacks used when handling devices with bare hands must be conductive. If the surface of finger sacks becomes charged, an electrostatic charge is induced in the device when a device is held, and the risk of the charged device model (CDM) discharge phenomenon occurring increases. (Fig. 5-18, Fig. 5-19)



(a) Measurement method



(b) Measurement results

Fig. 5-17 Changes in the Charge Potential of the Human Body

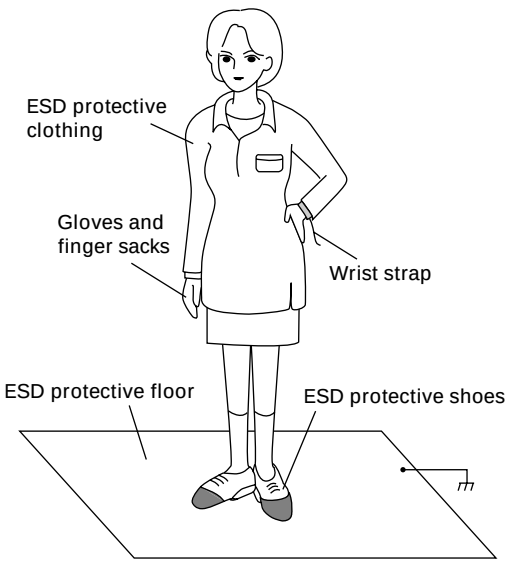


Fig. 5-18 Human Body (Worker) Countermeasures

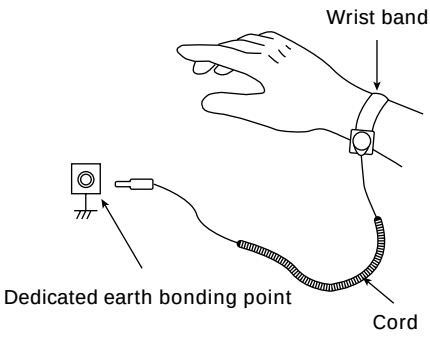


Fig. 5-19 Wrist Strap Usage

(2) Work surface

Work surfaces should be covered with ESD protective sheets (made from conductive materials or materials having electrostatic dissipative characteristics) or work tables should be made from materials having these same characteristics. Also, work surfaces must be grounded. (Fig. 5-20) Insulated objects which easily generate static electricity should not be placed on work surface. Fixtures and jigs required for work should be made from conductive or electrostatic diffusive materials, or ionizers should be used when that is not possible. The use of insulated objects for items which may contact or approach devices should be avoided as much as possible, especially during work. Also avoid working with insulated sheets or plates on worktables.

The seat and back rest surfaces of chairs that workers sit in should have ESD protective covers, or ESD protective chairs should be used. (Fig. 5-21) As shown in Fig. 5-17, static electricity with an extremely high potential may be generated momentarily when standing up from a chair.

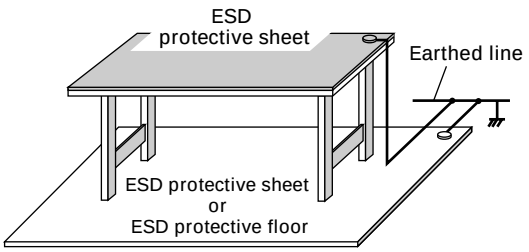


Fig. 5-20 Work surface

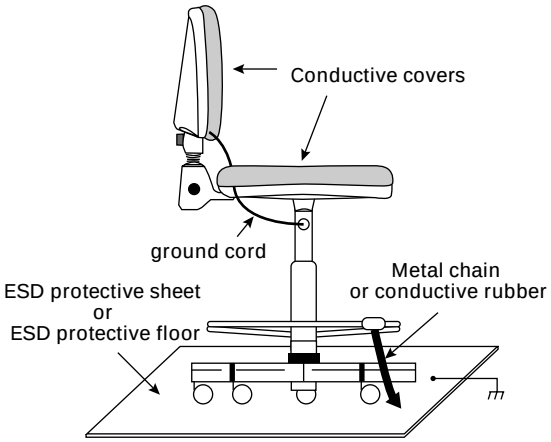


Fig. 5-21 Chair

(3) Floor

Floors in the work area should be ESD protective floors or covered with ESD protective sheets. When the entire work area floor cannot be covered, at the very least lay ESD protective sheets in the work area where workers wearing ESD protective shoes handle devices or substrates on which devices have been mounted. When laying ESD protective sheets, be sure to ground all of the sheets. (Fig. 5-20)

(4) Equipment and facilities

The frames of equipment such as mounters, solder baths and measuring instruments, and facilities such as belt conveyors must be grounded. (Fig. 5-22) Metal parts which are isolated from the grounded frame by insulating material and which may contact devices should be grounded individually. Insulating material parts which may contact or approach devices should be changed to materials with electrostatic dissipative characteristics, or charges should be eliminated using ionizers.

Both the body and tips of electric screwdrivers, soldering irons and other tools should be grounded. Otherwise, electric over stress (EOS) breakdown may occur if there is an AC voltage leak.

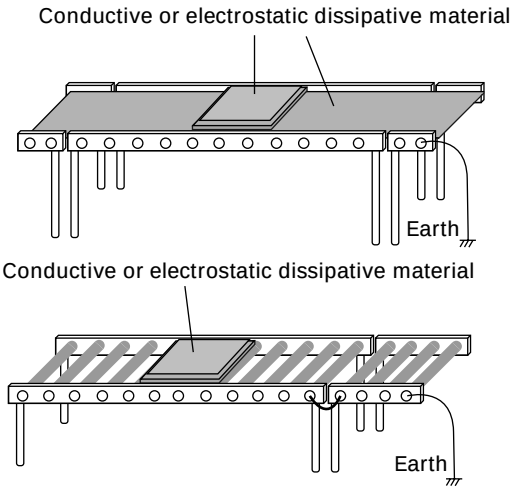


Fig. 5-22 Belt Conveyor

(5) Environment

It is generally considered difficult for static electricity to occur at higher humidity (moisture density in the air). However, rather than static electricity being difficult to generate, what actually happens is that the proportion of the generated charge that leaks due to moisture adhered to the surface increases, with the result that charging appears difficult. In process humidity control it is important to maintain a humidity environment which makes it difficult for static electricity to occur. In actual processes, however, heat generation by equipment and other factors create spaces with locally high temperatures (low relative humidity). Furthermore, substrates which generate heat when the power is on, components packed in plastic trays and bags, and products stored for long periods inside dry warehouses may not necessarily always be in a condition which inhibits the generation of static electricity. Therefore, it is extremely dangerous to think that static electricity can be uniformly inhibited by increasing the humidity, or that other electrostatic discharge control can be omitted. Humidity environment control must be understood only as an auxiliary electrostatic control.

(6) Storage and transport

Semiconductor devices should be stored in the packing format for shipment. Correctly storing devices in the same ESD protective packing materials as when shipped reduces the risk of electrostatic breakdown even when devices are handled during storage.

In addition, substrates on which devices are mounted must be stored in containers or on storage shelves made from conductive or electrostatic dissipative material. (Fig. 5-23, Fig. 5-24) At this time, the use of insulated partitions or storage in plastic insulated bags should be avoided. Mounting substrates are made from insulating materials, so if substrates become charged by vibration or rubbing during storage or transport or if they are placed near charged objects, an inductive charge may be generated in the substrate wiring pattern, and may discharge from the connectors during measurement or assembly and damage the device.

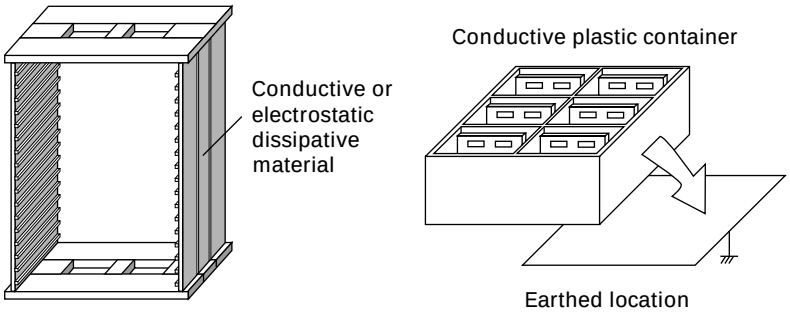


Fig. 5-23 Boad Storage Container

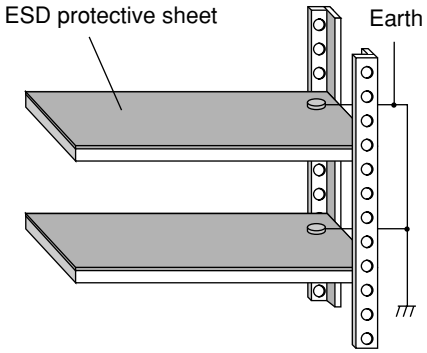


Fig. 5-24 Storage Shelf

(7) Components other than devices

Many components other than semiconductor devices which are mounted on boads become electrostatically charged during boad mounting. Components such as condensers, LCD pannels and flexible connectors which have capacitances capable of accumulating static electricity may cause ESD during boad mounting and damage devices.

Parts boxes used to store these components and delivery packing must have electrostatic countermeasures. (Fig. 5-25) Workers should be aware that some mounted components other than devices can also carry electrostatic charges, and countermeasures must be taken to prevent these components from causing ESD during boad mounting.

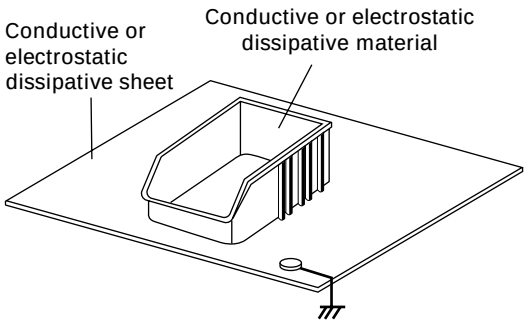


Fig. 5-25 Parts Box

(8) Eliminating charges using an ionizer

Ionizers are charge elimination equipment which generate corona discharge by applying a high voltage to the tip of a discharge electrode, and neutralize static electricity with the generated ions. Ionizers are an effective means of eliminating static electricity from insulating material which cannot be discharged by grounding. Unlike charges on metal, there is no risk of charges on insulating material being discharged to and damaging devices. However, these charges may generate inductive charges in devices and metal parts. Ionizers are effective when using insulating material near devices.[13)]

(9) Clothing

Workers should make efforts to wear clothing made from materials which do not generate static electricity. Clothing made from materials which easily generate static electricity may induce strong static electricity in human bodies with movement.

(10) Characteristics required of ESD protective items

The values given in the table below are references for the characteristics required of main ESD protective items. Even when the characteristics noted in the Specifications satisfy the required standards, the effects should be thoroughly verified before selecting ESD protective items for introduction.

Table 5-7 Characteristics Required of Main ESD Protective Items[14)]

ESD protective item	Surface resistivity Rs (Ω・cm) Resistance Rp (Ω)	Resistance value to GND Rg (Ω)
Floor	—	$<1\times10^{9}$
ESD protective sheet	$1\times10^{4}<Rs<1\times10^{10}$	$1\times10^{5}<Rg<1\times10^{9}$
ESD protective shoes (when worn)	—	$5\times10^{4}<Rg<1\times10^{8}$
Wrist strap (cord)	$7.5\times10^{5}<Rp<5\times10^{6}$	—
Wrist strap (when worn)	—	$5\times10^{4}<Rg<1\times10^{8}$
Chair	—	$<1\times10^{10}$

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11) “Guidelines on Technology for Avoiding Electrostatic Damage to Semiconductor Devices”, Reliability Center for Electronic Components of Japan (1995)
12) “Report on the Results of Investigative Findings on the Standardization of Device ESD Resistance Tests”, Reliability Center for Electronic Components of Japan (1994)
13) “Utilization Guide for Ionizers Used at Semiconductor Device and other Production Sites”, Reliability Center for Electronic Components of Japan (1995)
14) IEC 61340-5-1 (1998)

5.2.2 Strong Electric and Magnetic Fields

Strong external electromagnetic fields are generally not the direct cause of device failure. However, when devices are exposed to strong magnetic fields, the impedance may change, the leak current may increase, or other abnormal phenomenon may occur due to polarization of the package plastic materials or inside the IC chip.

In addition, if power supplies or parts which generate high voltages are located near devices, large noise in the power supply or ground lines may cause circuits to misoperate or the IC to generate noise.

To prevent these external electromagnetic interferences from impeding circuit functions, circuit layout patterns and component arrangements on printed substrates are optimized and shielded wires are used. In addition, care must be given to the set design such as changing mounting locations or providing electric and/or magnetic field shielding as necessary.

5.2.3 Overvoltage Breakdown (EOS Breakdown)

Failure modes where overvoltage or overcurrent other than static electricity causes breakdown are called overvoltage breakdown or electric over stress (EOS) breakdown. Electric over stress has various causes, but device failure is generally caused by the application of pulse type electric over stress called surge. Causes of surge include equipment power-on/off, relay switching, discharge from capacitive loads, lightning surge due to lightning strikes, etc.

The surge-induced EOS breakdown mechanism differs according to the type of applied surge, but applying voltage in excess of the ratings to the device power supply or input/output pins causes junction breakdown inside the device or the phenomenon where parasitic transistors are activated. At this time, if an overcurrent flows and the energy consumed by the aluminum wiring and transistors exceeds the wiring or junction endurance level, the wiring may melt or junctions may suffer thermal breakdown.

Countermeasures against EOS breakdown include inserting voltage clamp diodes or capacitors to the power supply and input/output pins on the substrate to prevent surges from entering the inside of the substrate. In addition, noise countermeasures must also be taken for measuring instruments used to adjust substrates within processes.

5.2.4 Handling of High Frequency Devices

As semiconductor devices incorporate more advanced functions and performance, the device structures are being further miniaturized with higher densities, and oxide films and wiring layers are becoming thinner. This has resulted in an intrinsic drop in electrostatic strength.

To increase the electrostatic strength, countermeasures such as adding electrostatic protection circuits to device input/output pins are generally taken, but this also has the drawback of causing characteristics degradation.

Particularly for high frequency and high speed devices, adequate electrostatic countermeasures cannot be taken for some pins in order to satisfy the required performance.

Therefore, thorough countermeasures must be taken in all aspects from device storage and transport to set mounting, inspection and other work environments, and also for handling during work.

5.2.5 Latch-up

Latch-up is the phenomenon where overvoltage or current stress such as static electricity or noise entering from an external source triggers the parasitic thyristors in CMOS devices and creates a short circuit between the power supply and GND.

The latch-up phenomenon occurs in the operating condition (the condition with the supply voltage applied), but as long as voltage stress which exceeds the device ratings is not applied, there is little or no risk of latch-up occurring within the normal operating voltage range. Latch-up which occurs randomly while using electronic equipment is thought to be mostly caused by the entry of stress in excess of the ratings to products incorporating semiconductors or the occurrence of this type of situation during operation. Possible causes of latch-up are as follows.

(1) Entry of static electricity from an external source

When static electricity enters an operating device which is mounted on a substrate, the discharge current passes through the input/output pin protective elements and flows to the power supply or GND wiring. In consideration of discharge from human bodies, the peak current value that flows at an ESD of several kV can reach several A to several ten A. If this current flows to the substrate power supply or GND wiring, the power supply or GND potential fluctuation may reach several V and exceed the device ratings. If this voltage fluctuation occurs during device operation, the junctions inside the device may break down and cause latch-up.

Portable electronic equipment (cellular phones, camcorders, laptop computers, portable data terminals, digital cameras, etc.) have spread rapidly in recent years, and the frames of these electronic equipment which are frequently and directly touched by people are not grounded. Therefore, these equipment are easily affected by supply voltage fluctuations caused by ESD from human bodies, and have a high risk of latch-up. Furthermore, in order to achieve higher speeds, compact size and low power consumption, these products use many devices manufactured by the latest processes, so the voltage margin against latch-up is becoming even stricter due to lower supply voltages and junction withstand voltages.

(2) Entry of lightning surge

Semiconductor devices used in communications facility or power supply facility equipment may experience latch-up due to lightning surge entering via communication cables or transmission lines. Household electronic products may also experience latch-up due to lightning surge entering through utility poles, transmission cables or telephone lines, etc.

(3) Electromagnetic susceptibility (EMS)

If sources of electromagnetic noise (car engines, cathode ray tubes, ESD) are present around electronic equipment, noise induced by sudden changes in the electromagnetic field may cause latch-up.

(4) Live wire insertion or removal

When performing maintenance or repair work on operating systems, depending on the manner in which the connectors are connected, voltage may be applied to the input/output pins before power is supplied to the substrate when a substrate is inserted with the system in the operating condition. At this time, the input/output pin potential momentarily becomes higher than the supply voltage, causing an influx of current from the pin and resulting in latch-up.

(5) Supply voltage application sequence for multi-power supply devices

In devices with multiple different power supplies, the potential of certain pins may rise above the supply voltage depending on the sequence in which the supply voltages are applied, and this may cause latch-up. Care must be taken for the order in which the power supplies are applied to the device for devices which use multiple power supplies.

Latch-up caused by these types of external factors can be suppressed by taking countermeasures to prevent the entry of surges and noise which serve as the respective triggers. Effective countermeasures for static electricity or surges which directly enter devices include inserting surge countermeasure diodes, capacitors or other elements to the substrate entrances which are the entry routes, or using substrate power supply and GND wiring patterns which are resistant to potential fluctuations and noise. In addition, lowering the power supply and GND wiring impedance, suppressing potential fluctuations due to sudden currents, and separating the power supply and GND wiring of circuit blocks which are susceptible to external surges from other circuits are also effective countermeasures. Countermeasures for the power supply application order include inserting capacitors or taking other measures to delay the respective rise timings, etc.

Electromagnetic noise requires shielding countermeasures to prevent electromagnetic waves from entering electronic equipment or the use of wiring patterns which are resistant to induction by electromagnetic fields. When sources of electromagnetic noise are present inside equipment, countermeasures must be taken for the noise source or the power supply and GND wiring must be separated, etc.

5.2.6 Thermal runaway

Thermal runaway is the phenomenon where positive feedback increases the power due to the temperature characteristics of the IC internal circuits, causing the temperature to rise without limit and resulting in failure. Most failure after mounting is thought to be caused by thermal runaway. In addition to thermal runaway caused by local heat generation in the device, thermal runaway may also occur depending on the heat radiation structure in power devices. Therefore, special care must be given to heat radiation design.

5.3 Notes on Handling for Mechanical Breakdown

Devices should be handled carefully. Devices may be damaged by dropping or shocks, so care should be taken to keep mechanical vibrations and shocks to a minimum.

Devices are comprised of chips, bonding wires, external pins, radiation fins, mold resin and other elements, and the mechanical strength and coefficient of thermal expansion of each component material differ. Therefore, mechanical breakdown may occur in various cases such as when forming or cutting external pins, mounting devices on printed substrates, washing, or attaching radiation fins.

These mechanical external forces may cause package or chip cracking, or delamination at the boundary between the mold resin and the external pins which results in degraded moisture resistance.

5.3.1 Forming and Cutting External Leads

When mounting semiconductor devices onto printed substrates, care should be taken not to apply excessive force to the external leads when forming or cutting the external leads beforehand. (Fig. 5-26)

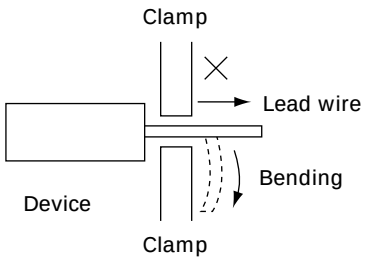


Fig. 5-26 Notes on Forming or Cutting External Leads

(1) When bending external leads, clamp the external lead between the point at which the lead is to be bent and the package body. Do not bend external leads while holding the package body.
When using a metal mold, also do not apply stress to the package body.
Likewise, when cutting external leads, do not apply stress to the package body.
(2) Do not repeatedly bend external leads.
(3) Do not bend external leads in the thick direction of the lead.
(4) Care should be taken as the external lead plating may be damaged depending on the bending method.

5.3.2 Mounting Devices on Printed Substrates

When mounting semiconductor devices on printed substrates, care must be taken not to apply excessive stress to the external leads. If the external leads bend or float, good solder contact with the printed substrate may not be obtained, resulting in a mounting defect. (Fig. 5-27)

(1) The external lead attachment interval on the printed substrate should match the external lead interval of the device.
(2) When inserting the device into the printed substrate, avoid forcibly inserting the device.
(3) Leave an appropriate gap between the semiconductor device and the printed substrate.
(4) When mounting a surface mounted type device on a printed substrate, if the external leads are deformed or float, good solder contact with the printed substrate may not be obtained, resulting in a mounting defect. Therefore, care must be taken not to deform the external leads.
(5) When mounting semiconductor devices on printed substrates using mounting sockets, use an appropriate socket for each package.

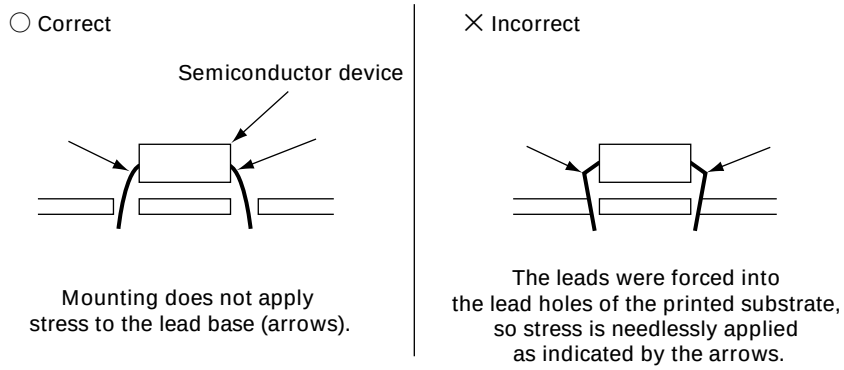


Fig. 5-27 Notes on Printed Substrate Mounting

5.3.3 Washing Methods

In principle, flux must be removed after soldering. Otherwise, flux residue may affect the reliability of components, printed substrate wiring or solder junctions.

(1) Ultrasonic washing offers excellent washing effects in a short time, but care must be given to the applied frequency, output, washing time, and to avoid direct contact with the device and printed substrate in order to prevent device breakdown.
(2) Do not rub marked surfaces during washing or while detergent has adhered to the device, as this may cause the marking to disappear. Care should also be taken as the marking may disappear if washing is performed for a long time.
(3) Even when using solvents or washing just with water, washing should be performed so that sodium, chlorine and other reactive ions do not remain. Also, be sure to dry all parts thoroughly.
(4) When using solvents, be sure to take into account public environmental standards and safety standards.

5.3.4 Attaching Radiation Fins

Care should be taken for the following points when attaching radiation fins to devices.

(1) Use an appropriate attachment method so that excessive stress is not applied to the device.
(2) Take care for flatness so that there is no burring or unevenness on radiator fins.
If radiator fins are inappropriate, sufficient radiation effects may not be obtained, or forced attachment may cause device characteristics degradation or mechanical breakdown.
(3) When there are two or more radiator fin mounts, first lightly pre-tighten all of the mounts, then tighten to the prescribed torque.
(4) Do not attach radiator fins to a semiconductor device after the device has been mounted on a substrate. Otherwise, excessive stress may be applied to the semiconductor device depending on the manner in which the device is mounted on the substrate. First attach the radiator fins to the semiconductor device, and then mount the device on the substrate.
(5) Thermal conductivity is generally improved by coating the junction between radiator fins and semiconductor devices with silicon grease. In this case be sure to apply an even coat.

5.3.5 Handling of CCD Area Sensors and CCD Linear Sensors

(1) Handling during mounting (adhesion)

Remain within the following limits when applying a static load to packages during mounting or other work. (Fig. 5-28)

① Compressive force: 39 N/face

(Do not apply any load 0.7 mm or more inside the outer perimeter of the glass surface.)

② Shearing stress: 29 N/face

③ Tensile force: 29 N/face

④ Twisting torque: 0.9 N·m

However, the following limits apply to area sensors with plastic packages. (Fig. 5-29)

① Compressive force: 50 N/face

② Twisting torque: 1.2 N·m

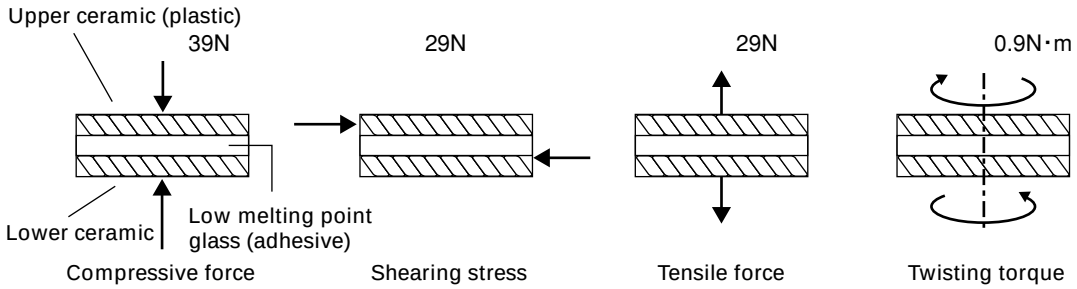


Fig. 5-28 Allowable Stress to Ceramic Packages

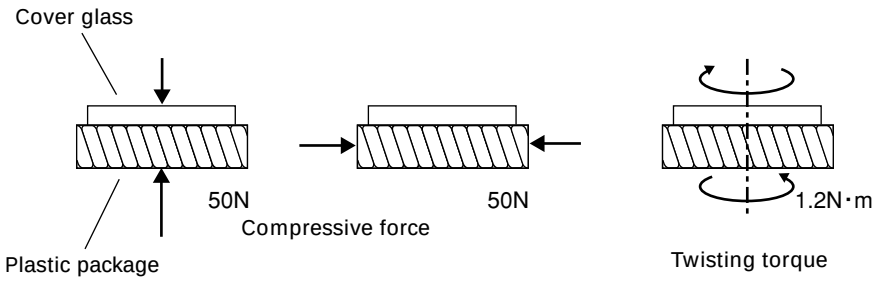


Fig. 5-29 Allowable Stress to Plastic Packages

If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for mounting, use either an elastic load, such as a spring plate, or an adhesive.

If the leads are bent repeatedly or metal, etc., strikes or rubs against the plastic package surface, the plastic may chip or fragment and generate dust.

In particular, the upper and lower ceramic (or the plastic and ceramic) of CERDIP packages and linear sensor plastic packages are adhered using low melting point glass (or adhesive). Care should be taken for these packages, as the following types of handling may cause the low melting point glass (or adhesive) to crack.

(1) Applying a local load or mechanical shock to the low melting point glass (or adhesive) using tweezers or other pointed tool.
(2) Twisting the upper and lower ceramic (or the plastic and ceramic) with the low melting point glass (or adhesive) as the fulcrum.

(2) Removing dust and dirt

The glass surfaces of elements must be kept constantly clean. Care should be taken not to either touch glass surfaces by hand or have any object come in contact with glass surfaces.

Dust or dirt adhering to glass surfaces should be removed by the following procedures.

- Dust or dirt adhered to glass surfaces

  Blow off dust or dirt with an air blower. For dirt stuck through static electricity, ionized air is recommended.
- Dirt or grease stains which cannot be removed by the above methods

  Wipe away the dirt with a cotton bud moistened with ethyl alcohol in the order of ① and ② below.

① For the effective area and surrounding glass surfaces, incline the cotton bud (45° or less) and wipe away the dirt in the same direction as the lead arrangement as shown in Fig. 5-30.

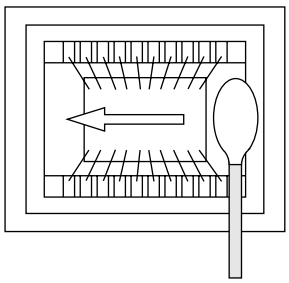


Fig. 5-30 Wiping the Glass Surface

② For the gap between the sealing glass and the package, hold the cotton bud straight up and wipe away the dirt as shown in Fig. 5-31.

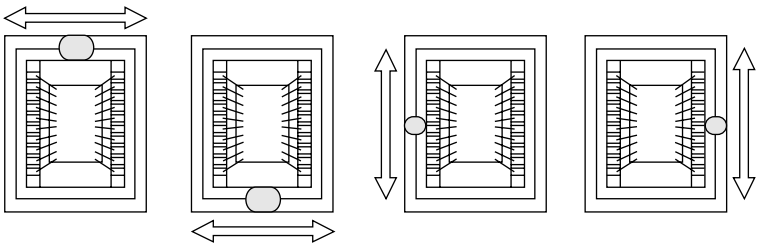


Fig. 5-31 Wiping the Sealing Glass Surface

[Notes]

- Do not wipe glass surfaces with a cotton bud if dust or dirt have not adhered.
- In step ①, do not allow the cotton bud to contact the glass edges or the ceramic surface.
- Do not reuse cotton buds.

(3) Handling of magazine-packed products

- Removing products

  When removing products from magazines, remove the products by the following procedure to prevent lead bending due to dropping or other problems.

① Remove the rubber stopper. Be careful so that the products do not fall from the magazine at this time.

② Incline the magazine at approximately 30° over a conductive mat and let the products slide slowly out of the magazine. (Be careful as the products will fly out with great momentum if the magazine is inclined too much.)

Also, keep the magazine outlet at a height of 5 mm or less from the mat while removing the products. (Fig. 5-32)

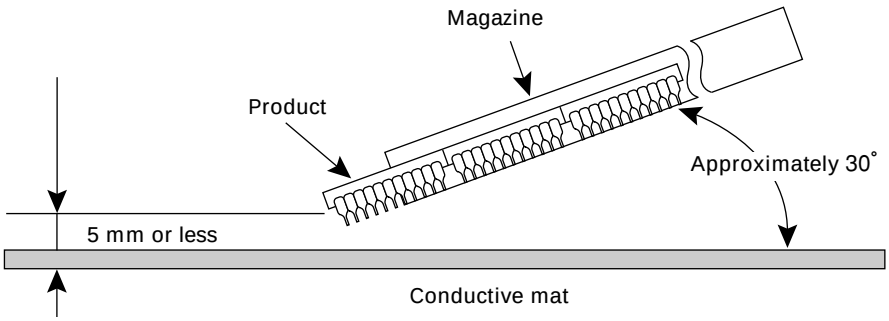


Fig. 5-32 Removing Products from Magazines

- Storing odd lots of products after opening magazines

  After products have been removed, magazines may contain an odd lot of products. When storing these odd-lot magazines, inserting a rubber spacer of an appropriate length into the magazine and then fitting a rubber stopper is recommended to prevent the products from moving inside the magazine and being damaged by mechanical shocks, etc. (Fig. 5-33)

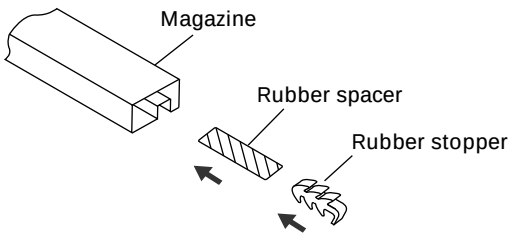


Fig. 5-33 Storing Odd Lots of Products in Magazines

5.4 Notes on Handling to Prevent Thermal Breakdown

Semiconductor devices have structures which combine a silicon chip, plastic encapsulating materials, copper and other metallic lead frames, and other materials, each of which have completely different thermal properties. In particular, when the plastic materials are exposed to high temperatures such as during soldering, the moisture accumulated in the plastic rapidly turns into steam and causes package cracking. The causes of delamination between the adhered portions of component materials, disconnection of conductors and other problems brought about by repeated heat stress are as follows.

(1) The mechanical strength drops significantly at high temperatures.

(2) Moisture in the air is absorbed and accumulated.

This section describes general precautions, particularly for product mounting, to prevent this type of thermal breakdown of devices.

5.4.1 Soldering

(1) Precautions during soldering

Semiconductor devices generally should not be left for long periods at high temperatures.

Even during soldering, regardless of whether hand soldering or reflow methods are used, if the soldering temperature is high and the soldering time is long, the device temperature may rise and result in degradation or breakdown. Therefore, soldering should be performed at the lowest temperature and shortest time possible.

(2) When soldering through hole device (THD) packages with a wave solder vat

This method dips the portions of the package lead pins to be soldered into the liquid surface of a jet solder bath. However, note the package may be damaged if the jet solder contacts the package body, so care should be taken not to allow the solder directly contact the package body.

In addition, when using a wave solder bath, the bottom of the substrate is heated by the solder heat, so substrate warping may occur due to the temperature difference between the top and bottom of the substrate.

If soldering is performed with the substrate in the warped condition, the substrate attempts to return to its original condition when it is taken from the solder bath, so excessive stress may be applied to the leads and package, causing solder junction cracking and lead and package damage.

Therefore, when using a wave solder bath, soldering should be performed in a manner that does not produce substrate warping.

5.4.2 Notes on Mounting Surface Mount Devices (SMD)

Substrate mounting methods for Surface Mount Devices (SMD) include infrared reflow, air reflow, and vapor phase reflow, etc. Thus, soldering methods which heat the entire package are often used.

In contrast to conventional THD where only the external lead pins are heated, the entire SMD package is suddenly exposed to high temperatures, so mold resin cracking and degraded moisture resistance must be taken into account as potential reliability problems.

In addition, SMD have short external lead pins, narrow pin intervals and large numbers of pins to facilitate high density mounting. Therefore, sufficient care must be taken when handling SMD.

General precautions when mounting SMD products are described below.

(1) Notes during mounting

When soldering is performed by infrared reflow or other methods which heat the entire device in the condition where the mold resin has absorbed moisture due to long-term storage in the normal environment or storage in a high humidity environment, the mold resin may crack or delamination may occur at the chip boundary.

Care should be taken for the following points during mounting.

- Set the soldering peak temperature as low as possible, and also reduce the number of processing times.
- Perform preheating to avoid subjecting devices to sudden temperature changes.
- Products which require moisture absorption control are packed in moisture-proof packing to avoid moisture absorption during transport and storage. To prevent the progression of moisture absorption after opening the moisture-proof packing, these products should be stored in the prescribed environment, and reflow mounting should be performed within the allowable storage time. If the mold resin has absorbed moisture, the devices should be baked before mounting.
- When removing mounted devices from printed substrates and then performing soldering again, use new devices if at all possible. If removed devices must be reused, take care for external lead deformation and also carry out baking before reusing devices which are susceptible to moisture absorption.
- When mounting devices on both sides of substrates, take care for the soldering temperature and time. In addition, moisture absorption must also be controlled during the first and second soldering periods for devices which are susceptible to moisture absorption.

(2) Deformation of external lead pins

If the external lead pins bend or float, good solder connection with the substrate may not be obtained, resulting in mounting defects. Particular care must be taken for the flatness of external leads so that pins do not float during mounting.

In addition, when mounting SMD, if strict control is performed for only the external lead pins and the substrate control is insufficient, good solder connection may not be obtained. Full care should be given to substrate warping and cream solder film thickness and uniformity, etc.

(3) Handling of taping parts

When using taping-packed SMD, static electricity is generated when the top cover tape is peeled from the carrier tape, and the SMD may become charged.

This charge voltage increases as the speed at which the top cover tape is peeled becomes faster.

High speed tape peeling and rubbing should be avoided as much as possible to prevent electrostatic breakdown.

(4) Other precautions

When coating SMD and other devices with plastic after mounting on a substrate, moisture absorption may cause the leak current to increase depending on the coating plastic, or the stress of the coating plastic may also produce mechanical stress on the plastic portions of devices. Therefore, post-coating reliability must be thoroughly confirmed when selecting the coating materials.

5.4.3 Reflow Mounting of SMD

SMD are mounted by applying a certain amount of solder paste to the printed substrate pattern using the screen printing or other method, and then placing the package on this solder paste. At this time the package is tentatively fixed by the surface tension of the solder paste. Then, when the solder is reflowed, the package leads and the printed substrate pattern are joined by the self-alignment effect due to the surface tension of the melted solder.

The types of reflow mounting are as follows according to the heating method. However, each heating method has its own characteristics, and the appropriate reflow method should be selected according to the characteristics of the mounting substrate and various mounted components to be soldered.

(1) Infrared reflow method

This soldering method irradiates infrared rays to the entire wiring substrate on which devices have been mounted. Multiple devices can be soldered at once, making this method suitable for mass production. However, it also has the disadvantage that if there is a large difference in device heights, temperature differences occur depending on the distance from the infrared ray source. There is also some equipment which uses both infrared rays and hot air.

(2) Hot air reflow method (Air reflow method)

This method heats air or inert gas with a heater, circulates this heated air or gas inside an oven, and performs solder reflow by thermal conduction from this hot air. Like vapor phase reflow, there is little temperature difference between the substrate and the device, and the temperature can be controlled to a certain temperature or less. Furthermore, solvent usage is not required, so cases of switching from vapor phase reflow to hot air reflow are increasing. However, the atmosphere allows solder oxidation to occur more easily than for vapor phase reflow, so it is more difficult to form solder balls, etc.

(3) Vapor phase reflow method

This method is also called vapor phase soldering (VPS). This method heats a solvent (fluorocarbon, etc.) with a vapor pressure of 200℃ to 215℃ to create a vapor layer, and reflows the solder inside this vapor layer. The use of solvent vapor facilitates temperature control, and there is no solder or flux sticking.

The VPS method is well suited for mass production and also has a high solderability level. However, the use of fluorocarbon-based solvents creates the problem of fluorocarbons in the exhaust, and with increased fluorocarbon regulations, many soldering facilities are being switched over to a different method.

(4) Laser heating method

This soldering method irradiates a laser beam at the soldered portions to melt the solder.

(5) Hot air heating method

This soldering method heats air, nitrogen or other gas with a heater and blows it from a nozzle. The thermal conductivity and heat capacity of the gas used as the heat medium are small, so a large gas flow must be supplied, making it difficult to ensure uniform and stable conditions. As a result, this method is not used much for mass production.

However, this method allows local melting of solder, so it is sometimes used to remove defective devices.

5.4.4 Recommended Conditions for Various SMD Mounting Methods

The mounting methods most generally performed for SMD are the infrared reflow method, vapor phase reflow method, and flow soldering method (wave soldering method). All of these mounting methods heat the entire package and apply strong heat stress to the package, so like the solder junction temperature, the package surface temperature must also be controlled from the viewpoint of maintaining reliability.

This section describes the recommended condition concepts using Fig. 5-34.

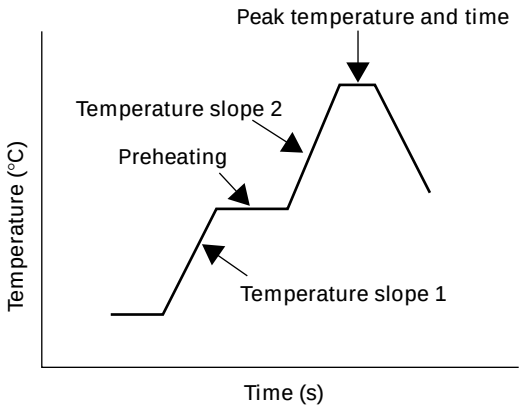


Fig. 5-34 Mounting Temperature Profile

(1) Temperature slope 1

When the temperature rises suddenly, the temperature at each part of the SMD package (for example, the package surface, interior, bottom) is uneven, and differences in the coefficients of thermal expansion of the materials may cause the package to warp and damage the chip. Therefore, care must be taken for the temperature rise rate slope.

(2) Preheating

The temperatures of the components, substrate and other parts are adjusted at the solder melting temperature or less to stabilize the solder junction and lessen the heat shock. The preheating temperature is generally set near the rated temperature for SMD.

(3) Temperature slope 2

Like (1) above, care must be taken for the temperature rise rate slope, and the peak temperature and time in (4) below must be kept within the prescribed limits.

(4) Peak temperature and time

The peak temperature and time require the most caution to minimize the damage sustained by the package. The peak temperature directly affects the drop in plastic strength (due to the resin temperature characteristics) and the steam pressure inside the package, so the temperature should be as low as possible. In addition, the steam pressure rises over time, so the soldering time must be as short as possible.

Fig. 5-35 shows the recommended conditions for infrared reflow and air reflow performed by the Sony Semiconductor Network Company.

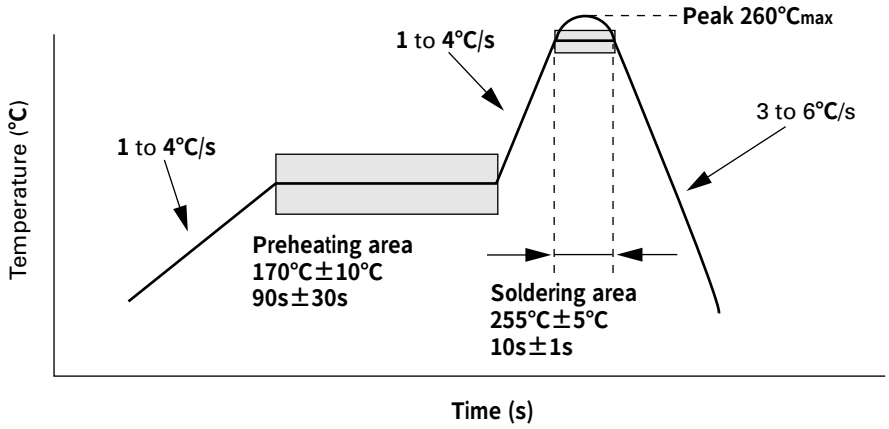


Fig. 5-35 Recommended Conditions for Infrared Reflow and Air Reflow

5.4.5 Soldering of CCD Area Sensors and CCD Linear Sensors

- **Soldering**

Care should be taken for the following points during soldering.

(1) Do not let the package temperature exceed 80℃.

(2) Absolutely do not use a mounting oven for soldering, as this may cause glass cracking or other problems.

(3) Use a grounded 30 W soldering iron with a tip temperature of 350℃, and solder each pin in 2 s or less. Solder should be applied to the areas shown in Fig. 5-36.

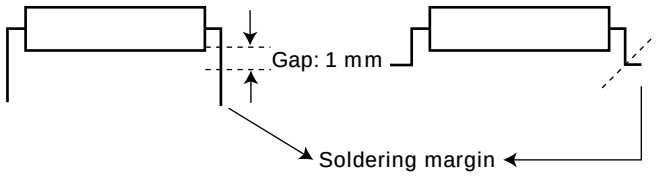


Fig. 5-36 Soldering Areas

(4) Allow sufficient cooling when readjusting or removing CCD area or linear sensors.

In particular, the upper and lower ceramic (or the plastic and ceramic) of CERDIP packages and linear sensor plastic packages are adhered using low melting point glass.

If the temperature difference between point b (low melting point glass) and point a (lead base) in Figs. 5-37 and 5-38 is 100℃ or more, the low melting point glass may crack.

Avoid local heating, rapid heating and rapid cooling

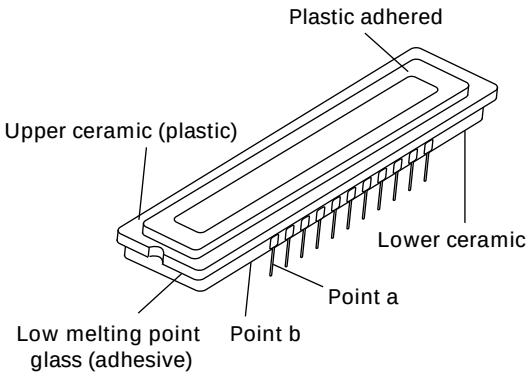


Fig. 5-37 Linear Sensor Structure

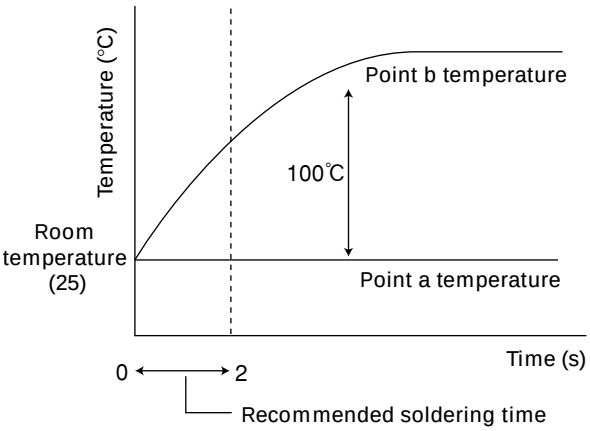


Fig. 5-38 Rise in Package Temperature due to Soldering

5.5 Notes on Handling to Prevent Misoperation

Unlike other semiconductor devices, microcomputers are semiconductors which first operate as completed products after having a program installed. Therefore, in addition to requiring the same care for handling as other semiconductors, it is also important to fully understand the microcomputer characteristics when creating programs in order to prevent accidents when products are used.

Hardware and software items which should be taken into account when using microcomputers are described below.

5.5.1 Notes on Hardware

(1) Power Supply

Power supply design must be thoroughly investigated in order to correctly operate not just microcomputers but all semiconductor products. Key points when designing power supplies include providing a stable voltage which satisfies the specifications, ensuring a current supply capacity that adequately satisfies the current consumption of the microcomputer (the current output from the microcomputer ports must also be taken into account), maintaining voltage for a certain time with respect to momentary voltage drops (this is related to the reset circuit described hereafter), blocking external noise to prevent it from affecting the microcomputer, and preventing noise generated by the microcomputer from leaking externally. Thus, it is not enough simply to produce voltage.

In terms of voltage stability, when the set uses an AC power supply or a battery, it is important to constantly maintain the voltage supplied to the microcomputer within the specified range with respect to the voltage fluctuations of this AC power supply or battery, and the microcomputer must also not be affected by sudden voltage fluctuations. It is particularly important to maintain voltage with respect to momentary power failures. However, a reset circuit must also be designed so that the set is reliably reset in the event of a power failure which might affect the microcomputer.

Insufficient current capacity may cause the supply voltage to drop with the result that the voltage falls below the range assured by the specifications. In addition to the current consumption prescribed by the specifications, the current flowing to the microcomputer also includes the current supplied from the output ports to external circuits, so this current changes according to the conditions under which the microcomputer is used. These elements must also be taken into account in the current capacity design.

When using an external power supply, noise may enter from that line. If this noise directly enters the microcomputer power supply, it may cause misoperation. Therefore, noise filters should be inserted to the external power supply input lines, or the power supply circuit should have low impedance. In addition, microcomputer operation may also be a source of noise, so noise countermeasures for power supplies are also important to prevent this noise from leaking externally.

There are also cases where separate power supplies for basic block circuits or for peripheral circuits such as an A/D converter are required in the microcomputer power supply pins. However, the required power supply characteristics differ in many of these cases. Power supplies must be connected to all of these pins, but it is important to check the specifications listed in the product data sheets and to design power supplies which satisfy the requirements.

(2) Oscillation Circuit

Oscillation circuits are important circuits which generate the microcomputer operating clocks, so oscillation must be stable and uninterrupted under the hypothesized operating conditions. Elements which can be used for oscillation include crystal oscillators and ceramic vibrators, but the added capacitance and other constants must be optimally set for each of these to ensure that oscillation starts reliably and to maintain stable oscillation. Furthermore, the operating voltage range also affects the circuit constant settings. The optimum added capacitance under these conditions must be determined using the final set board, and a reliable method for achieving this is to provide the board and intended microcomputer to the oscillator manufacturer and have the oscillator manufacturer measure the optimum capacitance.

(3) Reset Circuit

Like the power supply and oscillation circuits, the reset circuit is also an important circuit for reliably operating microcomputers. The circuit structure must reliably apply a reset not only during power-on, but also when momentary voltage drops occur.

During power-on from the zero-voltage state, a reset is applied even with a simple CR delay circuit. However, this cannot support cases where the voltage drops momentarily such as momentary power failures, and reliably applying a reset when the voltage drops gradually and the supply voltage is at the specification or less is also difficult, which can lead to malfunction.

When designing the reset circuit, the power-on reset cancel voltage, reset application time, and the voltage setting at which reset is applied when the voltage drops should all satisfy the product specifications. In addition, the circuit must also be able to reliably apply a reset when momentary voltage drops occur.

(4) Test Mode

Microcomputers switch between normal operation and test mode according to the input level of a certain pin during reset in order to make the test mode settings. The test pins also function as general-purpose ports to maximize the valid pins, and can be set to the level for entering test mode by an externally connected circuit. These pins are noted in the User's Manual of each microcomputer, and these contents should be fully understood before designing circuits.

(5) Noise Countermeasures

Thorough noise countermeasures must be taken for both external influences on microcomputers and the external influence of microcomputers. Although mentioned under Power Supply, the processing for each pin is also described here. In addition to power supply pins, input/output pins are also susceptible to the effects of noise. These pins are each connected to external circuits, so countermeasures suited to these circuits are required. Simple CR filters are generally used, but when directly controlling signals outside the substrate on which the microcomputer is mounted, the circuit configuration should connect through a buffer circuit to prevent noise received by long wiring paths from reaching the microcomputer.

Noise emitted by microcomputers must be suppressed by external circuits, and this requires optimization of the power supply and signal line layouts. Attaching the above CR filter to each pin is also effective in this case. There are often substrate design limitations, but it is important to first determine how to implement noise countermeasures, and then proceed with the overall substrate layout.

5.5.2 Notes on Software

(1) Initial Value Settings

When reset is canceled, operation starts in accordance with the program built into the microcomputer. However, initial settings must be made in the initial stages of this program to enable the various built-in functions. The initial RAM status is undetermined, so the areas to be used must all be set initially by the program. The initial register values of various peripheral circuits may be undetermined after reset, so initial values must be set for these as well. The initial register status for each peripheral circuit is noted in the User's Manual, so these must all be checked and set.

(2) Deadlock

When compiling a program, the program may wait for a certain phenomenon to occur before shifting to the next process. In this case, if the anticipated phenomenon does not occur for whatever reason, the program cannot shift to the next process, and the current process is repeated endlessly, making it appear as if operation has stopped. This is called deadlock, and countermeasures for avoiding deadlock must be considered. In addition to the anticipated phenomenon, timer interrupts and other regularly occurring phenomenon are also generally checked at the same time, so if the anticipated phenomenon does not occur for a certain time or more, this is processed as an error and the corresponding countermeasure routine is executed. This makes it possible to know the cause when operation stops, and is useful for investigating causes when trouble occurs.

5.6 Notes on Product Specifications, Packing, Transport and Storage

5.6.1 Notes on the Use of Semiconductor Devices

The Sony Semiconductor Network Company makes the utmost efforts to improve quality and reliability, but due to the nature of semiconductor devices, a certain percentage of devices may malfunction or fail. When using semiconductor products manufactured by the Sony Semiconductor Network Company, customers are requested and responsible for ensuring safe equipment and system designs to prevent accidents resulting in death, injury or damage to property from occurring as a result of semiconductor failure.

Note that when designing equipment and systems, the latest product specifications should be checked, and products should be used within the assured ranges.

Semiconductor products listed in catalogs and sold assume use in general electronic equipment (home appliances, telecommunications equipment, measuring instruments, office equipment, etc.). Customers should be sure to consult their Sony sales representative beforehand when planning use for applications requiring special quality and reliability, or in equipment and systems (automobiles, traffic equipment, medical equipment including life-support devices, safety devices, aerospace equipment, nuclear power control equipment, etc.) where product failure or malfunction may pose a direct life- or injury-threatening risk or damage to property.

Special consideration and selection is required for products which demand high reliability.

5.6.2 Maximum Ratings (Absolute Maximum Ratings)

The maximum ratings of semiconductor devices are normally prescribed by the [Absolute Maximum Ratings]. According to JIS C 7032, absolute maximum ratings are prescribed as "Limit values which must not be exceeded even momentarily, or limit values for which the values of two or more items must not be reached simultaneously when specification values are established for two or more items." Exceeding absolute maximum

ratings even temporarily causes degradation or failure, and even if the product continues to operate for some time thereafter, the life is significantly shortened. Therefore, when designing electronic circuits using semiconductor devices, care must be taken not to exceed the maximum ratings of these devices even due to fluctuations caused by external conditions during operation.

5.6.2.1 IC Maximum Ratings

Maximum ratings indicate the operating limit values for that IC, and parameters such as those shown in Table 5-8 are generally prescribed. When actually using ICs, operation must stay within these prescribed ranges.

Table 5-8 Examples of Absolute Maximum Ratings

Item	Conditions	Rating value	Contents
Supply voltage (V_{DD}) (V_{CC})	Ta=25℃ Measured relative to the V_{SS} pin	7.0 V (for a 5.0 V device)	This is the maximum voltage that can be applied between the power supply pins and the GND pins. 1. This is related to the endurance voltage of the transistors inside the IC, and breakdown may occur if this voltage is exceeded. 2. CMOS devices may break down due to dynamic latch-up or the injection of large quantities of hot carriers.
Input and output voltages (V_{IN}) (V_{OUT})	Ta=25℃ Measured relative to the V_{SS} pin	–1.0～7.0V	This is the maximum voltage that can be applied between the input/output pins and the GND pins. This voltage generally cannot be larger than the supply voltage. 1. Parasitic elements configured on the input and output pins may experience endurance voltage-related breakdown. 2. Breakdown may be caused by latch-up triggered by the input or output pins.
Allowable power dissipation (P_D)	Ta=25℃	1W	This is the maximum power consumption allowed inside the IC. 1. Breakdown may be caused by internal heat generation during operation. 2. This value differs according to the degree of IC integration and the heat radiation characteristics of the package.
Storage temperature (Tstg)	–55～150℃		This is the allowable ambient temperature range during storage. 1. The temperature is limited by the package materials and the intrinsic properties of semiconductors.
Junction temperature (Tj)			This is the maximum allowable junction temperature value at which continuous operation is possible.
Operating temperature (Topr)	0～70℃		Recommended operating temperature condition range: IC operation and functions can be assured within this temperature range, but the electrical characteristics indicated at Ta = 25℃ cannot necessarily be assured.

Note) Rating values are prescribed by the individual specifications for each device.

Fig. 5-39 shows the relationship between various IC maximum ratings.

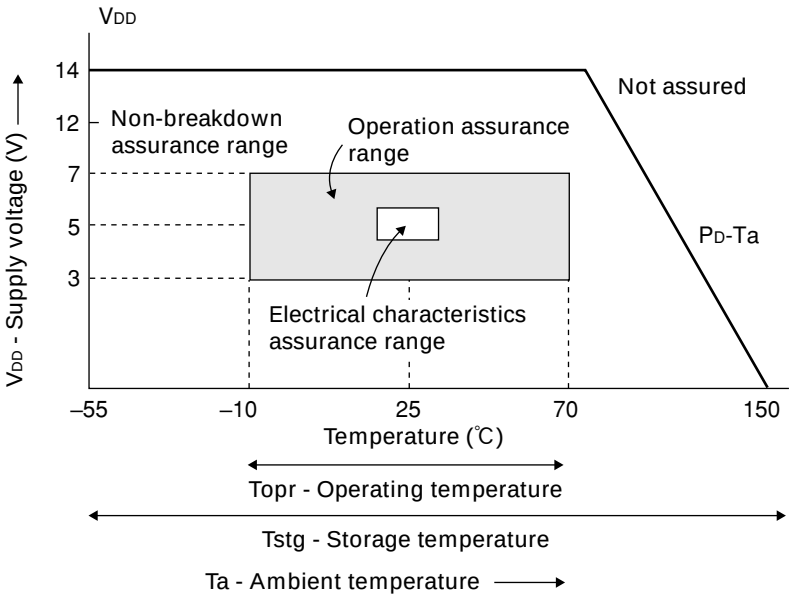


Fig. 5-39 Relationship between Various Maximum Ratings

IC maximum ratings are assured continuously, but the following guidelines should be taken into account, particularly for power ICs.

Average current: ICC×0.5
Peak current: ICC (peak)×0.8
Average power: Maximum rating×0.5

5.6.2.2 Derating of Diodes, Transistors and Power Devices

With respect to excessive conditions, the peak voltage, current, power and junction temperature including surge and other factors are generally set to the maximum ratings or less, and derating for reliability design is performed using the average values. (Table 5-9)

Derating: Intentionally reducing loads from rating values to improve reliability. (JIS Z8115-1981)

Table 5-9 Derating Design References

Derating element		Diode	Transistor	Power device
Junction temperature	Tj	Maximum rating ×0.7 times or less	Maximum rating ×0.7 times or less	Maximum rating ×0.7 times or less
		Power consumption, ambient temperature and radiation conditions $Tj = P_D \times \theta j-a + Ta$		
Voltage	V_{CBO}, V_{CEO}	Maximum rating ×0.8 times or less	Maximum rating ×0.8 times or less	Maximum rating ×0.8 times or less
Current	I_C, I_B, I_E	I_F, I_Z×0.7 times or less	Maximum rating ×0.8 times or less	Maximum rating ×0.8 times or less
	I_C (peak)	Maximum rating or less	Maximum rating or less	Maximum rating or less
Power	P_C, P_D	According to the derating curve within the Tj range		

5.6.3 Notes on Packing, Transport and Storage

5.6.3.1 Packing Methods

In order to maintain the high quality and high reliability of semiconductor devices (hereafter “devices”) the following three packing methods are mainly used in accordance with the package shape and mounting format.

(1)	Magazine	THD packages (DIP, SDIP, SIP) and SMD packages (SOP, SSOP, etc.)
(2)	Tray	SMD packages (QFP, LQFP, SOP, SSOP, etc.)
(3)	Embossed taping	SMD packages (QFP, LQFP, SOP, SSOP, etc.)

Care should be taken for electrostatic breakdown during handling, package cracking during mounting due to package moisture absorption, mechanical breakdown due to shocks, lead bending, and other causes of device breakdown.

(1) Magazine packing

- The magazine, stopper pin and rubber plug materials are PVC plastic. (Fig. 5-40)
  The surfaces are coated with an anti-charging agent to prevent static electricity. Care should be taken as this anti-charging agent is water soluble, and the effects will be lost if the magazine is dampened by water or stored in a high temperature and high humidity location. Apply the anti-charging agent again when reusing magazines.
- The magazines and stoppers do not have heat resistant specifications. (70℃ max.)
  When baking (drying at high temperature) is necessary, transfer the devices to a metal magazine. At this time, care must be taken to prevent lead bending particularly for SMD, such as by using a transfer jig.
- Magazines are packed in aluminum laminate moisture-proof bags to prevent moisture absorption and block contact with the outside air, and devices should be mounted as soon as possible after opening this packing. In addition, confirming the solderability is recommended before using products that have been stored for long periods.

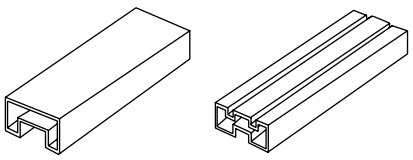


Fig. 5-40 Conductive Magazines (Tubes)

(2) Tray packing

Trays come in heat resistant specifications and normal temperature specifications. (Fig. 5-41) When products in normal temperature specification trays are to be baked (dried at high temperature), these products must be transferred to a heat resistant specification tray.

There are two types of trays as follows according to the molding method.

1. Injection molded hard trays
2. Vacuum molded soft trays

The plastic used for injection molding is mixed with carbon to prevent charging, and is conductive. Anti-charging materials are mixed into vacuum molding materials or applied in a coat over the plastic sheet, so both types have anti-charging specifications.

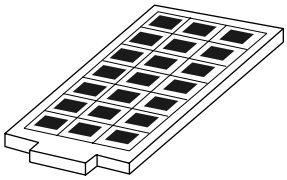


Fig. 5-41 Tray

Tray products are mainly QFP, LQFP, BGA and TSSOP package products which are stored and shipped in injection molded hard trays, and CCD, LCD and laser diodes which are stored and shipped in vacuum molded soft trays.

(3) Embossed taping packing

To improve mounting efficiency during set assembly, semiconductor products are stored in embossed conductive plastic tape, wound onto reels, and shipped in aluminum laminate bags with desiccants and humidity indicators. Embossed taping storage standards are prescribed by EIA 481A and JIS C 0806, and the widths of 8, 12, 16, 24, 32, 44 or 56 mm are used according to the product size. (Fig. 5-42)

For details, see the individual product specifications.

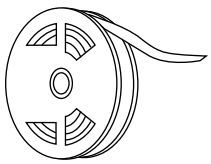


Fig. 5-42 Taping

The tape and reels do not have heat resistant specifications, so baking is not possible. When a reel is only partially used during mounting, care must be taken for handling to prevent moisture absorption by removing the reel from the mounter and repacking it in the original bag, etc.

The carrier tape and top cover tape are heat sealed with adhesive, and the peeling strength prescribed by EIA is assured for a period of one year after shipment.

5.6.3.2 Packing

Devices contained in magazines, trays and embossed taping are stored and shipped in inner and outer boxes to avoid the effects of external shocks during transport, rain water during storage, or contamination from the outside air, etc.

(1) Outer carton

- Products are stored and shipped in cardboard outer cartons to minimize the effects of shocks, vibration, humidity and other factors on devices.
- Cardboard and other outer cartons have symbol marks urging caution during handling such as those shown in Fig. 5-43 for “Avoid static charges”, “Fragile”, “Keep dry” and “This side up”. The caution marks should be observed during storage and transport.

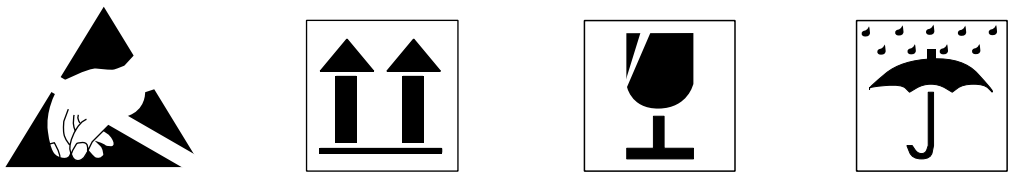


Fig. 5-43 Packing Carton Markings

(2) Inner Carton

- Magazine packing (see item 5.6.3.1) is used for THD, SOP and other packages with the external lead pins in two directions. The Sony Semiconductor Network Company places SMD packages and S-Pd PPF products in moisture-proof packing bags and then stores these bags in an inner carton.
- Moisture absorption affects Surface Mount Device (SMD) quality, and moisture-proof packing aims to prevent moisture absorption during storage. Devices, desiccants and moisture indicators for detecting humidity are placed in aluminum laminate bags which are deaerated and heat sealed to block outside air and prevent the entry of moisture. (Fig. 5-44)
  After the bags are opened, control should be performed so that devices are used within the specified time.

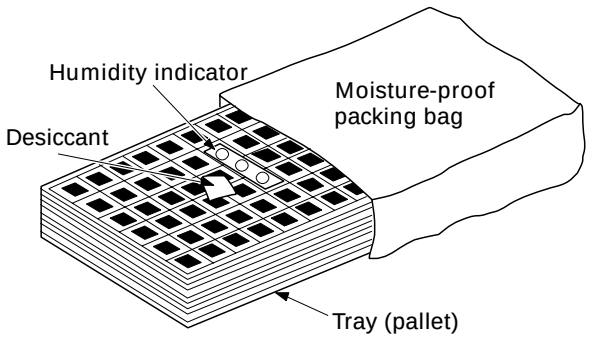


Fig. 5-44 Moisture-proof Packing

- Taping is used for SMD due to advantages such as easy handling during automatic mounting and high packing density. Note that the tape and reel do not have heat resistant specifications, so baking is not possible. The carrier tape and top cover tape peeling force (Fig. 5-45) is 0.1 to 0.7 N for a peeling speed of 300 mm/min and a peeling angle of 165° to 180° with respect to the adhered tape surface. The peeling strength is assured for a period of one year after shipment.

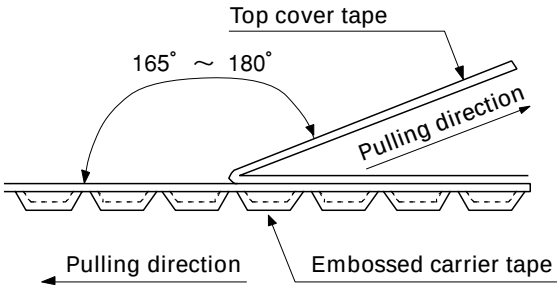


Fig. 5-45 Tape Carrier Peeling Method

[Note]

When the humidity indicated by the humidity indicators of devices in moisture-proof packing exceeds 30% (pink), these devices must be dried again (baking at 125℃ for 24 h or 125℃ for 48h).

5.6.3.3 Transport Methods

If handling is rough and strong shocks are applied during transport, Surface Mount Devices (SMD) in particular may experience lead bending, causing the coplanarity of the external leads to worsen (80 _m or more) and resulting in trouble during soldering. Also, if the aluminum laminate moisture-proof packing bags become torn, moisture is absorbed from the outside air and may cause package cracking.

The contents of caution marks on packing cartons are as follows.

- Fragile
  If packing cartons are thrown or dropped during handling, the packing materials and possibly the devices themselves may be damaged. Semiconductor devices should be handled as “fragile” items.
- This side up
  Packing cartons should be placed facing the correct direction as indicated on the packing carton during transport. If packing cartons are turned upside down or on their sides, unnatural force may be applied to and damage devices.
- Keep dry
  When cartons absorb water, the strength drops drastically, so cartons must not be allowed to become wet especially during transport in rain or snow.
- Avoid static charges
  This is not a caution during transport, but is indicated as a caution during set mounting.

In addition to the above cautions, devices must be transported in a manner which minimizes mechanical vibrations and shocks as much as possible.

5.6.3.4 Storage Methods

(1) Storage of assembled products

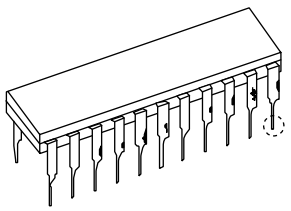
- Storage environment temperature
  Assembled products should be stored indoors under ambient conditions of 0℃ to 35℃ and humidity of 85% or less. The so-called normal temperature and humidity are suitable for the temperature and humidity of locations where semiconductor devices are stored.
- Storage time limit
  The limit for non-taping products (products packed in magazines and trays) is 1.5 years from the week indicated by the marking. The limit for taping products is the shorter of one year from the taping package label issue date or 1.5 years from the week indicated by the marking.
- Ambient conditions
  Avoid storage in locations exposed to direct sunlight, locations where corrosive gases are generated, or dusty locations.
  - Magazines and non-heat resistant trays may deform if exposed to direct sunlight.
  - Corrosive gases cause the external lead pins or metal casings of devices to corrode (deteriorated solderability).
- Temperature changes (avoiding condensation)
  Moisture condenses on packed products in locations where the temperature changes suddenly. Semiconductor devices must be stored in locations where the temperature changes as little as possible.
- Load limits
  Avoid stacking or placing heavy objects on packing boxes as much as possible to avoid applying loads to devices.
  The maximum mass of the outer box is prescribed as 10 kg.
- The storage location should not be exposed to radiation, strong electromagnetic fields or static electricity.

(2) Long-term storage

When storing devices for long periods, the storage time limit shall be 5 years or less based on the product packing specifications and under storage environment conditions of temperature 30℃ and humidity 85% or less. However, storage in the taping condition is prohibited.

Devices are stored in the loose condition (packed in trays or magazines), taping work is performed if necessary, and devices are shipped as quickly as possible.

Special care must be taken as follows for long-term storage, as the lead pin solderability may deteriorate, the lead pins may rust (Fig. 5-46), or the electrical characteristics may deteriorate.



When stored for long periods, the lead pin solderability may deteriorate.

Fig. 5-46 Lead Rusting

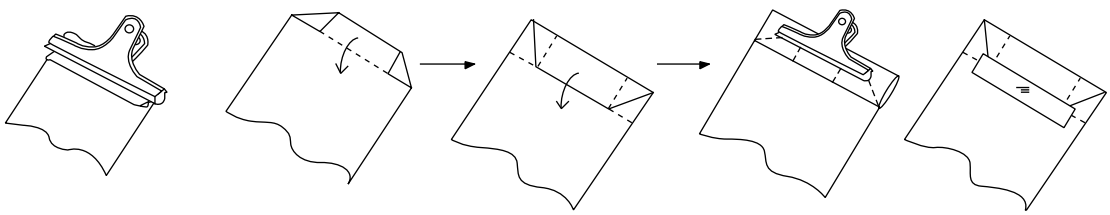
- Packing
  When long-term storage (one year or more) is anticipated from the start for THD (DIP, SIP, etc.) products without moisture-proof packing, these products should be placed in moisture-proof packing or other countermeasures should be taken to prevent deteriorated solderability and rust.
- Check items
  When a long time (one year or more) has passed in the stored condition, the solderability and lead rusting should be inspected prior to use. The electrical characteristics should also be inspected as necessary.

(3) Handling of products in moisture-proof packing

As packages become thinner, package cracking in soldering processes which use methods that heat the entire package (dip, reflow) has become a problem. Package cracking occurs when package resin that has absorbed moisture from the air is exposed to a high temperature atmosphere during soldering, and it is necessary to suppress moisture absorption as a countermeasure.

Resin basically has a nature which easily absorbs moisture, so it easily takes in moisture from the air. For this reason, Sony uses moisture-proof packing to prevent SMD from absorbing moisture. However, it should be kept in mind that moisture absorption starts when the moisture-proof packing is opened.

- Opening moisture-proof packing
  Moisture-proof packing must absolutely not be opened except when not using all of the SMD contained in that packing. Also, care should be taken during all work to prevent holes from being opened in the aluminum laminate bags. If holes are opened, devices must be transferred to a new aluminum laminate bag which is then deaerated and heat sealed.
  When storage in the opened condition is unavoidable, use a SMD stocker controlled to a humidity of 30% or less.
- After opening moisture-proof packing, devices should be used according to the package mounting rank instructions. If moisture absorption progresses, baking (125℃ for 24 h) is required.
- When temporary storage is required after opening moisture-proof packing, place the devices together with a desiccant inside an aluminum laminate bag, fold the opening two or more times, and seal it with a clip or cellophane tape as shown in Fig. 5-47 to suppress moisture absorption.
- Taping packed products cannot be baked.



(1) When the clip is larger than the opening

(2) When the clip is smaller than the opening

(3) Sealing with cellophane tape

Fig. 5-47 Moisture Absorption Measures after Opening

5.6.3.5 Reusing Packing Materials

The Sony Semiconductor Network Company makes active efforts to recover and reuse packing materials such as magazines, trays, reels and some cardboard boxes in order to reduce plastic waste as much as possible. Cooperation with the collection of used packing materials is requested to protect the environment. Please contact your Sony sales representative for details.

5.6.4 Handling LCDs

(1) Electrostatic countermeasures

TFT-LCD panels are easily damaged by static charges, so be sure to take the following protective measures.

a) Use non-chargeable gloves, or simply use bare hands.
b) Use a wrist strap when directly handling panels.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install conductive mats on the work floor and worktable.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels when handling.

(2) Dust and dirt countermeasures

a) Operate in a clean environment.
b) When delivered, the panel surface (glass) is covered by a protective sheet. Take appropriate measures to prevent static charges, and then peel off the protective sheet carefully so as not to damage the glass surface.
c) Do not touch the glass surface, as the surface is easily scratched. When cleaning is required, gently wipe the glass surface with a clean-room wiper moistened with isopropyl alcohol. Be careful not to leave a stain on the surface.
d) Use ionized air to blow dust off the glass surface.

(3) Other handling precautions

a) Do not twist or bend flexible print circuits especially at the connecting region because they are easily deformed.
b) Do not drop panels.
c) Do not twist or bend panels or panel frames.
d) Keep panels away from heat sources.
e) Do not dampen panels with water or other solvents.
f) Avoid storing or using panels at a high temperature or high humidity, as this may adversely affect the panel characteristics.
g) The minimum bending radius of flexible print circuits is 1 mm.
h) When mounting panels, use a screw tightening torque of 3 kg·cm or less.
i) Use filters as appropriate to protect panels.
j) Do not apply pressure to panel locations (cover, etc.) other than the mounting holes.

Appendix

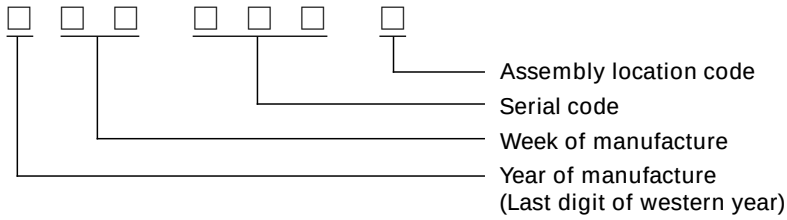
Appendix

1 Lot and Product Name Indications

The lot and product name indications used for products manufactured by the Sony Semiconductor Network Company (Sony Semiconductor products) are as follows.

(1) Product Lot Indications (Traceability)

1. Full lot number indication



2. Divided indication

□ □ □ Year and week of manufacture

□ □ □ □ Serial code and assembly location code

3. Lot indication omission order and abbreviated indication

When seven digits cannot be printed due to marking space limitations on products, the printed characters are omitted in the following order.

□ □ □ □ □ □ □

3) 2) 1)

1) Assembly location code
2) One's digit of serial code
3) Serial code

Abbreviated indication

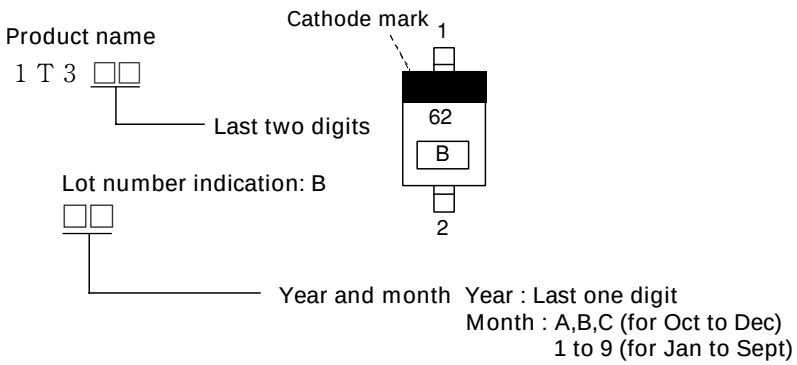
□ □ □ Year and week of manufacture

4. Marking on small products and lot indication on labels

Indications are abbreviated on small diodes, discrete devices, laser diodes, laser couplers and other small products. In addition, some products may not display markings.

Examples of specific varicap indications on products and product shipping labels are shown below.

4-1 SMVC

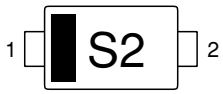


4-2 SSVC

Product name

1 T 4 □□

Last two digits code
402～409→S2～S9
410～416→X0～X6
Lot number indication omitted



1：Cathode
2：Anode

4-3 Label indication (example)

〈LOT〉 9 30 ／3000 G 5A07

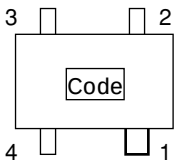
Control code
Assembly location code
Quantity
Year and week of manufacture

4-4 GaAs MES FET

4-4-1 Mini molded package

Product name	Product name/modification code
SGM2014AM	DA
SGM2016AM	MA
SGM2016AP	LA
3SK165A	JA
3SK166A	KA

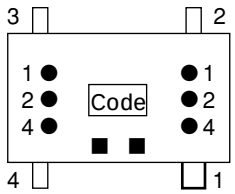
Marking method: Offset
(Laser marking introduced from 2000)
Indication method: Product name code only; lot number not indicated
(See the figure below.)



4-4-2 Super-mini molded package

Product name	Product name/modification code
SGM2013N	A
SGM2014AN	DA
SGM2016AN	MA

Marking method: Laser
Indication method: Product name code and lot number
(See the figure below.)



● Month of manufacture indication
January to June: Left side
July to December: Right side

■ Year of manufacture indication
Odd-numbered year: Left side
Even-numbered year: Right side

4-4-3 Label indications (example)

Mini molded package

〈LOT〉 931 ／3000 OB30 G

Assembly location code
Control number
Quantity
Year and week of manufacture

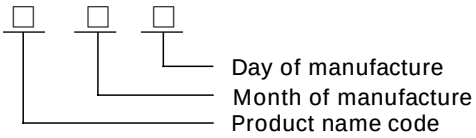
Super-mini molded package

〈LOT〉 930 ／3000 G 0A07

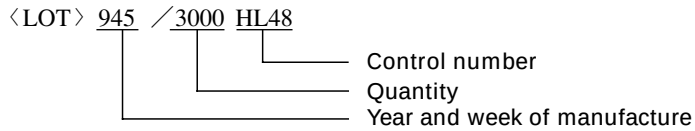
Control number
Assembly location code
Quantity
Year and week of manufacture

4-5 Small and large laser diodes

☆Indications are omitted on most small products.
When present, the indication is as follows.

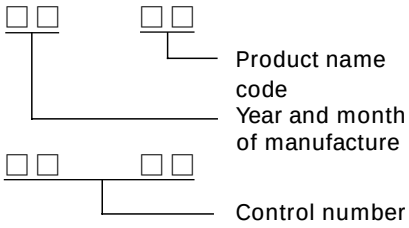


Label indication (example)
Small laser diode



4-6 Laser coupler

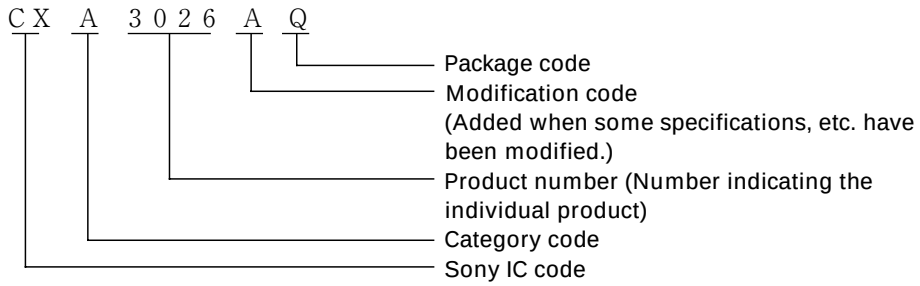
Indications are omitted on some products, but when present, the indication is as follows.



(2) Product Name Indications

1. IC

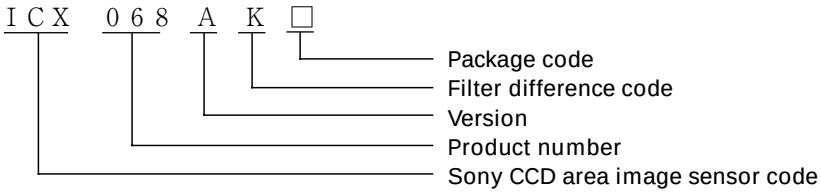
(Example)



2. CCD

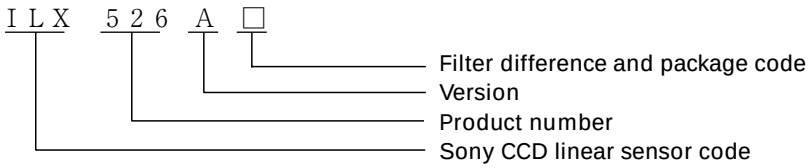
2-1 Area image sensor

(Example)



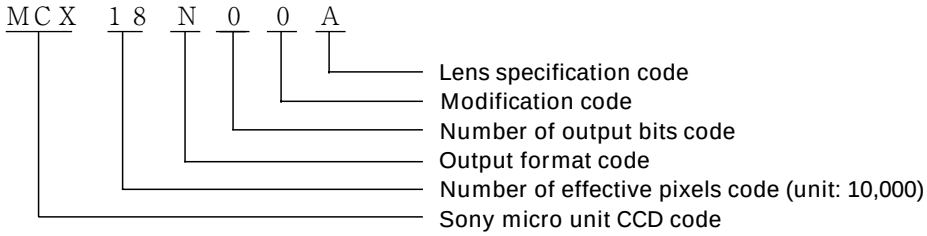
2-2 Linear sensor

(Example)



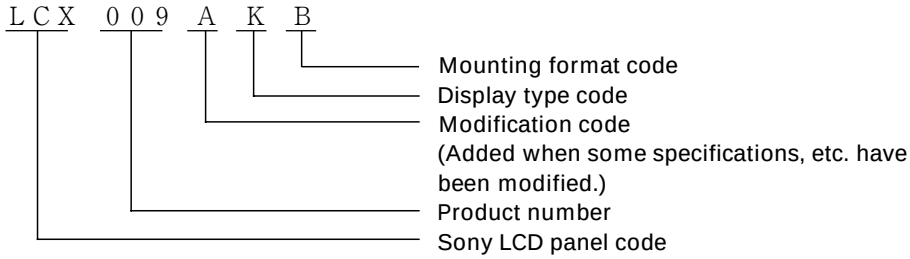
2-3 Micro unit CCD

(Example)



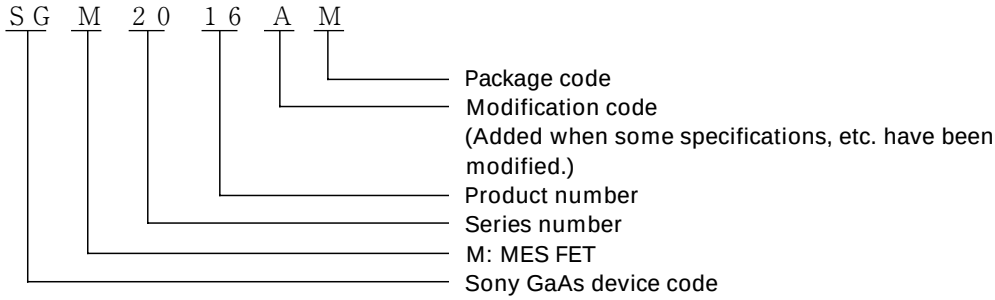
3. LCD

(Example)



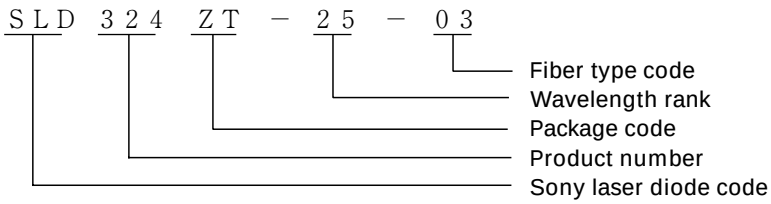
4. GaAs MES FET

(Example)

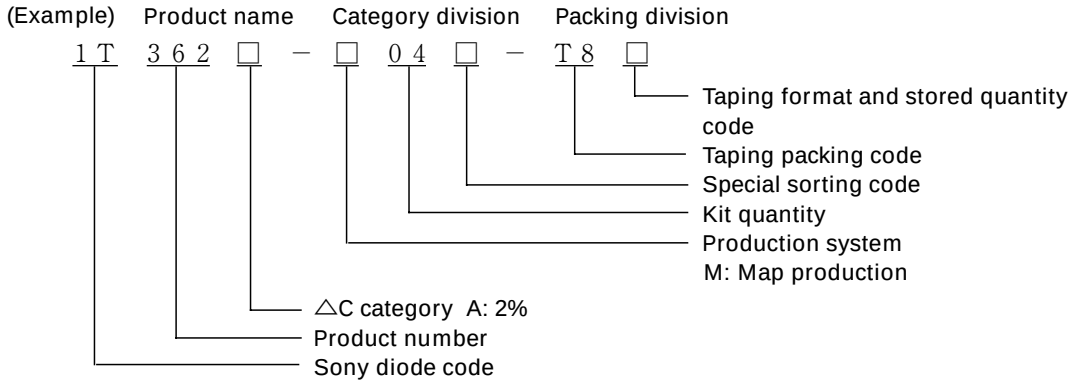


5. Laser diode

(Example)



6. Varicap (Varactor diode)



2 Sampling Inspections

Sampling inspections are used for shipping inspections, IPQC and other purposes.

Samples are taken from a lot and tested according to a predetermined sampling inspection plan, and these results are compared with lot judgment standards to judge whether that lot is accepted or rejected.

When n samples are taken at random from a lot having a defect rate of P, the probability P(x) that x defective products are contained in this sample is expressed by the following equation.

$$P(x) = \frac{n!}{x!\,(n-x)!} P^x (1-P)^{n-x}$$

A simple description of sampling inspection by attributes is given below.

The extracted samples are inspected and divided into good and defective products, then these quantities are compared with the judgment number to judge whether that lot is accepted or rejected.

For example, the operating characteristic curve (OC curve) for a lot size N = 1000, a sample size n = 20 and an acceptance number C = 1 is shown in Fig. A-1.

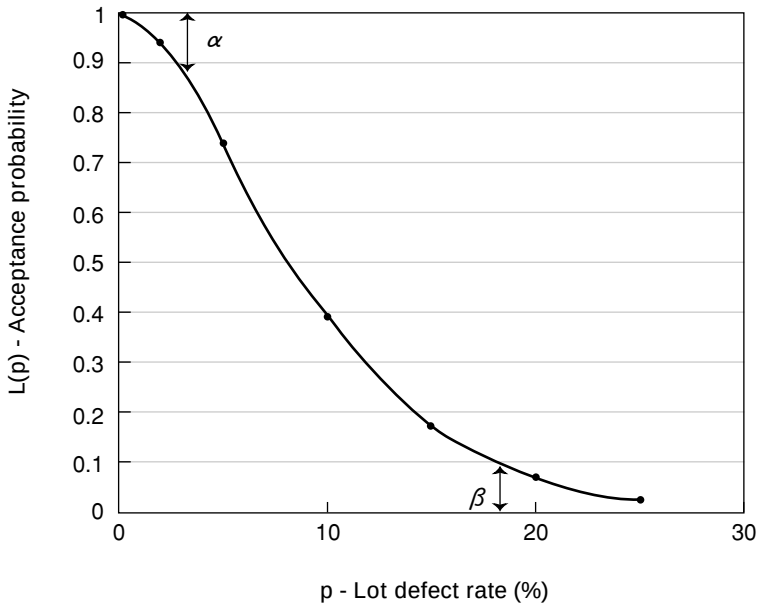


Fig. A-1 Operating Characteristic Curve

Fig. A-1 shows that when the lot defect rate is 10%, the probability L(p) of that lot being accepted is approximately 40%.

Thus, even bad lots may be accepted.

This is a problem for consumers, so the probability that a lot having the same defect rate as the Lot Tolerance Percent Defective (LTPD) might be accepted (consumer risk β) is prescribed at 0.1 or less. Conversely, the probability that a good lot might incorrectly be rejected (producer risk α) is prescribed at 0.05 or less.

Acceptable Quality Level (AQL) refers to the process average upper limit which can be considered acceptable.

Based on the ANSI/ASQC Z1.4 (MIL-STD-105E) Table, when single sampling inspection is performed with AQL = 0.065%, a lot size of 4000, inspection level II and normal inspection, the sample character is L, the sample size is 200, Ac = 0, and Re = 1.

Therefore, when 200 samples are taken and inspected, the lot is accepted if there are three or less defects, or rejected if there are four or more defects. (Fig. A-2, Tables A-1, A-2, A-3, A-4, A-5)

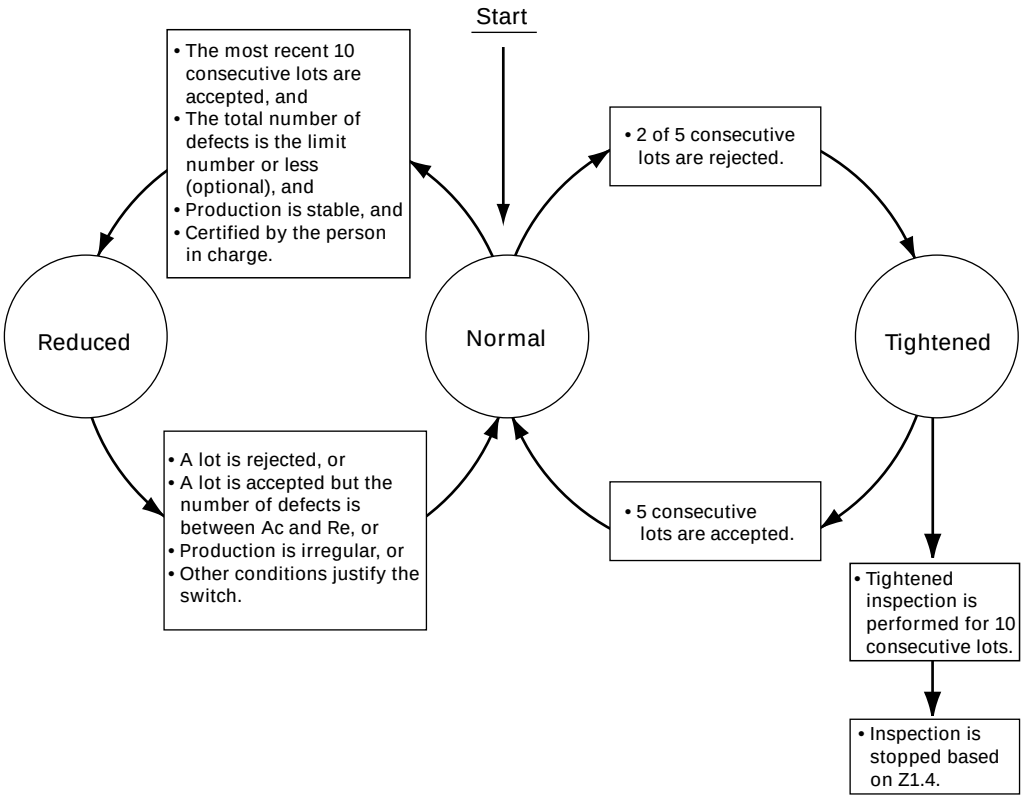


Fig. A-2 ANSI Z1.4 System Switching Rules

Table A-1 Sample Characters

Lot size	Special inspection levels				Normal inspection levels		
	S-1	S-2	S-3	S-4	Ⅰ	Ⅱ	Ⅲ
2 ～ 8	A	A	A	A	A	A	B
9 ～ 15	A	A	A	A	A	B	C
16 ～ 25	A	A	B	B	B	C	D
26 ～ 50	A	B	B	C	C	D	E
51 ～ 90	B	B	C	C	C	E	F
90 ～ 150	B	B	C	D	D	F	G
151 ～ 280	B	C	D	E	E	G	H
281 ～ 500	B	C	D	E	F	H	J
501 ～ 1200	C	C	E	F	G	J	K
1201 ～ 3200	C	D	E	G	H	K	L
3201 ～ 10000	C	D	F	G	J	L	M
10001 ～ 35000	C	D	F	H	K	M	N
35001 ～ 150000	D	E	G	J	L	N	P
150001 ～ 500000	D	E	G	J	M	P	Q
500001 ～	D	E	H	K	N	Q	R

ANSI / ASQC Z1.4

Table A-2 Normal Inspection Single Sampling Method (Main sampling table)

Sample character	Sample size	AQL: Acceptable Quality Level (Normal inspection)																												
		0.010	0.015	0.025	0.040	0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25	40	65	100	150	250	400	650	1000
		Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re
A	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	0 1	↓	1 2 3	1 2 3 4	2 3 4 5	3 4 5 6 7 8	5 6 7 8 10 11	7 8 10 11 14 15	10 11 14 15 21 22	14 15 21 22 30 31	21 22 30 31 44 45	30 31 44 45
B	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
C	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
D	8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2 3 4	2 3 5 6	3 4 5 6 7 8	↓	7 8 10 11 14 15	10 11 14 15 21 22	↓	↓	↓	↓	↓	↓
E	13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	1 2	1 2 3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
F	20	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
G	32	↓	↓	↓	↓	↓	↓	↓	0 1	0 1	↑	1 2	1 2 3 4	2 3 4 5 6	3 4 5 6 7 8	5 6 7 8 10 11	7 8 10 11 14 15	10 11 14 15 21 22	14 15 21 22	21 22	↓	↓	↓	↓	↓	↓	↓
H	50	↓	↓	↓	↓	↓	↓	↓	↓	↓	1 2	2 3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
J	80	↓	↓	↓	↓	↓	↓	0 1	↓	↓	↓	3 4	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
K	125	↓	↓	↓	↓	↓	0 1	↓	1 2 3	1 2 3 4	2 3 5 6	5 6 7 8	5 6 7 8 10 11	7 8 10 11 14 15	10 11 14 15 21 22	14 15 21 22	21 22	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
L	200	↓	↓	↓	↓	0 1	↓	1 2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
M	315	↓	↓	↓	0 1	↑	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
N	500	↓	↓	0 1	↓	1 2 3	1 2 3 4	2 3 3 4 5 6	3 4 5 6 7 8	5 6 7 8 10 11	7 8 10 11 14 15	10 11 14 15 21 22	14 15 21 22	21 22	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
P	800	↓	0 1	↑	1 2	↑	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Q	1250	0 1	↑	1 2	2 3	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
R	2000	↑	↑	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑

ANSI / ASQC Z1.4

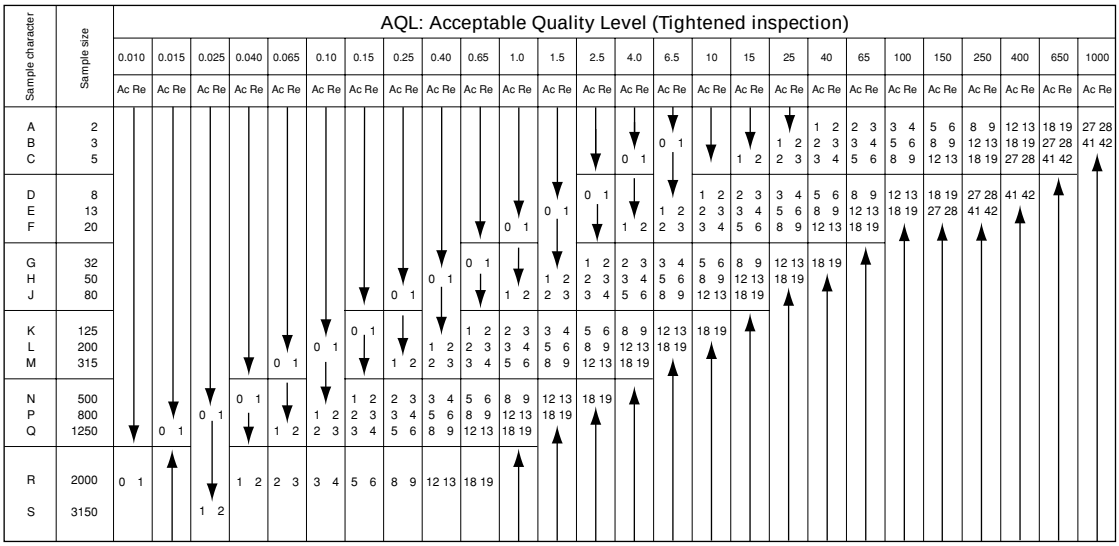
↓ = The first sampling plan below the arrow is used. If the sample size is larger than the lot size, the entire lot is inspected.

↑ = The first sampling plan above the arrow is used.

Ac = Acceptance number

Re = Rejection number

Table A-3 Tightened Inspection Single Sampling Method (Main sampling table)



ANSI / ASQC Z1.4

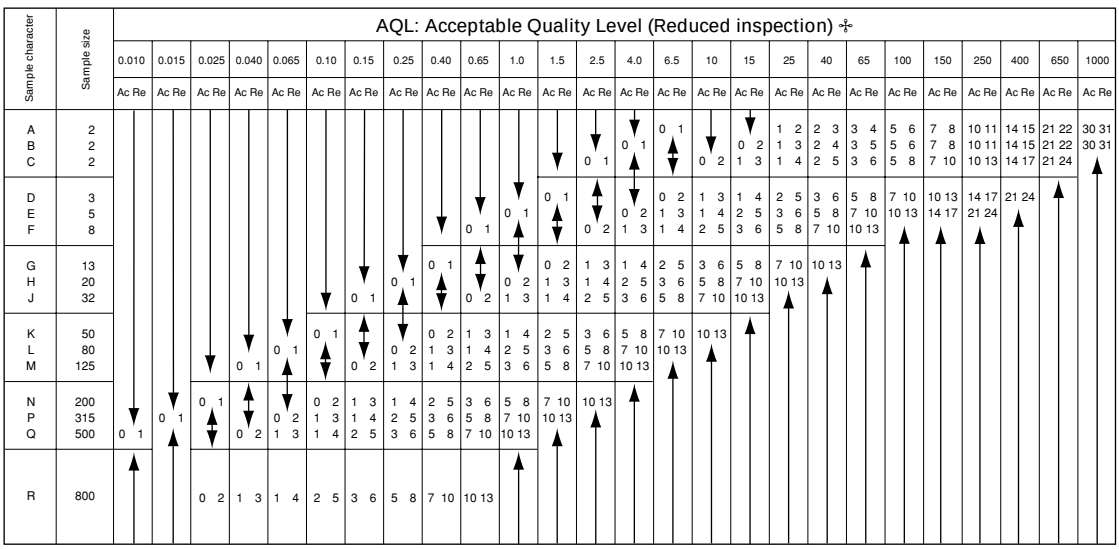
↓ = The first sampling plan below the arrow is used. If the sample size is larger than the lot size, the entire lot is inspected.

↑ = The first sampling plan above the arrow is used.

Ac = Acceptance number

Re = Rejection number

Table A-4 Reduced Inspection Single Sampling Method (Main sampling table)



ANSI / ASQC Z1.4

↓ = The first sampling plan below the arrow is used. If the sample size is larger than the lot size, the entire lot is inspected.

↑ = The first sampling plan above the arrow is used.

Ac = Acceptance number

Re = Rejection number

✣ = If the number of defects exceeds the acceptance number but does not reach the rejection number, that lot is accepted, but the inspection system returns to normal inspection from the next lot.

Table A-5 MIL-S-19500 Sampling Inspection Table

Confidence level 90%

Max. Percent Defective **(LTPD) or** λ	50	30	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2	0.15	0.1
Acceptance Number (a) **(r = a + 1)**	Minimum Sample Sizes																
0	5 (1.03)	8 (0.64)	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)	1152 (0.005)	1534 (0.003)	2303 (0.002)
1	8 (4.4)	13 (2.7)	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1290 (0.027)	1946 (0.018)	2592 (0.013)	3891 (0.009)
2	11 (7.4)	18 (4.5)	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)	2662 (0.031)	3547 (0.022)	5323 (0.015)
3	13 (10.5)	22 (6.2)	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)	3341 (0.041)	4452 (0.031)	6681 (0.018)
4	16 (12.3)	27 (7.4)3	38 (5.0)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)	3997 (0.040)	5327 (0.037)	7994 (0.025)
5	19 (13.8)	31 (8.3)	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)	4638 (0.056)	6181 (0.042)	9275 (0.028)
6	21 (15.6)	35 (9.4)	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)	5267 (0.062)	7019 (0.047)	10533 (0.031)
7	24 (16.6)	39 (10.2)	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	567 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)	5886 (0.067)	7845 (0.051)	11771 (0.034)
8	26 (18.1)	43 (10.9)	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)	6498 (0.072)	8660 (0.054)	12995 (0.036)
9	28 (19.4)	47 (11.5)	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)	7103 (0.077)	9468 (0.057)	14206 (0.038)
10	31 (19.9)	51 (12.1)	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)	7704 (0.080)	10268 (0.060)	15407 (0.040)
11	33 (21.0)	54 (12.8)	83 (8.3)	111 (6.2)	166 (4.2)	238 (2.9)	332 (2.1)	555 (1.2)	832 (0.83)	1109 (0.62)	1604 (0.42)	2378 (0.29)	3323 (0.21)	5546 (0.12)	8319 (0.083)	11092 (0.062)	15638 (0.042)
12	36 (21.4)	59 (13.0)	89 (8.6)	119 (6.5)	178 (4.3)	254 (3.0)	356 (2.2)	594 (1.3)	890 (0.86)	1187 (0.65)	1781 (0.43)	2544 (0.3)	3562 (0.22)	5936 (0.13)	8904 (0.089)	11872 (0.065)	17808 (0.043)
13	38 (22.3)	63 (13.4)	95 (8.9)	126 (6.7)	190 (4.5)	271 (3.1)	379 (2.26)	632 (1.3)	948 (0.89)	1264 (0.67)	1896 (0.44)	2709 (0.31)	3793 (0.22)	6321 (0.134)	9482 (0.089)	12643 (0.067)	18964 (0.045)
14	40 (23.1)	67 (13.8)	101 (9.2)	134 (6.9)	201 (4.6)	288 (3.2)	404 (2.3)	672 (1.4)	1007 (0.92)	1343 (0.69)	2015 (0.46)	2878 (0.32)	4029 (0.23)	6716 (0.138)	10073 (0.092)	13431 (0.069)	20146 (0.046)
15	43 (23.3)	71 (14.1)	107 (9.4)	142 (7.1)	213 (4.7)	305 (3.3)	426 (2.36)	711 (1.41)	1066 (0.94)	1422 (0.71)	2133 (0.47)	3046 (0.33)	4265 (0.235)	7108 (0.141)	10662 (0.094)	14216 (0.070)	21324 (0.047)
16	45 (24.1)	74 (14.6)	112 (9.7)	150 (7.2)	225 (4.8)	321 (3.37)	450 (2.41)	750 (1.44)	1124 (0.96)	1499 (0.72)	2249 (0.48)	3212 (0.337)	4497 (0.241)	7496 (0.144)	11244 (0.096)	14992 (0.072)	22487 (0.048)
17	47 (24.7)	79 (14.7)	118 (9.86)	158 (7.36)	236 (4.93)	338 (3.44)	473 (2.46)	788 (1.48)	1182 (0.98)	1576 (0.74)	2364 (0.49)	3377 (0.344)	4728 (0.246)	7880 (0.148)	11819 (0.098)	15759 (0.074)	23630 (0.049)
18	50 (24.9)	83 (15.0)	124 (10.0)	165 (7.54)	248 (5.02)	354 (3.51)	496 (2.51)	826 (1.51)	1239 (1.0)	1652 (0.75)	2478 (0.50)	3540 (0.351)	4956 (0.251)	8200 (0.151)	12390 (0.100)	16520 (0.075)	24780 (0.050)
19	52 (25.5)	86 (15.4)	130 (10.2)	173 (7.76)	259 (5.12)	370 (3.58)	518 (2.56)	864 (1.53)	1296 (1.02)	1728 (0.77)	2591 (0.52)	3702 (0.358)	5183 (0.256)	8638 (0.153)	12957 (0.102)	17276 (0.077)	25914 (0.051)
20	54 (26.1)	90 (15.6)	135 (10.4)	180 (7.82)	271 (5.19)	386 (3.65)	541 (2.60)	902 (1.56)	1353 (1.04)	1803 (0.78)	2705 (0.52)	3864 (0.364)	5410 (0.260)	9017 (0.156)	13526 (0.104)	18034 (0.078)	27061 (0.052)
25	65 (27.0)	109 (16.1)	163 (10.8)	217 (8.08)	326 (5.38)	466 (3.76)	652 (2.69)	1086 (1.61)	1629 (1.08)	2173 (0.807)	3259 (0.538)	4656 (0.376)	6518 (0.269)	10863 (0.161)	16295 (0.108)	21726 (0.081)	32589 (0.054)

3 Saturated Vapor Pressure Table

Table A-6 Saturated Water Vapor Pressure 1/4

Unit: Pa

t/℃	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
0.	611.21	615.67	620.15	624.67	629.21	633.78	638.38	643.01	647.67	652.36
1.	657.08	661.83	666.61	671.42	676.26	681.14	686.04	690.98	695.94	700.94
2.	705.97	711.03	716.13	721.26	726.41	731.61	736.83	742.09	747.38	752.70
3.	758.06	763.45	768.88	774.34	779.83	785.36	790.92	796.52	802.15	807.82
4.	813.52	819.26	825.03	830.84	836.69	842.57	848.49	854.45	860.44	866.47
5.	872.54	878.64	884.79	890.97	897.19	903.44	909.74	916.07	922.45	928.86
6.	935.31	941.80	948.34	954.91	961.52	968.17	974.86	981.60	988.37	995.19
7.	1002.0	1008.9	1015.9	1022.9	1029.9	1037.0	1044.1	1051.2	1058.4	1065.7
8.	1072.9	1080.3	1087.6	1095.1	1102.5	1110.0	1117.6	1125.2	1132.8	1140.5
9.	1148.2	1156.0	1163.8	1171.7	1179.6	1187.6	1195.6	1203.7	1211.8	1219.9
10.	1228.1	1236.4	1244.7	1253.0	1261.4	1269.9	1278.4	1286.9	1295.5	1304.2
11.	1312.9	1321.7	1330.5	1339.3	1348.2	1357.2	1366.2	1375.3	1384.4	1393.5
12.	1402.8	1412.1	1421.4	1430.8	1440.2	1449.7	1459.3	1468.9	1478.5	1488.2
13.	1498.0	1507.8	1517.7	1527.7	1537.7	1547.7	1557.9	1568.0	1578.3	1588.6
14.	1598.9	1609.3	1619.8	1630.3	1640.9	1651.6	1662.3	1673.0	1683.9	1694.8
15.	1705.7	1716.7	1727.8	1739.0	1750.2	1761.4	1772.8	1784.2	1795.6	1807.1
16.	1818.7	1830.4	1842.1	1853.9	1865.8	1877.7	1889.7	1901.7	1913.8	1926.0
17.	1938.3	1950.6	1963.0	1975.5	1988.0	2000.6	2013.3	2026.0	2038.8	2051.7
18.	2064.7	2077.7	2090.8	2104.0	2117.2	2130.5	2143.9	2157.4	2170.9	2184.5
19.	2198.2	2212.0	2225.8	2239.7	2253.7	2267.8	2281.9	2296.1	2310.4	2324.8
20.	2339.2	2353.8	2368.4	2383.1	2397.8	2412.7	2427.6	2442.6	2457.7	2472.9
21.	2488.2	2503.5	2518.9	2534.4	2550.0	2565.7	2581.4	2597.3	2613.2	2629.2
22.	2645.3	2661.5	2677.7	2694.1	2710.5	2727.1	2743.7	2760.4	2777.2	2794.1
23.	2811.0	2828.1	2845.2	2862.5	2879.8	2897.2	2914.8	2932.4	2950.1	2967.9
24.	2985.8	3003.7	3021.8	3040.0	3058.3	3076.6	3095.1	3113.6	3132.3	3151.1
25.	3169.9	3188.9	3207.9	3227.0	3246.3	3265.6	3285.1	3304.6	3324.3	3344.0
26.	3363.9	3383.8	3403.9	3424.0	3444.3	3464.7	3485.2	3505.7	3526.4	3547.2
27.	3568.1	3589.1	3610.2	3631.5	3652.8	3674.2	3695.8	3717.4	3739.2	3761.1
28.	3783.1	3805.2	3827.4	3849.7	3872.2	3894.7	3917.4	3940.2	3963.1	3986.1
29.	4009.2	4032.5	4055.8	4079.3	4102.9	4126.6	4150.5	4174.4	4198.5	4222.7
30.	4247.0	4271.5	4296.0	4320.7	4345.5	4370.5	4395.5	4420.7	4446.0	4471.5
31.	4497.0	4522.7	4548.5	4574.5	4600.5	4626.7	4653.1	4679.5	4706.1	4732.8
32.	4759.7	4786.7	4813.8	4841.0	4868.4	4895.9	4923.6	4951.4	4979.3	5007.4
33.	5035.6	5063.9	5092.4	5121.0	5149.7	5178.6	5207.7	5236.8	5266.2	5295.6
34.	5325.2	5355.0	5384.8	5414.9	5445.1	5475.4	5505.9	5536.5	5567.2	5598.1
35.	5629.2	5660.4	5691.8	5723.3	5754.9	5786.8	5818.7	5850.8	5883.1	5915.5
36.	5948.1	5980.8	6013.7	6046.8	6080.0	6113.3	6146.9	6180.5	6214.4	6248.4
37.	6282.5	6316.9	6351.3	6386.0	6420.8	6455.8	6490.9	6526.2	6561.7	6597.3
38.	6633.1	6669.1	6705.2	6741.5	6778.0	6814.7	6851.5	6888.5	6925.6	6963.0
39.	7000.5	7038.2	7076.0	7114.1	7152.3	7190.7	7229.2	7268.0	7306.9	7346.0
40.	7385.3	7424.8	7464.4	7504.2	7544.3	7584.5	7624.8	7665.4	7706.2	7747.1
41.	7788.2	7829.6	7871.1	7912.8	7954.6	7996.7	8039.0	8081.5	8124.1	8167.0
42.	8210.0	8253.2	8296.7	8340.3	8384.1	8428.2	8472.4	8516.8	8561.5	8606.3
43.	8651.3	8696.5	8742.0	8787.6	8833.5	8879.5	8925.8	8972.3	9018.9	9065.8
44.	9112.9	9160.2	9207.7	9255.5	9303.4	9351.6	9399.9	9448.5	9497.3	9546.3
45.	9595.6	9645.0	9694.7	9744.6	9794.7	9845.0	9895.6	9946.4	9997.4	10049.
46.	10100.	10152.	10204.	10256.	10308.	10361.	10414.	10467.	10520.	10573.
47.	10627.	10681.	10735.	10790.	10845.	10899.	10955.	11010.	11066.	11122.
48.	11178.	11234.	11291.	11348.	11405.	11462.	11520.	11578.	11636.	11694.
49.	11753.	11812.	11871.	11930.	11990.	12049.	12110.	12170.	12231.	12292.
50.	12353.	12414.	12476.	12538.	12600.	12663.	12725.	12788.	12852.	12915.

Remarks: From SONNTAG (1990). The temperature scale is ITS-90.

Unit: Pa

t/℃	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
51.	12979.	13043.	13107.	13172.	13237.	13302.	13368.	13433.	13499.	13566.
52.	13632.	13699.	13766.	13833.	13901.	13969.	14037.	14106.	14175.	14244.
53.	14313.	14383.	14453.	14523.	14594.	14665.	14736.	14807.	14879.	14951.
54.	15023.	15096.	15169.	15242.	15316.	15389.	15464.	15538.	15613.	15688.
55.	15763.	15839.	15915.	15991.	16068.	16145.	16222.	16299.	16377.	16455.
56.	16534.	16613.	16692.	16771.	16851.	16931.	17012.	17093.	17174.	17255.
57.	17337.	17419.	17501.	17584.	17667.	17750.	17834.	17918.	18003.	18087.
58.	18173.	18258.	18344.	18430.	18516.	18603.	18690.	18778.	18866.	18954.
59.	19043.	19131.	19221.	19310.	19400.	19491.	19581.	19672.	19764.	19856.
60.	19948.	20040.	20133.	20226.	20320.	20414.	20508.	20603.	20698.	20793.
61.	20889.	20985.	21082.	21179.	21276.	21374.	21472.	21571.	21669.	21769.
62.	21868.	21968.	22069.	22170.	22271.	22372.	22474.	22577.	22679.	22783.
63.	22886.	22990.	23094.	23199.	23304.	23410.	23516.	23622.	23729.	23836.
64.	23944.	24052.	24160.	24269.	24379.	24488.	24598.	24709.	24820.	24931.
65.	25043.	25155.	25268.	25381.	25494.	25608.	25723.	25837.	25953.	26068.
66.	26184.	26301.	26418.	26535.	26653.	26772.	26890.	27010.	27129.	27249.
67.	27370.	27491.	27612.	27734.	27857.	27979.	28103.	28226.	28351.	28475.
68.	28600.	28726.	28852.	28979.	29106.	29233.	29361.	29489.	29618.	29748.
69.	29877.	30008.	30138.	30270.	30402.	30534.	30667.	30800.	30933.	31068.
70.	31202.	31338.	31473.	31609.	31746.	31883.	32021.	32159.	32298.	32437.
71.	32577.	32717.	32858.	32999.	33140.	33283.	33425.	33569.	33713.	33857.
72.	34002.	34147.	34293.	34439.	34586.	34734.	34882.	35030.	35179.	35329.
73.	35479.	35630.	35781.	35933.	36085.	36238.	36391.	36545.	36700.	36855.
74.	37010.	37166.	37323.	37480.	37638.	37796.	37955.	38115.	38275.	38436.
75.	38597.	38758.	38921.	39084.	39247.	39411.	39576.	39741.	39907.	40073.
76.	40240.	40408.	40576.	40744.	40914.	41084.	41254.	41425.	41597.	41769.
77.	41942.	42116.	42290.	42464.	42640.	42815.	42992.	43169.	43347.	43525.
78.	43704.	43884.	44064.	44245.	44426.	44608.	44791.	44974.	45158.	45343.
79.	45528.	45714.	45900.	46088.	46275.	46464.	46653.	46843.	47033.	47224.
80.	47416.	47608.	47801.	47994.	48189.	48384.	48579.	48776.	48972.	49170.
81.	49368.	49567.	49767.	49967.	50168.	50370.	50572.	50775.	50979.	51183.
82.	51388.	51594.	51800.	52007.	52215.	52424.	52633.	52843.	53053.	53265.
83.	53477.	53689.	53903.	54117.	54332.	54547.	54764.	54981.	55198.	55417.
84.	55636.	55856.	56076.	56298.	56520.	56743.	56966.	57190.	57415.	57641.
85.	57868.	58095.	58323.	58552.	58781.	59011.	59242.	59474.	59707.	59940.
86.	60174.	60409.	60644.	60881.	61118.	61356.	61594.	61834.	62074.	62315.
87.	62557.	62799.	63042.	63286.	63531.	63777.	64024.	64271.	64519.	64768.
88.	65017.	65268.	65519.	65771.	66024.	66278.	66532.	66788.	67044.	67301.
89.	67559.	67817.	68077.	68337.	68598.	68860.	69123.	69386.	69651.	69916.
90.	70182.	70449.	70717.	70986.	71255.	71526.	71797.	72069.	72342.	72616.
91.	72890.	73166.	73442.	73719.	73998.	74277.	74556.	74837.	75119.	75401.
92.	75685.	75969.	76254.	76540.	76827.	77115.	77404.	77693.	77984.	78276.
93.	78568.	78861.	79155.	79450.	79746.	80043.	80341.	80640.	80940.	81240.
94.	81542.	81844.	82148.	82452.	82757.	83064.	83371.	83679.	83988.	84298.
95.	84609.	84921.	85234.	85547.	85862.	86178.	86495.	86812.	87131.	87451.
96.	87771.	88093.	88415.	88739.	89063.	89389.	89715.	90043.	90371.	90701.
97.	91031.	91362.	91695.	92028.	92363.	92698.	93035.	93372.	93711.	94050.
98.	94391.	94732.	95075.	95418.	95763.	96109.	96455.	96803.	97152.	97502.
99.	97853.	98204.	98557.	98911.	99266.	99623.	99980.	100338.	100697.	101058.
100.	101419.	101782.	102145.	102510.	102875.	103242.	103610.	103979.	104349.	104720.

Remarks: From SONNTAG (1990). The temperature scale is ITS-90.

Table A-6 Saturated Water Vapor Pressure 3/4

Unit: kPa

t/℃	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
100.	101.4	101.8	102.1	102.5	102.9	103.2	103.6	104.0	104.3	104.7
101.	105.1	105.5	105.8	106.2	106.6	107.0	107.3	107.7	108.1	108.5
102.	108.9	109.3	109.6	110.0	110.4	110.8	111.2	111.6	112.0	112.4
103.	112.8	113.2	113.6	114.0	114.4	114.8	115.2	115.6	116.0	116.4
104.	116.8	117.2	117.6	118.0	118.4	118.8	119.2	119.7	120.1	120.5
105.	120.9	121.3	121.7	122.2	122.6	123.0	123.4	123.9	124.3	124.7
106.	125.1	125.6	126.0	126.4	126.9	127.3	127.8	128.2	128.6	129.1
107.	129.5	130.0	130.4	130.8	131.3	131.7	132.2	132.6	133.1	133.6
108.	134.0	134.5	134.9	135.4	135.8	136.3	136.8	137.2	137.7	138.2
109.	138.6	139.1	139.6	140.0	140.5	141.0	141.5	141.9	142.4	142.9
110.	143.4	143.9	144.3	144.8	145.3	145.8	146.3	146.8	147.3	147.8
111.	148.3	148.8	149.3	149.8	150.3	150.8	151.3	151.8	152.3	152.8
112.	153.3	153.8	154.3	154.8	155.3	155.8	156.4	156.9	157.4	157.9
113.	158.4	159.0	159.5	160.0	160.5	161.6	161.6	162.1	162.7	163.2
114.	163.7	164.3	164.8	165.4	165.9	166.4	167.0	167.5	168.1	168.6
115.	169.2	169.7	170.3	170.8	171.4	172.0	172.5	173.1	173.6	174.2
116.	174.8	175.3	175.9	176.5	177.0	177.6	178.2	178.8	179.4	179.9
117.	180.5	181.1	181.7	182.3	182.9	183.4	184.0	184.6	185.2	185.8
118.	186.4	187.0	187.6	188.2	188.8	189.4	190.0	190.6	191.2	191.8
119.	192.5	193.1	193.7	194.3	194.9	195.5	196.2	196.8	197.4	198.0
120.	198.7	199.3	199.9	200.6	201.2	201.8	202.5	203.1	203.8	204.4
121.	205.0	205.7	206.3	207.0	207.6	208.3	208.9	209.6	210.3	210.9
122.	211.6	212.2	212.9	213.6	214.2	214.9	215.6	216.3	216.9	217.6
123.	218.3	219.0	219.7	220.3	2210.	221.7	222.4	223.1	223.8	224.5
124.	225.2	225.9	226.6	227.3	228.0	228.7	229.4	230.1	230.8	231.5
125.	232.2	232.9	233.7	234.4	235.1	235.8	236.6	237.3	238.0	238.7
126.	239.5	240.2	240.9	241.7	242.4	243.2	243.9	244.6	245.4	246.1
127.	246.9	247.6	248.4	249.2	249.9	250.7	251.4	252.2	253.0	253.7
128.	254.5	255.3	256.0	256.8	257.6	258.4	259.1	259.9	260.7	261.5
129.	262.3	263.1	263.9	264.7	265.5	266.3	267.1	267.9	268.7	269.5
130.	270.3	271.1	271.9	272.7	273.5	274.3	275.2	276.0	276.8	277.6
131.	278.5	279.3	280.1	281.0	281.8	282.6	283.5	284.3	285.1	286.0
132.	286.8	287.7	288.5	289.4	290.3	291.1	292.0	292.8	293.7	294.6
133.	295.4	296.3	297.2	298.0	298.9	299.8	300.7	301.6	302.4	303.3
134.	304.2	305.1	306.0	306.9	307.8	308.7	309.6	310.5	311.4	312.3
135.	313.2	314.1	315.1	316.0	316.9	317.8	318.7	319.7	320.6	321.5
136.	322.4	323.4	324.3	325.3	326.2	327.1	328.1	329.0	330.0	330.9
137.	331.9	332.8	333.8	334.8	335.7	336.7	337.6	338.6	339.6	340.6
138.	341.5	342.5	343.5	344.5	345.5	346.5	347.4	348.4	349.4	350.4
139.	351.4	352.4	353.4	354.4	355.4	356.4	357.5	358.5	359.5	360.5
140.	361.5	362.6	363.6	364.6	365.6	366.7	367.7	368.8	369.8	370.8
141.	371.9	372.9	374.0	375.0	376.1	377.1	378.2	379.3	380.3	381.4
142.	382.5	383.5	384.6	385.7	386.8	387.8	388.9	390.0	391.1	392.2
143.	393.3	394.4	395.5	396.6	397.7	398.8	399.9	401.0	402.1	403.2
144.	404.4	405.5	406.6	407.7	408.9	410.0	411.1	412.3	413.4	414.5
145.	415.7	416.8	418.0	419.1	420.3	421.4	422.6	423.8	424.9	426.1
146.	427.3	428.4	429.6	430.8	432.0	433.1	434.3	435.5	436.7	437.9
147.	439.1	440.3	441.5	442.7	443.9	445.1	446.3	447.5	448.7	450.0
148.	451.2	452.4	453.6	454.9	456.1	457.3	458.6	459.8	461.0	462.3
149.	463.5	464.8	466.0	467.3	468.5	469.8	471.1	472.3	473.6	474.9
150.	476.2	477.4	478.7	480.0	481.3	482.6	483.9	485.2	486.5	487.8

Remarks: From WAGNER & PRUSS (1993). The temperature scale is ITS-90.

Unit: kPa

t/℃	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9
150.	476.2	489.1	502.2	515.7	529.5	543.5	557.8	572.5	587.4	602.7
160.	618.2	634.1	650.3	666.9	683.7	700.9	718.5	736.4	754.6	773.2
170.	792.2	811.5	831.2	851.3	871.8	892.6	913.8	935.5	957.5	980.0
180.	1003.	1026.	1050.	1074.	1098.	1123.	1149.	1175.	1201.	1228.
190.	1255.	1283.	1311.	1340.	1369.	1399.	1429.	1460.	1491.	1523.
200.	1555.	1588.	1621.	1655.	1689.	1724.	1760.	1796.	1833.	1870.
210.	1908.	1946.	1985.	2025.	2065.	2106.	2147.	2189.	2232.	2276.
220.	2320.	2364.	2410.	2456.	2502.	2550.	2598.	2647.	2696.	2746.
230.	2797.	2849.	2901.	2954.	3008.	3063.	3118.	3174.	3231.	3289.
240.	3347.	3406.	3466.	3527.	3589.	3651.	3715.	3779.	3844.	3909.
250.	3976.	4044.	4112.	4182.	4252.	4323.	4395.	4468.	4542.	4617.
260.	4692.	4769.	4847.	4925.	5005.	5085.	5167.	5249.	5333.	5417.
270.	5503.	5590.	5677.	5766.	5856.	5946.	6038.	6131.	6225.	6320.
280.	6417.	6514.	6612.	6712.	6813.	6915.	7018.	7122.	7227.	7334.
290.	7442.	7551.	7661.	7772.	7885.	7999.	8114.	8231.	8348.	8468.
300.	8588.	8710.	8832.	8957.	9082.	9209.	9338.	9467.	9599.	9731.
310.	9865.	10000.	10137.	10275.	10415.	10556.	10699.	10843.	10988.	11136.
320.	11284.	11434.	11586.	11740.	11895.	12051.	12209.	12369.	12530.	12693.
330.	12858.	13024.	13193.	13362.	13534.	13707.	13882.	14059.	14238.	14418.
340.	14601.	14785.	14971.	15159.	15349.	15541.	15734.	15930.	16128.	16328.
350.	16529.	16733.	16939.	17147.	17358.	17570.	17785.	18002.	18221.	18442.
360.	18666.	18892.	19121.	19352.	19586.	19822.	20061.	20302.	20546.	20794.
370.	21044.	21297.	21554.	21814.	22064.*					

Note*: Critical point 373.946℃
Remarks: From WAGNER & PRUSS (1993). The temperature scale is ITS-90.

4 Basic Reliability Theory

4.1 Measures for Representing Reliability

Measures used to quantitatively represent reliability and their definitions are described below.

(1) Reliability: R(t)

Reliability indicates the probability for functioning correctly without failure until time t.

When n samples are used under the same conditions, if the number of failures occurring until time t has elapsed is expressed as r(t), then the reliability R(t) is given by the following equation.

$$R(t) = \frac{n - r(t)}{n}$$

(2) Failure Distribution Function (Unreliability): F(t)

This indicates the probability of failure occurring until time t, and is expressed by the following equation.

$$F(t) = \frac{r(t)}{n}$$

In addition, the following relationship is established between unreliability F(t) and reliability R(t).

$$R(t)+F(t)=1$$

As shown in Fig. A-3, R(t) decreases from 1 over time, while conversely F(t) increases from 0 toward 1 over time.

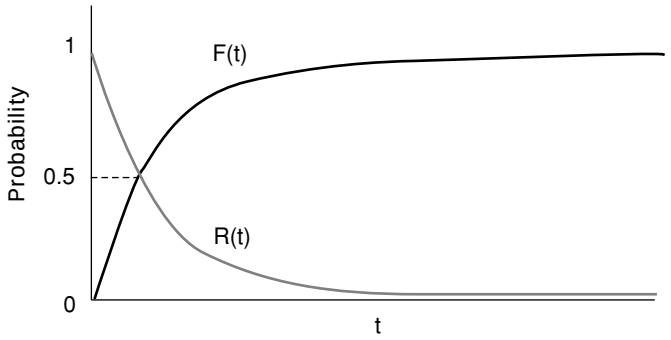


Fig. A-3 Relationship between F(t) and R(t)

(3) Failure Probability Density Function: f(t)

This represents the probability of failure occurring per unit time when time t has elapsed.

$$f(t) = \frac{dF(t)}{dt} = -\frac{dR(t)}{dt}$$

(4) Failure Rate Function: λ (t)

This represents the probability of failure occurring in the next unit time for samples which have not yet failed when time t has elapsed.

$$\lambda(t) = \frac{f(t)}{1 - F(t)} = \frac{f(t)}{R(t)}$$

4.2 Distributions Used in Reliability Analysis

Reliability analysis is a method for estimating the above-mentioned reliability measures. There are two types of methods: the parametric method which estimates reliability by postulating the distribution and the non-parametric method which does not postulate the distribution. However, data analysis for semiconductor devices generally uses the parametric method which has higher accuracy.

Typical distribution functions used to analyze reliability data are described below.

(1) Normal Distribution

The normal distribution is a typical continuous distribution used for quality control. In reliability analysis it is often applied to wear-out life where failures concentrate around a certain time.

The probability density function f(t) and distribution function F(t) are as follows.

$$f(t) = \frac{1}{\sqrt{2\pi}\sigma} \exp\{-\frac{(t-\mu)^2}{2\sigma^2}\} \qquad (-\infty < t < +\infty)$$

$$F(t) = \frac{1}{\sqrt{2\pi}\sigma} \int_{-\infty}^{t} \exp\{-\frac{(x-\mu)^2}{2\sigma^2}\} dx \quad (-\infty < t < +\infty)$$

This distribution is given by the mean parameter μ and the dispersion (variance) parameter σ.

As shown in Fig. A-4 below, the normal distribution has a symmetrical bell shape centering on μ, and the probability of the value t being contained within the range of $\pm\sigma$, $\pm 2\sigma$ and $\pm 3\sigma$ to both sides of μ is 68.26%, 95.44% and 99.7%, respectively.

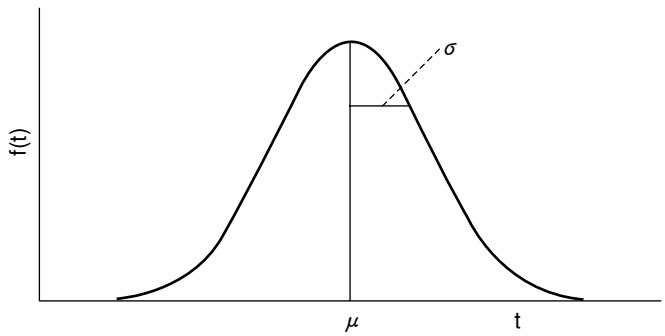


Fig. A-4 Normal Distribution

(2) Exponential Distribution

The exponential distribution represents the life distribution in the random failure region where the failure rate λ is constant over time.

The probability density function f(t) and reliability R(t) are as follows.

$$f(t) = \lambda e^{-\lambda t}$$
$$R(t) = e^{-\lambda t}$$

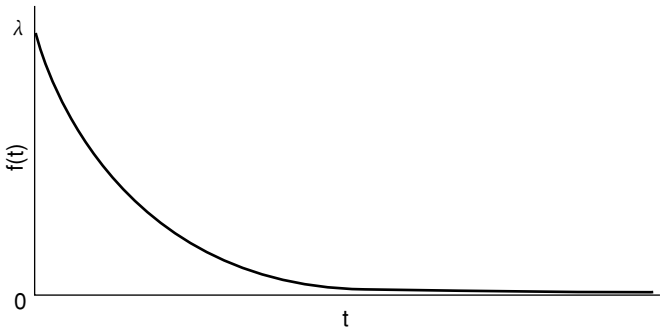


Fig. A-5 Exponential Distribution

The mean time to failure (MTTF) is given as follows from t_0, which is the inverse of the failure rate λ .

$1/\lambda = t_0$ = MTTF (Mean Time To Failure)

In semiconductor device reliability, the electromigration life and hot carrier life are generally known to follow a logarithmic normal distribution.

(3) Logarithmic Normal Distribution

The logarithmic normal distribution is a distribution function where lnt, which is the logarithm of the life time t, follows the above mentioned normal distribution.

The probability density function f(t) and distribution function F(t) are as follows.

$$f(t) = \frac{1}{\sqrt{2\pi}\sigma t} \exp\left[-\frac{1}{2}\left(\frac{1nt-\mu}{\sigma}\right)^2\right] \quad (0 < t < \infty)$$

$$F(t) = \frac{1}{\sqrt{2\pi}\sigma} \int_0^F \frac{1}{x} \exp\left[-\frac{1}{2}\left(\frac{1nx-\mu}{\sigma}\right)^2\right] dx$$

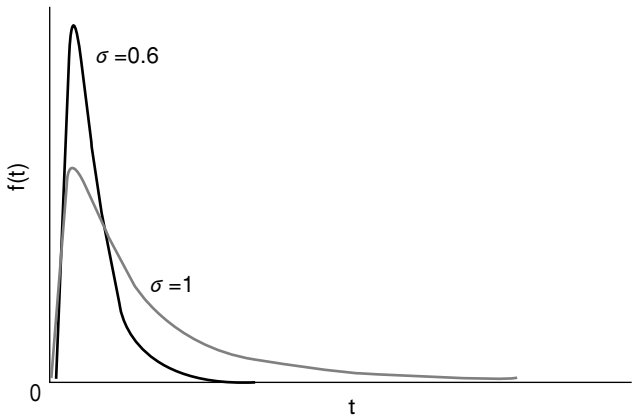


Fig. A-6 Logarithmic Normal Distribution

(4) Weibull Distribution

The Weibull distribution is a highly general-purpose distribution function which is expanded from the logarithmic distribution. In reliability data analysis, this model is frequently used to analyze life data in reliability tests, etc.

The probability density function f(t) and distribution function F(t) of this distribution are as follows.

$$f(t) = \frac{m}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{m-1} \exp\{-\left(\frac{t-\gamma}{\eta}\right)^{m}\}$$

$$F(t) = 1 - \exp\{-\left(\frac{t-\gamma}{\eta}\right)^{m}\}$$

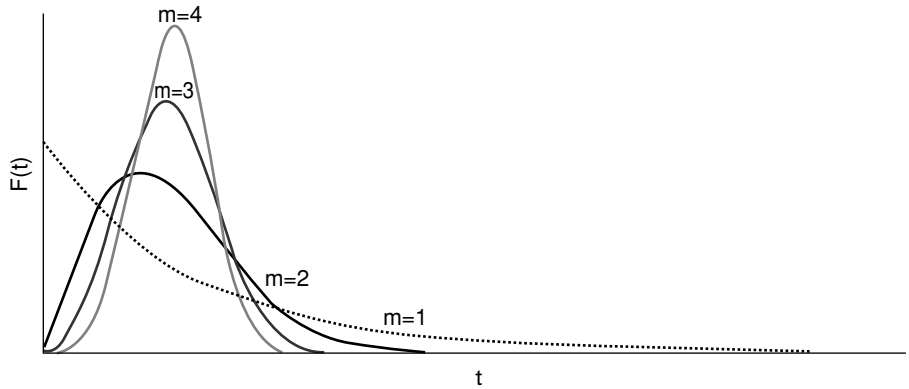


Fig. A-7 Weibull Distribution

Here, m is called the form parameter, η the measure parameter, and γ the position parameter.

In addition, assuming $t_0 = \eta^m$ (= characteristic life), the failure rate γ (t) is expressed by the following equation.

$$\lambda(t) = \frac{m}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{m-1} = \frac{m}{t_0}\, t^{m-1}$$

The following information concerning the failure pattern can be obtained from the value of the form parameter m.

m value:	Failure pattern
0 < m < 1:	Initial failure (DFR) pattern where the failure rate decreases over time
m = 1:	Random failure (CFR) pattern where the failure rate is constant (matches with the exponential distribution)
m > 1:	Wear-out failure (IFR) pattern where the failure rate increases over time

4.3 Example Data Analysis Method

This section describes an example reliability data analysis method using Weibull probability paper.

Weibull distributions are generally used to analyze life data, and this is because Weibull distributions can approximate the normal distribution, logarithmic normal distribution and exponential distribution life distribution models. In addition, Weibull distributions also have the advantage of allowing analysis even when two or more failure modes are present at the same time.

(1) Data analysis method using Weibull probability paper

Weibull probability paper makes it possible to estimate reliability distribution parameters more easily than by calculation from theoretical equations.

As mentioned above, the Weibull distribution failure distribution function is expressed by the following equation.

$$F(t) = 1 - \exp\{-\left(\frac{t-\gamma}{\eta}\right)^m\}$$

When $\gamma = 0$, the above equation changes as follows.

$$F(t) = 1 - \exp\left\{-\left(\frac{t}{\eta}\right)^m\right\}$$

Taking the natural logarithm of both sides two times, the equation can be transformed as follows.

$$1n1n\frac{1}{1-F(t)} = m1nt - m1n\eta$$

Replacing with X and Y,

$$X = 1nt$$

$$Y = 1n1n\frac{1}{1-F(t)}$$

This equation becomes a linear first-degree equation with X and Y as follows.

$Y = mX - mln\ \eta$

Weibull probability paper is scaled paper which uses this relational formula to plot Y = lnln (1/(1–F(t)) on the vertical axis and X = lnt on the horizontal axis. By plotting the X and Y data on Weibull probability plotting paper, the value of m can be easily obtained from the slope of the resulting straight line, and the value of η from the time t at which Y = 0.

(2) Data Analysis Procedure

A specific data analysis procedure using Weibull probability paper is described below. (See Fig. A-8.)

<Step 1> Arrange the obtained n life data in order from the smallest.

<Step 2> Obtain the cumulative failure rate F(t) for the ith failure data from the following equation.

(1) Mean rank method

$$\frac{i}{n+1} \times 100(\%)$$

(2) Median rank method

$$\frac{i-0.3}{n+0.4} \times 100(\%)$$

<Step 3> Plot the obtained life data on the Weibull probability paper as follows.

Horizontal axis t	Vertical axis F(t)
t_1	$F(t_1)$
t_2	$F(t_2)$
⋮	⋮
t_i	$F(t_i)$
⋮	⋮
t_n	$F(t_n)$

<Step 4> Draw an appropriate straight line through the plotted n points. At this time, make sure the line passes through the plotted points in the vertical axis range of F(t) = 30% to 70%. Even if the line does not pass through the plotted points in the range of F(t) = 10% or less or 90% or more, there is no substantial error.

<Step 5> Draw a straight line parallel to the line in Step 4 and passing through the “m estimated point”. Read the vertical (lnln 1/(1–F(t)) axis scale to the right of the point where this line intersects with the vertical main axis (lnt = 0). The absolute value of this value is the estimated value of form parameter m.

<Step 6> The estimated value of measure parameter η can be obtained by reading the t axis scale at the intersection between the line in Step 4 and the horizontal main axis (Y = 0).

<Step 7> The MTTF is obtained by reading the μ / η measure scale at the m point obtained in Step 5, and multiplying this value by the value of η obtained in Step 6.

<Step 8> The unreliability F(tx) at time tx is obtained by reading the Y sub-axis F(t) value at tx on the straight line. In addition, the reliability R(tx) can be obtained from R(tx) = 100–F(tx).

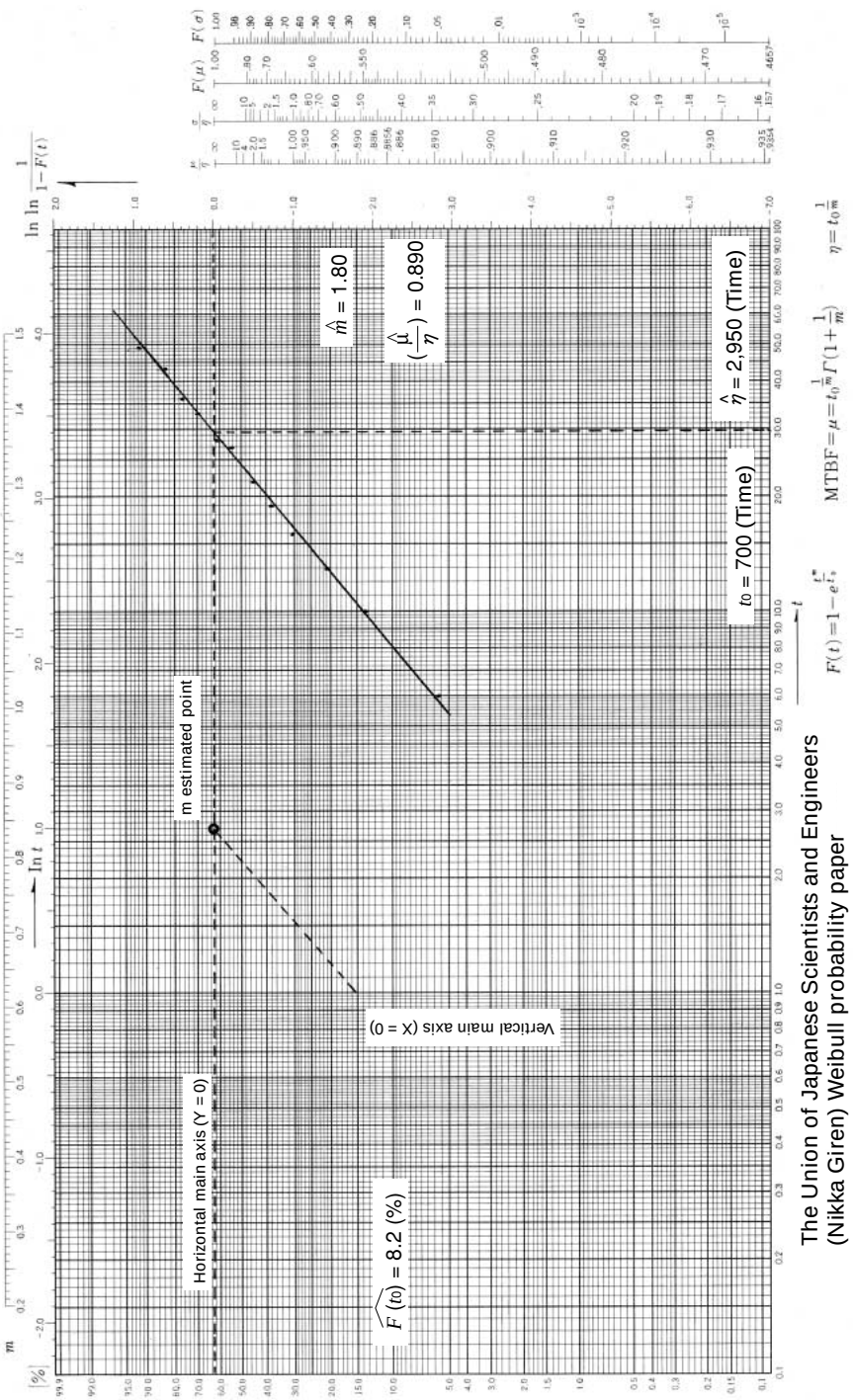


Fig. A-8 Example of Date Analysis Using Weibull Probability Paper

The Union of Japanese Scientists and Engineers
(Nikka Giren) Weibull probability paper

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