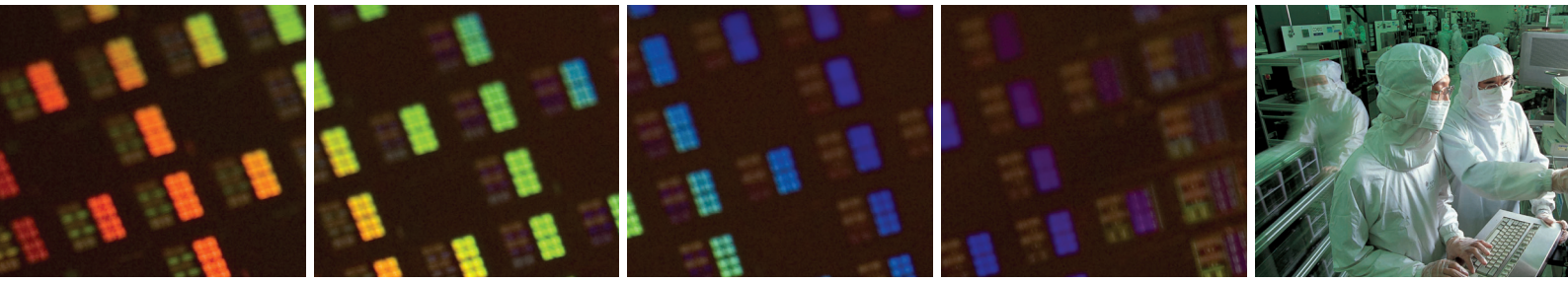
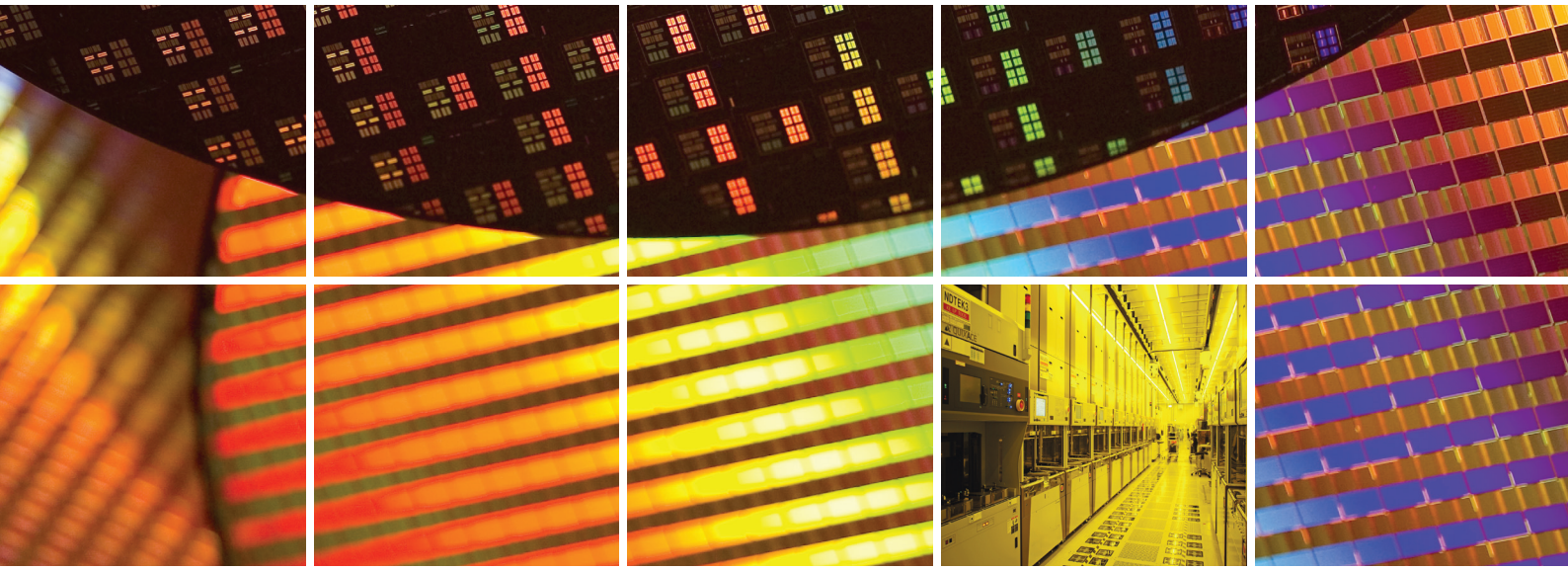
Open Innovation Platform™



Open Innovation Platform™



Open Innovation Platform™ (OIP)

Overview

The TSMC Open Innovation Platform is a comprehensive design technology infrastructure that encompasses all critical IC implementation areas to reduce design barriers and improve first-time silicon success. OIP promotes the speedy implementation of innovation amongst the semiconductor design community, its ecosystem partners and TSMC's IP, design implementation and DFM capabilities, process technology and backend services.

A key element of the Open Innovation Platform is a set of ecosystem interfaces and collaborative components initiated and supported by TSMC that more efficiently empowers innovation throughout the supply chain and in turn, drives the creation and sharing of newly-created revenue and profits. TSMC's Active Accuracy Assurance™ (AAA) initiative is critical to the Open Innovation Platform, providing the accuracy and quality required by the ecosystem interfaces and collaborative components.

Hosted by TSMC and built on the company's design-enabling building blocks and an ecosystem interface, the Open Innovation Platform is available to customers and ecosystem partners to improve time-to-market, increase return on investment, and reduce waste. The platform includes:

- The foundry segment's largest, most complete silicon-proven IP and library portfolio
- Advanced design methodology delivery through reference flows, design for manufacturing (DFM), and process design kits
- Comprehensive design ecosystem alliance programs covering market-leading EDA, library, IP, and design services suppliers

TSMC Libraries and IP

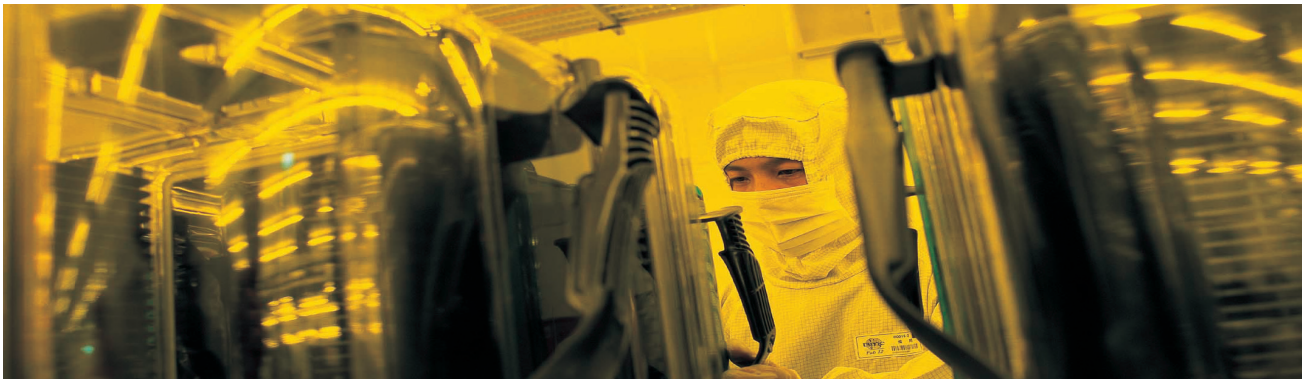
TSMC, in collaboration with industry leaders, provides the most comprehensive portfolio of libraries and silicon-proven IP in the foundry segment. These TSMC-specific libraries and IP are checked against TSMC's quality requirements and TSMC's DFM compliance standards to provide shorter design cycle time, increased first-time silicon success, and faster time-to-production.

TSMC's portfolio includes over 1,000 IP macros and 550 libraries from over 20 IP suppliers across TSMC process technologies, including the 0.35-micron, 0.25-micron, 0.18-micron, 0.13-micron, 90nm, 65nm, 40nm, and 28nm nodes. Libraries are also available for TSMC's 0.22-micron, 0.15-micron, 0.11-micron, 80nm, and 55nm half-nodes.

Standard Cell and I/O Libraries

The TSMC Design Infrastructure ecosystem provides state-of-the-art standard cell techniques for TSMC's process-optimized library portfolio. Designers choose from a large selection of TSMC and third-party standard cell libraries to meet their needs for area, power, speed, or the best tradeoff among the three.

The libraries contain features for high density, multiple-threshold, multiple Vdd, back-bias control, low power control, and a proprietary routing methodology. In addition, many libraries facilitate migration to TSMC half-nodes with little or no additional design.



	0.35µm	0.25µm	0.18µm	0.15µm	0.13µm	90nm	65nm	40nm	28nm
High Speed Standard Cell					ARM, Dolphin Tech	ARM, Dolphin Tech	ARM, Dolphin Tech,TSMC	ARM, Dolphin Tech,TSMC	ARM, Dolphin Tech,TSMC
High Density Standard Cell	TSMC	ARM	ARM, Dolphin integration, TSMC	ARM, TSMC	ARM, Virage, Dolphin integration, Dolphin Tech, TSMC	ARM, Dolphin Tech, TSMC, Virage	ARM, Dolphin Tech, TSMC, Virage	ARM, Dolphin Tech, TSMC, Virage	ARM, Dolphin Tech, TSMC, Virage
Ultra High Density Standard Cell			Dolphin integration	TSMC	ARM, Dolphin integration, Dolphin Tech, Virage	ARM, Dolphin Tech, TSMC	Dolphin Tech	Virage, Dolphin Tech	Virage, Dolphin Tech
Low Power Standard Cell			Dolphin integration		Dolphin Tech	Dolphin Tech, TSMC	ARM, Dolphin Tech, TSMC	ARM, Dolphin Tech, TSMC	ARM, Dolphin Tech, TSMC
I/O Library	TSMC	ARM, TSMC	ARM, TSMC	ARM, TSMC	ARM, Dolphin Tech, TSMC	ARM, Dolphin Tech, TSMC	ARM, Dolphin Tech, TSMC	ARM, Dolphin Tech, TSMC	ARM, Dolphin Tech, TSMC

Memory Compilers

TSMC and its partners offer a set of five standard memory compilers and a large number of specialized memories to address system-on-chip (SoC) embedded memory needs. The five standard memory compilers include single- and dual-port SRAM, 1P/2P register files, and Via/Diff ROM compilers. The SRAM compilers use TSMC's high-density bit cells for maximum density on a smaller chip area. Both single-port and dual-port SRAM compliers generate SRAM instances of up to 8 Mbits. TSMC's high current bit cell and ultra-low leakage bit cell lead our memory partners to create single- and dual-port SRAM compilers for maximum speed or minimum leakage. In addition, redundant row or column features are available in all process nodes (except 0.25-micron) for high yielding volume production.

	0.35µm	0.25µm	0.18µm	0.15µm	0.13µm	90nm	65nm	40nm	28nm
High Density Compilers	TSMC	ARM, Virage	ARM, Virage	ARM, Virage	ARM, Dolphin Tech, Virage	ARM, Dolphin Integration, Dolphin Tech, Virage,	ARM, Dolphin Integration, Dolphin Tech, Virage,	ARM, Dolphin Tech, TSMC, Virage	ARM, Dolphin Tech, TSMC, Virage
High Speed Compilers	TSMC		Virage	Virage	ARM, Dolphin Tech, Virage	ARM, Dolphin Tech, TSMC, Virage	ARM, Dolphin Tech, TSMC, Virage	ARM, Dolphin Tech, TSMC, Virage	ARM, Dolphin Tech, TSMC, Virage
Low Power Compilers		Dolphin Integration	Dolphin Integration		Dolphin Integration, Dolphin Tech, Virage	Dolphin Integration, Dolphin Tech, TSMC, Virage,	Dolphin Integration, Dolphin Tech, TSMC, Virage	Dolphin Tech, TSMC, Virage,	Dolphin Tech, TSMC, Virage,

Mixed-Signal IP

TSMC and its partners provide process-optimized mixed-signal IP that covers a wide range of specifications. Clock generating de-skewing PLLs provide competitive specifications in frequency range and jitter. ADC and DAC feature a wide range of specifications in resolution, sample rate, linearity, and area required in applications ranging from digital consumer and mobile applications to graphic processing and server chip sets.

IP	Vendors
PLL	Analog Bits, Cadence, GUC, MIPS, S3, TCI, TSMC
DLL	Analog Bits, Dolphin Technology, Prism, TCI
ADC	Cadence, Cosmic Circuits, Dolphin Integration, IP goal, MIPS, S3, Snowbush, TSMC
DAC	Cadence, Cosmic Circuits, Dolphin Integration, GUC, IP goal, MIPS, S3, Snowbush, TSMC
Voltage Regulator	Cosmic Circuits, GUC, MIPS, TSMC

Embedded Processor and DSP

TSMC's embedded processor partners provide IP support, complete with EDA, test, and software/hardware co-designs systems, to shorten design cycles and enhance first-time silicon success. TSMC works closely with its partners to provide the easiest access to processor and DSP cores. For example, the single usage foundry program provides silicon-validated RISC processors that create a low cost-of-adoption business model for ARM cores at the 0.25-micron, 0.18-micron, 0.13-micron, 90nm, and 65nm process nodes. TSMC also provides licensable design kits for ARM926 and ARM1176 at 90nm, 65nm, 40nm, and 28nm nodes.

IP	Vendor
ARM7, ARM9, ARM9E, ARM10E, ARM11, Cortex families	ARM
4KE, 24K, 34K	MIPS
Ceva-X, Palm, Teak, TeakLite	Ceva
ARC600, 700, ARC FPX, ARC XY	Virage
Diamond, Xtensa	Tensilica

Electrical Fuse

TSMC's Electrical Fuse IP is one-time programmable (OTP) non-volatile memory (NVM) based on programming a fuse. TSMC offers two electrical fuse IP types - serial interface and random accessible. Electrical fuses are used in chip ID, memory redundancy, feature selection, security keys, and parameter trimming. Starting at the 0.13-micron process node, TSMC provides high density enhanced random accessible IP featuring an extremely compact bit cell size to facilitate redundan circuit design in high density embedded SRAM blocks. TSMC's highly reliable, low cost electrical fuses feature a low programming voltage and field programmability.

	0.13µm	0.11µm	90nm	80nm	65nm	40nm	28nm
Random Access Interface	◎	◎					
High Speed Compilers			◎	◎	◎	◎	◎
Low Power Compilers			◎	◎	◎	◎	◎

High-Speed Interface IP

TSMC's process-optimized high-speed serial interfaces provide top-end optimized bandwidth performance. The portfolio includes IP for consumer connectivity, memory interface, computing interfaces, storage interfaces, and wired and wireless connections, as well as high-speed backplane applications. These IP are silicon-validated across all targeted technology nodes.

IP	Partners
USB2.0 & USB3.0	Synopsys, TSMC
DDR, DDR2, DDR3, Mobile DDR	Analog Bits, ARM, Dolphin Technology, Mosys, Synopsys, TSMC
PCI-e	Analog Bits, ARM, Cadence, Mosys, Snowbush, Synopsys
SATA	Ceva, Mosys, Snowbush, Synopsys
HDMI	Explore, Silicon Image, Silicon Library, Synopsys
10/ 100 Ethernet	Cadence, Transwitch
HSTL, PECL, LVDS	ARM, Dolphin Technology, Synopsys, TSMC

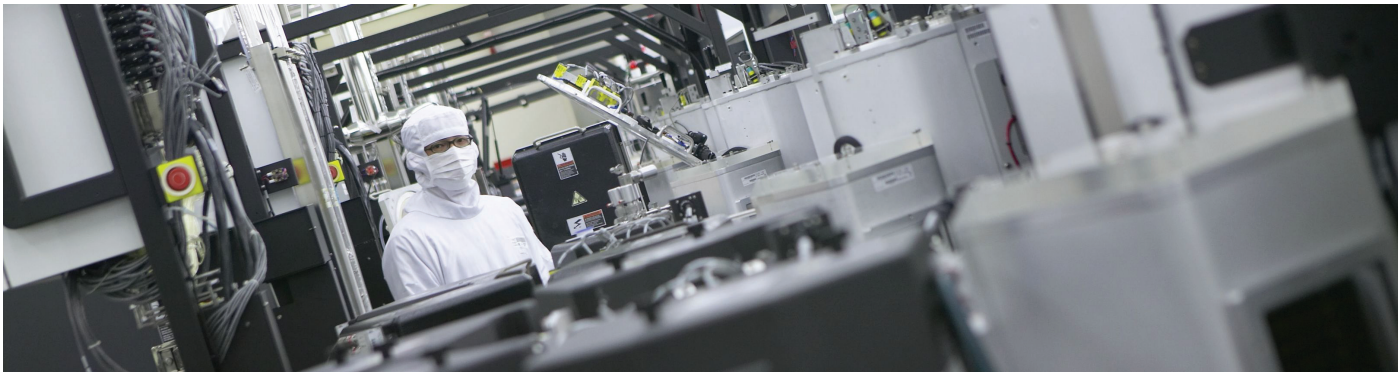
Embedded Flash IP

TSMC offers embedded Flash IP in all of its embedded Flash process technologies. High speed and low power features meet a wide range of applications. Embedded Flash IP blocks with small sector sizes can replace EEPROM functions.

	0.18µm	0.13µm	90nm	65nm
MoSys	1TP	1TQ*	Embedded DRAM*	Embedded DRAM*
TSMC			Embedded DRAM	Embedded DRAM

** Contact TSMC for IP9000 qualification status*

	0.5µm	0.35µm	0.25µm	0.18µm	90nm
Memory Density	4K-512Kb	4K-4Mb	8K-4Mb	4K-8Mb	4K-32Mb
Bus Width	x8, x16	x8, x16	x8, x16, x32	x8, x16, x32	x8, x16, x32
Compiler	NOW	N/A	NOW	N/A	NA
EE Emulator	2K-16	1K-4Kx8	512-4Kx8 512-2Kx16	Upon Request	Upon Request
Automotive	N/A	N/A	NOW	NOW	N/A



Embedded DRAM IP

TSMC's embedded DRAM, a high density memory IP available in the 90nm and 65nm process technologies, meets today's need for high density on-chip memory configurations. Memory density is available in 1Mb granularity. Power saving options, such as sleep mode and deep power down mode, are also available. The IP provides a pipeline and a flow-through SRAM interface with 32-256bit data bus width for design flexibility. A built-in circuit extends data retention, reduces soft error rate (SER), and greatly improves production yield.

	90nm	65nm	40nm
Pipeline Access	◎	◎	◎
Flow-Thru Access	◎	--	--

Quality Management

TSMC rates all libraries and IP whether provided by TSMC or by its third-party partners according to its own stringent quality standards. The TSMC library and IP quality program is the industry's first formally structured evaluation system that gives designers the confidence to use third-party libraries and IP, increases first-time silicon success, and improves yield ramp. The program consists of series of checks at five levels: pre-screen at design-kit delivery, pre-silicon design margin check, silicon-based functionality and timing check, split-lot margin check, and mass-production record check. Status reports are available on the TSMC-Online Design Portal.

Please Click the indicator for detailed information of each validation level.

◎ **Complete**
Pre-Screen: Physical review
Level IV: Split lot verific action

◑ **Did Not Pass**
Level I: Pre-silicon assessment
Level V: Volume production

○ **In-progress**
Level III: Test chip verification
: Data updated after Feb. 28, 2006

Product Name	Version	Description	TSMC comment	DFM comment	Pre-Screen	Level I	Level III	Level IV	Level V
TSMC-CL090G-NGPIO-PL-3VT-2.5V	2005q2v1	Standard I/O, Pad Limited, 1.0V/2.5V/3V-tolerant			◎	◎	◑		
tsmc090g-hivt_sc-x3	2004q2v1	Sage-X3 Standard Cell, high Vt			◎	◎			
tsmc090g-hivt_sc-x3	2004q2v2	Sage-X3 Standard Cell, high Vt			◎	◎	◎		
tsmc090g-hivt_sc-x3	2005q3v2	Sage-X3 Standard Cell, high Vt		◎	◎	◎	◑		
tsmc090g-od-hivt_sc-x3	2006q1v1	Sage-X3 Standard Cell, Standard Vt, high Vt		◎	◎	○			

Advanced Design Methodology

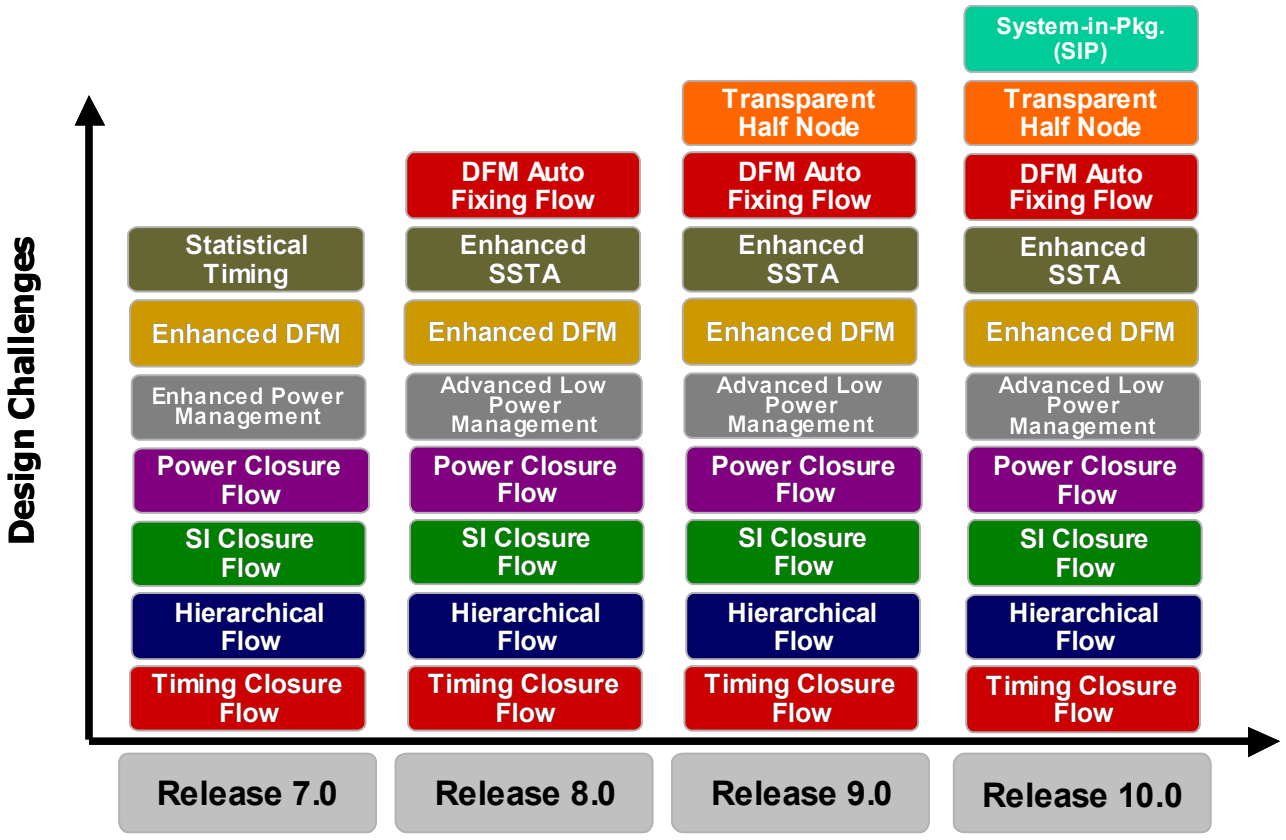
Reference Flow

TSMC introduced the industry's first Reference Flow in 2001. The company has since established Reference Flow as a foundry design service standard and continues to enhance its capabilities. The result is the most comprehensive reference flow portfolio that includes nine consecutive releases.

As the foundry design methodology leader, TSMC addresses today's most critical design challenges with Reference Flow, paving the wave for 28nm technology design support. Reference Flow includes new power management techniques, an improved statistical static timing analysis methodology, transparent half-node support, and an array of DFM enhancements that reduce power consumption, optimize design margins, and maximize yield.

Reference Flow is supported by the same Active Accuracy Assurance (AAA) initiative that defines accuracy standards for all TSMC's design ecosystem partners. Reference Flow focuses on ease-of-use and provides a reference of qualified design tools and flows that give designers a proven path from specification to tape out.

Extensive EDA partner collaboration is the hallmark of TSMC's Reference Flow. Reference Flow offers three complete design implementation tracks – Cadence, Synopsys and Magma – for high-value, low-risk, and easy adoption of TSMC process technology.



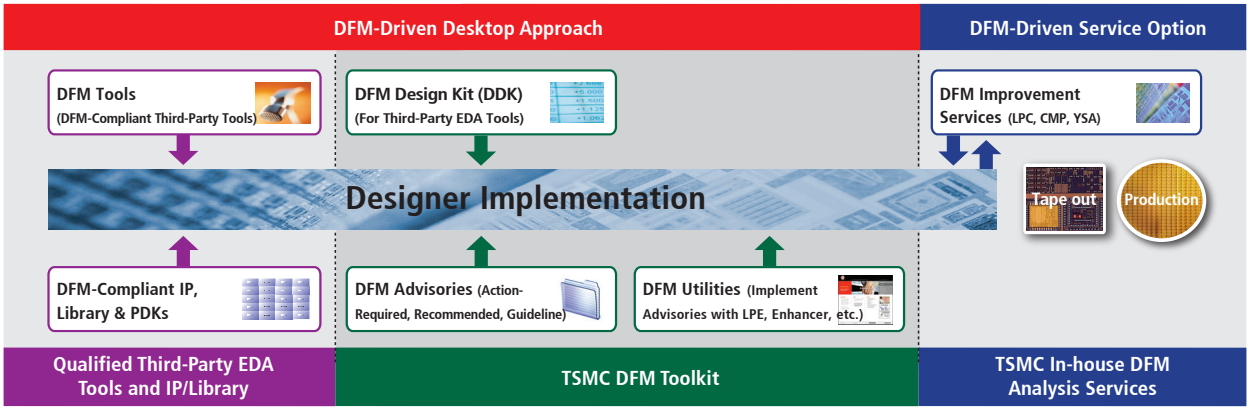
Design for Manufacturing

TSMC created the foundry segment's first Design For Manufacturing (DFM) initiative through a careful, detailed compilation of manufacturing data and collaborative development with key ecosystem partners.

TSMC's DFM initiatives produce more good die per wafer by applying manufacturing-related information to the design implementation stage. TSMC provides DFM Data Kits (DDKs) and tool-specific utilities to enhance yields and accelerate time-to-volume. TSMC also makes available its own internal expertise and resources to address design-specific DFM improvements prior to tape out.

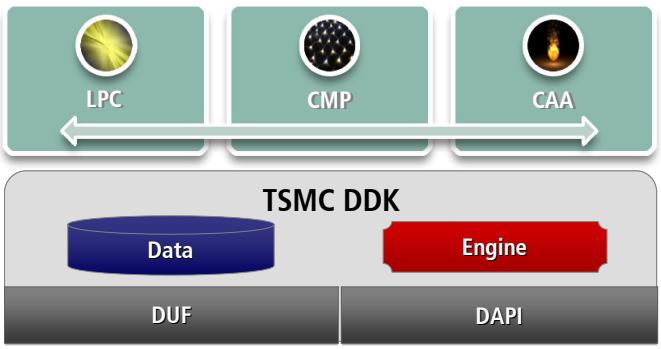
TSMC's design for manufacturing architecture consists of a DFM-Driven Desktop Approach and a DFM-Driven Service Option. The Desktop Approach is accessed through the TSMC DFM Toolkit that is available from TSMC or qualified third-party EDA and IP companies. The DFM Toolkit includes comprehensive data and utilities for design implementation including up-to-date DFM advisories that provide descriptive guides, TSMC-developed DFM utilities, and DDKs.

The DFM-driven Service Option extends TSMC's own expertise to the design community. Services include lithographic process checking (LPC), chemical mechanical polishing effect simulation (CMP), and yield sensitivity analysis (YSA). Designers can implement these services through TSMC-qualified tools or through TSMC's professional services.



TSMC's new Unified Design For Manufacturing (UDFM) architecture targets 28nm and smaller process technology and geometries to improve yields, lower design costs and accelerate time-to-market and time-to-volume.

UDFM was developed in collaboration with EDA vendors and other design infrastructure partners to provides a unified, encapsulated access to TSMC foundry data.



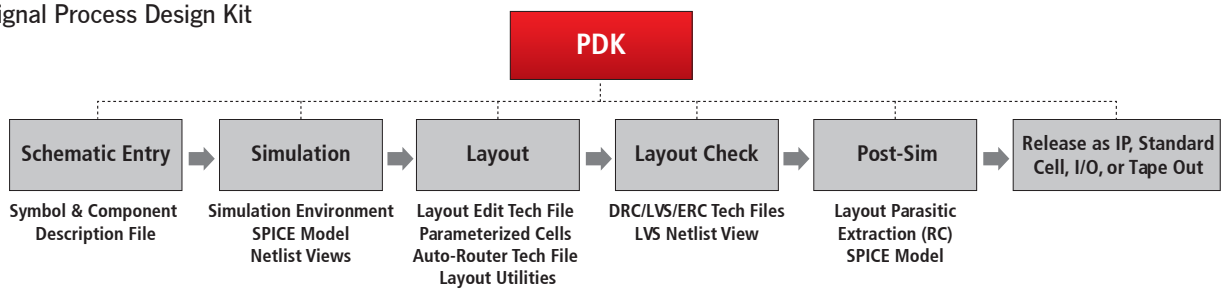
The TSMC UDFM architecture includes a new DFM Design Kit (DDK) that, for the first time encapsulates an embedded DFM software engine with an interoperable API along with process-related DFM data and models. UDFM inserts an exact copy of TSMC's factory tool chain and process models into IC design tool chains, providing access to more TSMC's manufacturing data than ever before.

This "copy exact" method compensates for increasing manufacturing variances in advanced process technologies, radically improves design alignment between simulated hotspots and actual manufacturing hotspots, and delivers a high level of accuracy. The new DFM architecture handles a very large DFM dataset and design complexity, resulting in reduced design cycle time and faster time-to-volume.

Process Design Kits

TSMC's comprehensive and accurate design kits provide custom digital, analog, and mixed-signal/RF designers that much needed head start in today's competitive environment. Design kits consist of symbols for each device that are linked to the device model and layout. The PDKs cover the entire design flow, from schematic entry, simulation, layout, and layout check to post-layout simulation. TSMC's PDKs cover CMOS, Silicon Germanium, high voltage, and CMOS image sensors, encompassing technologies from 0.6µm to 28nm. The entire suite of technology and command files is posted at TSMC-Online. TSMC provides direct and e-mail technical support to increase designer productivity.

Mixed-Signal Process Design Kit



Design Ecosystem Alliances

IP/Library Alliance

The IP/Library Alliance is the industry's largest and most comprehensive catalog of silicon-verified and production-proven IP and process-specific libraries. IP cores are validated in TSMC silicon through our CyberShuttle™ prototyping service, providing the best design experience, easiest design reuse, and fastest integration.

IP Library Partners

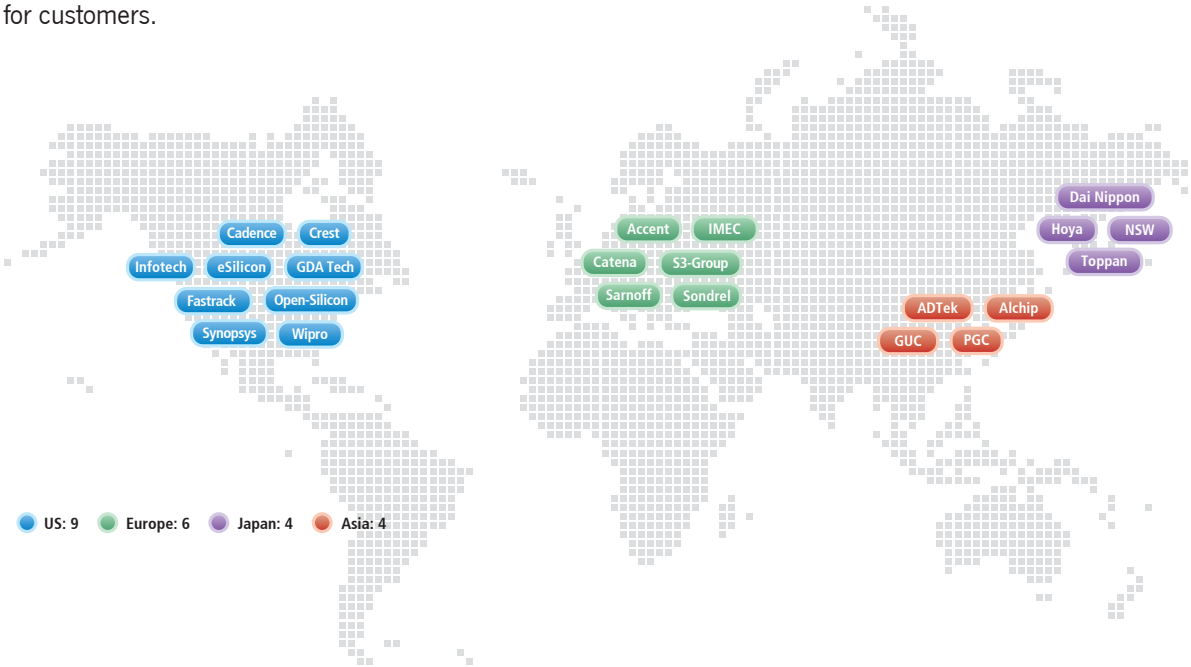
ARM, Kilopass, MIPS Technologies, Renesas, Silicon Image, mixIC, YMC, NANGATE, denali, Rambus, Innovative Semiconductors, Inc., CEVA, IPGoal, THETA microelectronics, SLi, Imagination Technologies, Analog Bits, TransSwitch, TCI True Circuits Inc., AWARE, cadence, 創意電子 Global Unichip Corp., eMemory, Sidense The Future of Logic NVM, Snowbush IP A Division of Gennum, novelics, ARAGIO, Hitachi ULSI Systems Co., Ltd., GigaDevice, Dolphin Technology, MoSys, tensilica, S3 Group, Virage Logic, SYNOPSYS, COSMIC Circuits, DOLPHIN

EDA Alliance

The EDA Alliance, consisting of leading EDA companies, provides a comprehensive set of process technology files and PDKs to simplify the design process. Selected alliance members work closely with TSMC's design technology services team to implement TSMC's design methodology and Reference Flows. Through the EDA Alliance, EDA companies gain access to TSMC's technical insights to validate their tools and methodologies. TSMC supports the industry's most popular design and verification tools, with tech files posted at TSMC-Online. These tech files are kept current and at optimal accuracy through the cooperation of EDA Alliance members.

Design Center Alliance

The Design Center Alliance (DCA) is a global network of experienced, qualified IC design centers that brings design ideas from concept to finished product. TSMC's DCA provides a wide range of IC implementation services. The Alliance's combined service capability and capacity dramatically reduce design, manufacturing, and schedule risks for customers.



Collaborate to Innovate

TSMC provides the robust design ecosystem, technology platforms and manufacturing excellences that promote the highest level of collaboration to drive your next innovations.

Open Innovation Platform™

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