The Design of High-Performance Analog Circuits on Digital CMOS Chips

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Abstract—**Devices available in digital oriented CMOS processes are reviewed, with emphasis on the various modes of operation of a standard transistor and their respective merits, and on additional specifications required to apply devices in analog circuits. Some basic compatible analog circuit techniques and their related tradeoffs are then surveyed by means of typical examples. The noisy environment due to cohabitation on the chip with digital circuits is briefly evoked.**

I. Introduction

THE EVOLUTION of scaled-down digital processes will shift the boundary between digital and analog parts of systems [1]. However, analog circuits will remain irreplaceable components of systems-on-a-chip. Besides A/D conversion, they will always be needed to perform a variety of critical tasks required to interface digital with the external world, such as amplification, prefiltering, demodulation, signal conditioning for line transmission, for storage, and for display, generation of absolute values (voltages, currents, frequencies), and to implement compatible sensors on chip. In addition, analog will retain for a long while its advantage over digital when very high frequency or very low power is required.

Most of the limitations of analog circuits are due to the fact that they operate with electrical variables and not simply with numbers. Therefore, their accuracy is fundamentally limited by unavoidable mismatches between components, and their dynamic range is limited by noise, offset, and distortions.

For economical reasons, the analog part of a system-on-a-chip must be fully compatible with a process basically tailored for digital requirements, and this with a minimum number of additional specifications. Section II will review all active and passive devices available in digital CMOS processes, together with the additional specifications needed to use them for implementing analog circuits. Some basic analog circuit techniques will then be described in Section III by means of typical examples. Finally, the problems related to the noisy environment due to cohabitation on the chip with large digital circuits will be briefly evoked in Section IV.

Manuscript received November 2, 1984; revised December 24, 1984.
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II. Devices Available for Analog Circuits

A. Transistors

A clear understanding of the various ways of biasing a normal MOS transistor, and of their respective merits, is a key factor in the design of optimum analog subcircuits. Fig. 1 illustrates the complete transfer characteristics $I_D(V_G)$ of a n-channel MOS transistor in saturation for various possible modes of operation. For the sake of symmetry, all potentials are defined with respect to that of the local substrate, in this case the p-well.

The general behavior of drain current in saturation I_D in the two basic modes of field effect operation can be described by two separate approximative models [2], [3] which sacrifice accuracy to clarity and simplicity:

Strong inversion ($I_D \gg \beta U_T^2$)

$$I_D = \frac{\beta}{2n}(V_G - V_{T0} - nV_S)^2, \quad \text{for } V_D > V_{D\,sat} = (V_G - V_{T0})/n. \quad (1)$$

Weak inversion ($I_D \ll \beta U_T^2$)

$$I_D = K\beta U_T^2 \exp\left((V_G - V_{T0} - nV_S)/nU_T\right), \quad \text{for } V_D > V_{D\,sat} = 3 \text{ to } 4U_T. \quad (2)$$

These models only include the three most important device parameters required for circuit design

$\beta = \mu C_{ox} W/L$ transfer parameter for strong inversion

V_{T0} gate threshold voltage for $V_S = 0$

n slope factor in weak inversion, which also describes approximately the effect of fixed charges in the channel in strong inversion. Its value depends slightly on V_S [3] and ranges usually from 1.3 to 2.

K is a factor somewhat larger than 1, which connects weak and strong inversion. Its exact value has no importance in circuit design, since transistors in weak inversion must be biased at fixed drain current I_D to avoid the very high sensitivity to $U_T = kT/q$ and V_{T0} for fixed gate voltage V_G.

In CMOS logic circuits, transistors usually operate with $V_S = 0$ as shown in heavy lines in Fig. 1. Their role is to

Reprinted from *IEEE J. Solid-State Circuits*, vol. SC-20, no. 3, pp. 657–665, June 1985.

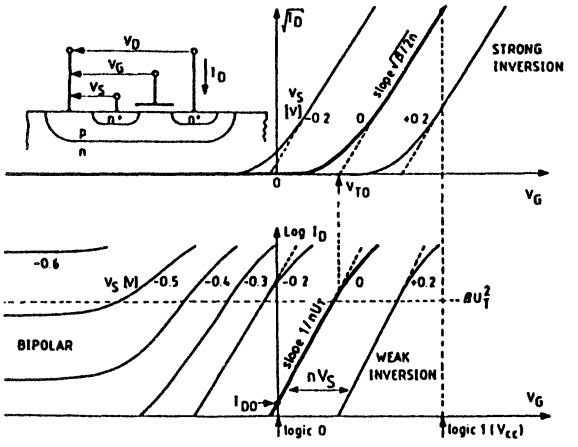

Fig. 1. General transfer characteristics $I_D(V_G)$ of a MOS transistor in saturation. Different modes of operation can be identified, namely strong inversion, weak inversion, and bipolar.

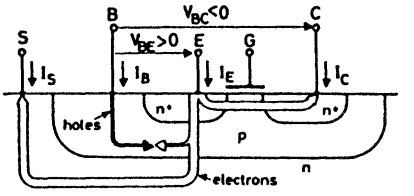

Fig. 2. Flows of carriers in bipolar operation.

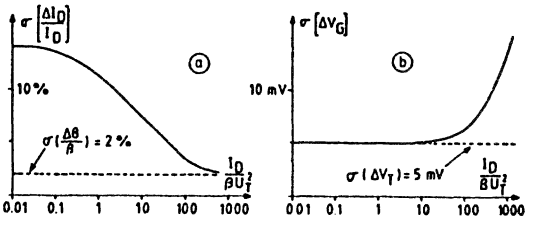

Fig. 3. Matching of a pair of MOS transistors as a function of drain current, for (a) same gate voltage and (b) same drain current. Uncorrelated components with mean standard deviations of 2 percent for $\Delta\beta/\beta$ and 5 mV for ΔV_T are assumed in this example.

provide maximum drain current in the "on" state for $V_G = V_{cc}$, and minimum residual current I_{D0} in the "off" state for $V_G = 0$. The only requirements for digital circuits are thus a maximum possible value of transfer parameter β, and a value of threshold voltage V_{T0} as low as possible while ensuring acceptable value of residual current for $V_G = 0$

$$I_{D0} = K\beta U_T^2 \exp(-V_{T0}/nU_T). \tag{3}$$

This is only possible if slope factor n of weak inversion is not too large. These requirements are also favorable to analog circuits, since they allow a maximum value of transconductance g_m which can be easily derived from (1) and (2) as

$$g_m = ((2\beta I_D)/n)^{1/2} = 2I_D/(V_G - V_{T0} - nV_S) \quad \text{(strong inversion)}, \tag{4}$$

$$g_m = I_D/nU_T \quad \text{(weak inversion)}. \tag{5}$$

However, specifications on the maximum range of variation of β, V_{T0}, and n are usually necessary.

Transconductance g_m is proportional to drain current I_D in weak inversion, but only to the square root of I_D in strong inversion. If source voltage V_S is not zero, the gate voltage for constant drain current is shifted by nV_S for both modes of operation. Thus transconductance g_{ms} from source to drain is given by

$$g_{ms} = ng_m. \tag{6}$$

Fig. 1 also shows that when gate voltage V_G is sufficiently negative, it has not more effect on drain current, which means that gate transconductance g_m decreases to zero. However, I_D can still be controlled by negative values of source voltage V_S which corresponds to a forward-biased source junction. The device then operates as a lateral bipolar, with the flow of carriers pushed away from the surface by the negative gate potential [4]. The various flows of carriers in this mode of operation are shown in Fig. 2. Source, drain, and p-well have been renamed emitter E, collector C, and base B. Since a large fraction of emitter current I_E flows to substrate, the maximum alpha-gain of this lateral bipolar is only 0.2 to 0.6, depending on the process. However, owing to the low rate of recombination in the well, the β-gain can reach quite acceptable values ranging from 20 to 500. This high value of current gain is only obtained for the transistor implemented in the well, in this case a n-p-n. The n-p-n to substrate can be used without lateral collector, but only in common collector configurations.

For implementing analog circuits, it is necessary to specify the matching properties of similar adjacent transistors. Matching must be characterized by two independent statistical values: threshold mismatch ΔV_T, which may have in practice a mean standard deviation ranging from 1 to 20 mV, and $\Delta\beta/\beta$ mismatch which is usually in the range of 0.5–5 percent. Fig. 3 shows that when two transistors have the same gate voltage, as in a current mirror, the mismatch of their drain currents

$$\Delta I_D/I_D = \Delta\beta/\beta - (g_m/I_D)\Delta V_T \tag{7}$$

is maximum in weak inversion, for which g_m/I_D is maximum, and only comes down to $\Delta\beta/\beta$ when the transistors operate deeply in strong inversion. On the contrary, when they have the same drain current, as in a differential pair, the mismatch of their gate voltages

$$\Delta V_G = \Delta V_T - (I_D/g_m)\cdot\Delta\beta/\beta \tag{8}$$

is just ΔV_T in weak inversion, and increases in strong inversion where g_m/I_D is reduced.

Noise is a very important limitation of most analog circuits. As shown in Fig. 4, the noise of a transistor must also be characterized by at least two independent sources: White channel noise is independent of the process and corresponds to an equivalent input noise resistance R_N approximately equal to the inverse of transconductance g_m [5]. Gate interface $1/f$ noise dominates at low frequencies

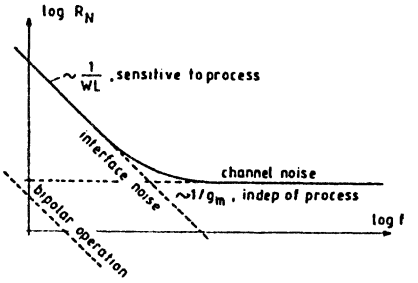

Fig. 4. Contributions to equivalent input noise resistance R_N of a MOS transistor.

TABLE I
SPECIFICATIONS ON TRANSISTORS FOR ANALOG AND DIGITAL APPLICATIONS.
(Analog Requires Specifications on Additional Parameters, and on Maximum and Minimum Values of Some Parameters.)

Parameter	Digital	Analog
β	min.	min.-max.
V_T	max.	min.-max.
n	max.	min.-max.
I_{D0}	max.	max.
β -bipolar	—	min.
mismatch	—	max.
1/f noise	—	(max.)
output resist.	—	min.

and is approximately independent of drain current. It is inversely proportional to gate area, and very sensitive to process quality. It should therefore be eliminated by circuit techniques such as chopping or autozeroing [6]–[8].

Both flicker noise and threshold mismatch are drastically reduced when the transistor operates in the lateral bipolar mode [4]. This is because the device is then shielded from all surface effects.

The respective qualitative specifications on transistors for digital and analog applications are summarized in Table I. An additional requirement for analog is a high value of output resistance which is approximately proportional to channel length. Designs should be made independent of the exact value of this parameter.

B. Passive Components

In digital CMOS circuits, passive components, namely capacitors and resistors, are only present as parasitics and should therefore by minimized. On the contrary, functional passive components of reasonable values and acceptable quality are required in most analog subcircuits.

Excellent precision capacitors can be implemented in a compatible way by using the silicon dioxide dielectric, provided both electrodes have a sufficiently low resistivity. Thin oxide gate capacitors are available in metal gate technologies, but they cannot be implemented in Si-gate processes without additional steps. For processes with a single polysilicon layer, the only reasonable choice is the capacitor between aluminum and polysilicon layers [9], which usually achieves rather low specific values. Many modern technologies provide two layers of polysilicon that can be used as electrodes for the capacitors [10].

Good resistors of less than 100 Ω/sq. can be obtained in the polysilicon layer. Higher values of few kiloohms per square are possible by using the well diffusion, but these resistors are slightly voltage dependent, and they are always associated with a large parasitic capacitance. Lightly doped polysilicon resistors such as those used to implement quasi-static RAM's [11] achieve very high values but they have a very poor accuracy.

Most of the modern design techniques for analog circuits are based on ratios of capacitances or resistances, and therefore only require specifications on matching and linearity of passive devices. If absolute values are needed as well, data on spread, temperature behavior, and aging must be available, and must be ensured by periodic statistical measurements.

No floating diode is usually available, except the base–emitter junction of the bipolar transistor to substrate. Some special micropower processes offer a lateral diode in the polysilicon layer [12].

III. BASIC ANALOG CIRCUIT TECHNIQUES

A. Optimum Matching

Most analog circuit techniques are based on the matching properties of similar components. For a given process, matching of critical devices may be improved by enforcing the set of rules that are summarized in Table II. These rules are not specific to CMOS and are applicable to all kinds of IC technologies. The relevancy and the quantitative importance of each of these rules depend on the particular process and on the particular device under consideration.

1) Devices to be matched should have the same structure. For instance, a junction capacitor cannot be matched with an oxide capacitor. This also means that the error due to parasitic junction capacitors cannot be compensated by adjusting the value of functional oxide capacitors.

2) They should have same temperature, which is no problem if power dissipated on chip is very low. Otherwise, devices to be matched should be located on the same isotherm, which can be obtained by a symmetrical implementation with respect to the dissipative devices.

3) They should have same shape and same size. For example, matched capacitors should have same aspect ratios, and matched transistors or resistors should have same width and same length, and not simply same aspect ratios.

4) Minimum distance between matched devices is necessary to take advantage of spatial correlation of fluctuating physical parameters.

5) Common-centroid geometries should be used to cancel constant gradients of parameters. Good practical examples

TABLE II
RULES FOR OPTIMUM MATCHING

1. Same structure
2. Same temperature
3. Same shape, same size
4. Minimum distance
5. Common-centroid geometries
6. Same orientation
7. Same surroundings
8. Non minimum size

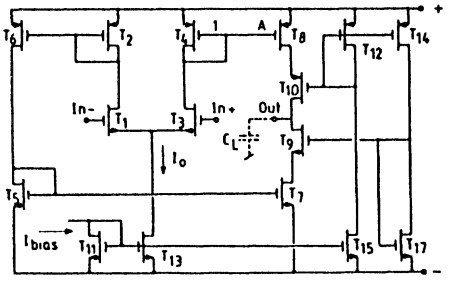

Fig. 5. Single-stage cascode operational transconductance amplifier (OTA) [13].

are the quad configuration used to implement a pair of transistors, and common-centroid sets of capacitors.

6) The same orientation on chip is necessary to eliminate dissymmetries due to unisotropic steps in the process, or to the unisotropy of the silicon substrate itself. In particular, the source to drain flows of current in matched transistors should be strictly parallel.

7) Devices to be matched should have the same surroundings in the layout. This to avoid for instance the end effect in a series of current sources implemented as a line of transistors, or the street effect in a matrix of capacitors.

8) Using nonminimum size is an obvious way of reducing the effect of edge fluctuations, and to improve spatial averaging of fluctuating parameters.

Matching can be extended to the realization of non-unity n/m ratios by separately grouping m and n matched devices. A slight alteration of one or many devices is necessary when intermediate ratios are required.

B. Amplifiers

The basic configurations and tradeoffs related to the realization of amplifiers can be discussed with the example of a single-stage cascode OTA represented in Fig. 5 [13].

Differential pair $T_1 - T_3$ converts the differential input voltage into a difference of currents which is integrated in load capacitance C_L. These transistors can have minimum channel length since they are loaded by the high input conductance of current mirrors. Remaining design parameters are then channel width W and value of tail current I_0. Optimization of this input pair therefore amounts to choosing the best possible point in the (W, I_0) plane, with respect to conflicting requirements. This plane is represented in Fig. 6, with the limit between weak and strong inversion which corresponds to a given value of W/I_0.

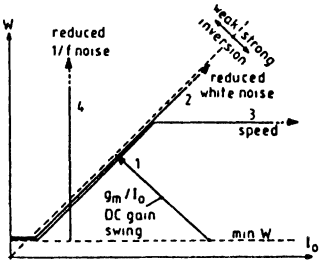

Fig. 6. Optimization of width W and tail current I_0 of input pair $T_1 - T_3$. Arrowed paths 1 to 4 indicate displacements in plane (W, I_0) for maximum improvement of various features of the amplifier.

Displacements in the plane for maximum improvement of various important features of the whole amplifier are represented in a qualitative way.

Transconductance for a given current, dc gain, and maximum possible swing are all improved by increasing W/I_0 to approach weak inversion, where they reach their maximum values (path 1). This also reduces input offset voltage.

The white noise spectral density is inversely proportional to transconductance g_m, which increases linearly with current I_0 up to the upper limit of weak inversion. To keep the advantages of weak inversion, a further increase of g_m requires a parallel increase of width W and current I_0 (path 2), which is only limited by size.

Speed (path 3) is proportional to g_m as long as parasitic capacitances of the transistors (proportional to W) are constant or negligible. A further increase in speed requires a progressive incursion into strong inversion, which results in progressive degradations of dc gain and of maximum possible swing. Speed in strong inversion only increases with the square root of current.

Low frequency $1/f$ noise is reduced by increasing channel width (path 4) and by choosing the better type of transistor, which is usually a p-channel.

If input current can be tolerated, very low $1/f$ noise and very high speed can be achieved by using transistors operated as lateral bipolars [4], [14].

The maximum differential current available from the pair is equal to tail current I_0, which puts a fundamental limit to slew rate. This problem can be circumvented by momentarily increasing current I_0 by a fixed amount each time an input step is anticipated, which yields a dynamic amplifier [15]. It can also be increased by an amount proportional to the difference of drain currents to realize an adaptive bias [16], [17], which provides operation in class AB.

Complementary pairs $T_1 - T_2$ and $T_3 - T_4$ can be viewed as common emitter amplifiers, each of which amplifies half of the total differential input voltage. Gain $g_{m1,3}/g_{m2,4}$ must be high enough, of the order of 3 to 10, to have noise and offset voltage limited to the only contribution of the differential input pair. This requires operation of transistors T_2 and T_4 deep enough into strong inversion. Too much gain reduces the stability phase margin.

As was illustrated by Fig. 3, the mismatch of current mirrors is maximum in weak inversion. It can be shown

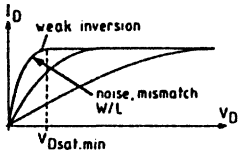

Fig. 7. Optimization of W/L of current mirrors.

that this is true as well for both white and $1/f$ noise [18]. However, according to relations (1) and (2), weak inversion provides the minimum possible value of drain saturation voltage of the order of 100 mV. Therefore, the optimization of W/L of current mirrors $T_{11}-T_{13}-T_{15}, T_2-T_6, T_4-T_8, T_5-T_7$ amounts to an acceptable compromise between small mismatch and low noise (V_G-V_{T0} large), and small saturation voltage (V_G-V_{T0} small) to permit large-signal swing (Fig. 7).

The overall transconductance of the amplifier can be multiplied by ratio A of mirror T_4-T_8, at the expense of a reduction in phase margin. Some of the mirrors can be avoided by using the folded cascode scheme [20].

Cascode transistors T_9 and T_{10} decrease the output conductance by a factor equal to g_{ms}/g_o. This is obtained without any noise penalty, and with only a very small reduction of phase margin. The resulting dc gain is thus higher than that of a two-stage noncascode amplifier which requires internal compensation. Gain may be further boosted by using double or triple cascode [19], until it becomes limited by the direct conductance to ground due to impact ionization in the drain depletion layers.

The reduction of maximum output swing due to the cascode transistors can be minimized by careful design of the bias circuitry $T_{12}-T_{14}-T_{15}-T_{17}$ [13], [20]. Drain voltages of transistors T_7 and T_8 can be made equal to their limit value $V_{D\,sat}$ for saturation, independently of bias current. Maximum output swing is then only reduced by $4V_{D\,sat}$ with respect to total supply voltage, which only amounts to about 400 mV in weak inversion.

The circuit can be modified to provide differential output [20]. This doubles the maximum output swing, but requires a common mode feedback scheme.

All amplifiers based on a differential input pair suffer noise and speed penalties with respect to a simple CMOS inverter used as an amplifier with an adequate biasing scheme [21]. This kind of amplifier is furthermore free from any slew rate limitation. It represents a very attractive solution for very low power [7] or very high speed [22] applications, in spite of its poor intrinsic PSRR.

C. Switch and Sample-and-Hold

The realization of the analog switch, which is a very important component of CMOS analog circuits, is illustrated in Fig. 8. A n-channel transistor is switched on by connecting its gate to the positive power line V_B. However, its on-conductance g_n comes to zero if potential V_F at which the device floats is too high. The same is true if V_F is too low for on-conductance g_p of the p-channel transistor

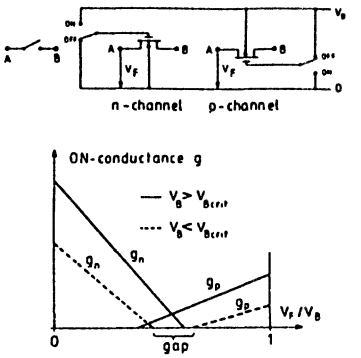

Fig. 8. Realization of an analog switch. On-conductances g_n and g_p of n-channel and p-channel transistors depend on floatation voltage V_F.

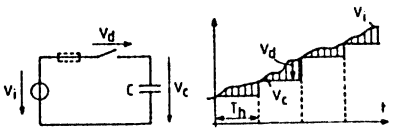

Fig. 9. Elementary sample-and-hold.

with gate connected to zero. If total supply voltage V_B is larger than a critical value $V_{B\,crit}$, the conductance of the switch can be ensured independently of V_F by connecting both types of transistors in parallel. Below this critical value, a gap of conduction appears at intermediate levels of V_F. Because of substrate effects, this critical supply voltage may widely exceed the sum $V_{T0p}+V_{T0n}$ of p and n thresholds for zero source voltages. For example, $V_{T0p}=0.6$ V and $V_{T0n}=0.7$ V may correspond to $V_{B\,crit}=2.3$ V [18], [23]. This very severe limitation to low-voltage operation of analog circuits may be circumvented by on-chip clock voltage multiplication [8], [24].

Leakage in the off state is due to residual channel current and to reverse currents of junctions. Care must be taken not to bootstrap the switch potential beyond that of the power supply lines, which would forward bias these junctions [25].

The combination of a switch and a capacitor provides a basic sample-and-hold shown in Fig. 9. Voltage V_C across capacitor C keeps a constant value equal to that of input voltage V_i at the last sampling instant. The value the of noise voltage at the sampling instant is also frozen in capacitor C; therefore, the total noise power is concentrated below the clock frequency. Voltage V_d across the switch is readjusted to zero each time the switch is closed, which corresponds to the transfer function for the fundamental signal (component of output signal V_d at the frequency of input signal V_i) shown in Fig. 10 [26]. At low frequency, this autozeroing by means of a sample-and-hold amounts to a differentiation, with a time constant equal to half the value of hold duration T_h. It may be used to cancel offset and to reduce low-frequency noise components generated in a circuit [6], [27].

Another source of sampling error is caused by the charge which is released from the channel into holding capacitor C when the transistor of the switch is blocked [28]. This problem has been analyzed in the general case shown in

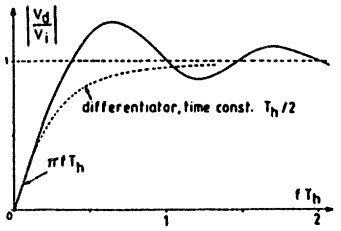

Fig. 10. Differentiating property of autozeroing obtained by sample-and-hold.

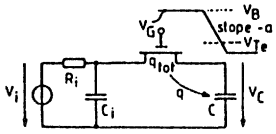

Fig. 11. Equivalent circuit of a practical sample-and-hold. Finite fall time of gate voltage V_G allows redistribution of charge through the transistor.

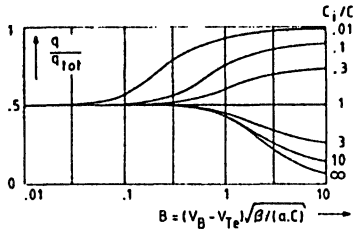

Fig. 12. Calculated fraction q of total charge q_{tot} left in holding capacitor C after switch-off [23].

Fig. 11 where the source of the signal is assumed to have an internal capacitance C_i [23], [26]. Finite fall time of V_G (slope $-a$) from initial value V_B to effective threshold voltage V_{Te} allows a redistribution through the transistor of total charge $q_{tot} = C_{gate}(V_B - V_{Te})$ between C and C_i. The result obtained by numerical integration of a normalized nonlinear equation describing this process, for time constant R_iC_i much larger than the switching time, is represented in Fig. 12. This figure shows the fraction q of total channel charge q_{tot} which goes into holding capacitor C for various values of ratio C_i/C. This fraction is a function of an intermediate parameter B which combines clock amplitude, clock slope, β of transistor, and value of holding capacitor C. These curves suggest various strategies for minimizing parasitic charge q.

A first possibility is to choose C_i very large and B much larger than 1. All charges released into C flow back into C_i during the decay of gate voltage, and q tends to zero (some easily calculable additional charge is due to the coupling through overlap capacitors after switching off). The drawback is the long period of time needed for switching off.

A second solution is to equilibrate the values of both capacitors [29]. By symmetry, half of the channel charge flows in each capacitor, and can be compensated by half-sized dummy switches that are switched on when the main switch is blocked [28].

The need for equal values of capacitors may be eliminated by choosing a value of B much smaller than 1 which also ensures equipartition of the total charge. Charge q is then compensated by a single dummy switch.

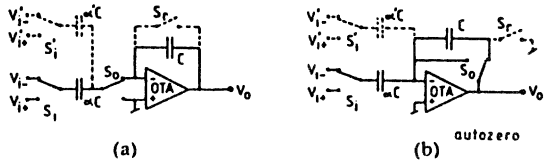

Fig. 13. Stray insensitive SC integrators.

When complementary transistors are used to implement the switch, they partially compensate each other, although matching is very poor. The effect of charge injection can be drastically reduced by appropriate circuit techniques such as differential implementation [25], and active compensation by a low sensitivity auxiliary input [26], [30].

D. Switched Capacitor Integrators

Switched capacitor integrators are the building blocks of all kinds of circuits, in particular SC filters. Two different implementations that are insensitive to parasitic capacitances to ground are shown in Fig. 13. Both provide a differential input and a time constant $1/\alpha f_c$, which only depends on clock frequency f_c and ratio of capacitors α. Version b includes autozeroing, which reduces low-frequency noise and compensates offset. It can therefore be realized with a nondifferential amplifier such as a CMOS inverter [7].

Output resetting can be obtained by additional switch S_r, and many differential signals can be separately weighted and summed by repeating the input circuitry, as shown in dotted lines. These integrators may be damped at will by connecting one of these additional inputs to output.

They can be transformed into amplifiers with controlled gain, either by resetting the output at every clock cycle, or by deleting integrating capacitor C in a damped configuration.

E. Comparators

Comparators must usually achieve a very low value of input offset voltage. An excellent solution is obtained by removing integrating capacitor C in the basic integrator of Fig. 13b [31]. Any difference $V_{i+} - V_{i-}$ will cause an output current to charge (or discharge) the parasitic output capacitance. The comparator thus behaves as an integrator of input error voltage, and sensitivity is proportional to the time alotted for comparison. It is ultimately limited by the finite dc gain of the amplifier. The speed-sensitivity ratio may be increased by achieving nth order integration along a cascade of n stages [26], as shown in Fig. 14.

The effects of charge injection and switching noise may be virtually cancelled by sequentially opening switches S_1 to S_n before toggling switch S_0: When S_1 is opened first, charge injection and sampled noise cause an error voltage across C_1. Since switch S_2 is still closed, a compensation voltage appears across C_2 after equilibration. The same is true when S_2 to S_{n-1} are then opened sequentially. The

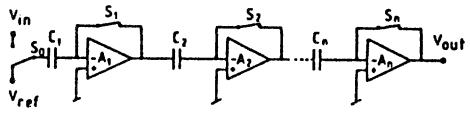

Fig. 14. Multistage comparator.

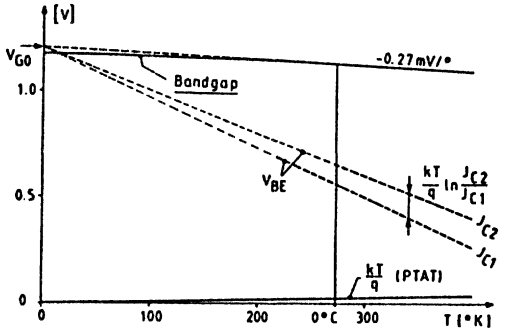

Fig. 15. "Built-in" voltages available in silicon.

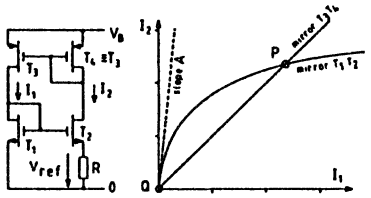

Fig. 16. Extraction of $U_T = kT/q$ with MOS transistors $T_1 - T_2$ operated in weak inversion.

only residual error at the input is thus that due to switch S_n divided by the gain of the $n-1$ first stages [32], [33]. Accuracy is further improved by using a fully differential implementation for which values of offset as low as 5 μV have been reported [34].

F. Voltage and Current References

The realization of absolute references must be based on intrinsic physical values, in order to reduce their sensitivity to process variations.

The various "built-in" voltages provided by silicon are represented in Fig. 15. They can be extracted by adequate circuits to implement voltage references.

Thermal voltage $U_T = kT/q$, proportional to absolute temperature (PTAT), can be extracted by two MOS transistors operated in weak inversion with different current densities, as shown in Fig. 16 [3], [35]. If $T_3 = T_4$, application of weak inversion model (2) to transistors T_1 and $T_2 = AT_1$ yields

$$V_{ref} = U_T \ln(A) \tag{9}$$

which in turn imposes current I_2 in the circuit.

Bandgap voltage V_{gap} decreases approximately linearly with temperature from extrapolated value V_{G0}, with a slight curvature. A possible technique for direct extraction of V_{gap} is shown in Fig. 17 [36]. Transistor T_1 is n-channel with a normal n^+-doped silicon gate. Transistor T_2 is also

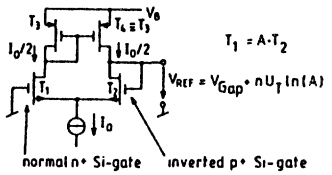

Fig. 17. Extraction of bandgap voltage V_{gap} by MOS transistors [36].

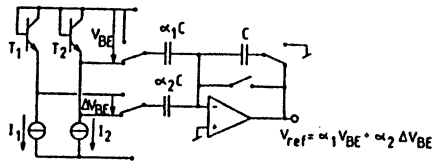

Fig. 18. Principle of SC-weighted bandgap reference.

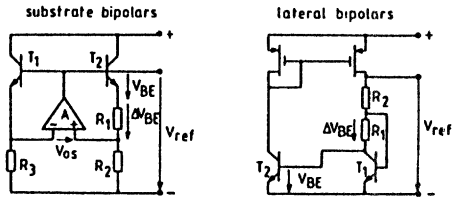

Fig. 19. Principle of R-weighted bandgap reference.

n-channel but with a p^+-doped gate, as is possible in some technologies. Their threshold voltages therefore differ by approximately V_{gap} which appears at the output of this simple amplifier connected in unity gain configuration. After compensation by a small PTAT voltage obtained by operating T_1 and T_2 in weak inversion at different current densities, a temperature coefficient lower than 30 ppm °C can be obtained. All references based on MOS operation have their accuracy degraded by large uncontrolled offset components due to surface effects.

Base–emitter voltage V_{BE} of bipolar transistors is not really a physical parameter, but it only depends very slightly on the process. The difference ΔV_{BE} of two bipolars operated at different current densities is strictly proportional to kT/q. After multiplication by an adequate factor, it can be added to V_{BE} to obtain a voltage of value V_{G0} independent of temperature. This principle of bandgap reference is well known in bipolar technology, and can be applied to the bipolars available in CMOS technology.

Weighting and summing V_{BE} and ΔV_{BE} can be achieved by the SC circuit shown in Fig. 18, which is derived from the integrator of Fig. 13(b) [23], [37], [38]. Transistors T_1 and T_2 are bipolars to substrate. Accuracy is mainly limited by charge injection from the feedback switch.

Another solution consists in using a resistive divider, as depicted in Fig. 19. Version *a* uses substrate bipolars and a CMOS amplifier [39]. The offset of this amplifier, which is multiplied by R_2/R_1 of the order of 10, causes independent errors of the value of V_{ref} and of its temperature coefficient. Adjustment at two different temperatures would thus be required to achieve an accuracy of a few millivolts. Version *b* uses compatible lateral bipolars and avoids any MOS amplifier [4]. The error due to the p-channel mirror is

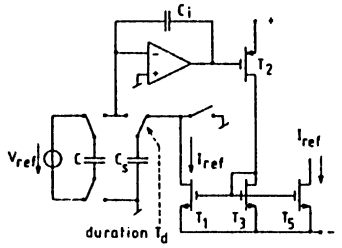

Fig. 20. SC voltage-to-current converter [40].

lowered by operating deeply in strong inversion. The offset of bipolars is small and only causes an error PTAT, which can be corrected at a single temperature.

Semiconductor physics do not provide any "built-in" current. Current references must thus be derived from voltage references by applying Ohm's law in voltage to current converters. Poor absolute precision and temperature coefficient of available resistors result in errors of many tens of percent. A good solution based on a SC scheme that takes advantage of the better accuracy of available capacitors is shown in Fig. 20 [40]. It is a closed loop system which forces equilibrium, for every clock cycle, between charge CV_{ref} poured into storage capacitor C_s and charge $I_{ref}T_d$ withdrawn from the same capacitor. Thus

$$I_{ref} = CV_{ref}/T_d. \tag{10}$$

Generation of an independent frequency on chip is not possible with a precision better than a few tens of percent. It is normally not required since an accurate clock frequency is usually provided by the system, from which synchronous signals of any frequency can be derived in a digital way. Totally asynchronous signals of accurate frequency can be produced by quasi-sinusoidal SC oscillators [41]–[43].

IV. Analog Circuits in a Digital Environment

If no precaution is taken, the dynamic range of analog circuits will be limited by the noise generated by digital circuits operating on the same chip. This problem is specially accute for sampled circuits which fold down high-frequency noise components by undersampling.

Coupling may occur through power lines, current in the common substrate, capacitive links, and possibly by minority carriers that are released when digital transistors are being blocked.

Various provisions can be suggested to improve the situation: Utilization of separate power lines, including pads, bondings, and possibly pins. Implementation of power supply filters or regulators. High value of PSRR, also at high frequencies for sampled circuits; care must be taken not to destroy the PSRR of amplifiers by the additional circuitry. Systematic implementation of fully differential structures. Avoidance of large current spikes in digital circuits, and of any digital transition during critical analog tasks. Provision of maximum distance on chip to digital lines, and of separate clean clocks for analog circuits. Critical nodes should be shielded from substrate and from digital lines by adequate layers, and analog circuits can be separated by special wells that collect parasitic minority carriers. Processes that provide an epitaxial layer on a highly doped substrate, to improve immunity to latch-up, allow to drain all parasitic currents to substrate.

V. Conclusion

Thanks to the versatility of the CMOS technology, all kinds of analog circuits can be combined on the same chip with digital circuits, without any process modification. However, additional parameters need to be specified and guaranteed, the number of which depends on the type of function and on design cleverness.

A standard MOS transistor can be operated in various modes which have their respective merits. Weak inversion provides maximum values of gain and signal swing, and minimum offset and noise voltages. Strong inversion is required to achieve high speed, and provides minimum relative values of offset and noise currents. The lateral bipolar mode exhibits excellent matching properties and very low $1/f$ noise, and can be used to implement a variety of schemes previously developed for normal bipolars transistors.

Mismatch of active and passive devices represents a major limitation to the accuracy of analog circuits. It can be minimized by respecting a set of basic rules. Designs must be based on sound concepts that take maximum advantage of all available components.

Single-stage cascoded OTA's should be preferred to multistage amplifiers. Their optimization amounts to choosing the best possible compromise with respect to various conflicting requirements. The excellent performance of the MOS transistor as a switch and the availability of high-quality capacitors are key elements in the implementation of a variety of analog functions. The elementary sample-and-hold that is made possible by the absence of any dc gate control current can be used to reduce low-frequency noise and to compensate offset. Its major limitation is due to charge injection from the switch, which can be evaluated and partially compensated by an adequate strategy.

Accurate absolute references are very critical circuits which must be based on intrinsic physical values to achieve low sensitivity to process. This is possible for voltage references, from which current references can be derived by applying Ohm's law.

Precautions must be taken to avoid degradation of analog performances by the noise generated by the digital part of the chip.

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