Analog IC Design Project

Folded Cascode Operational Amplifier

Submitted By
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12/06/04

Operational Amplifier Design Using Folded Cascode Structure

Design Specifications:-

1) Differential Voltage Gain (Avd) >= 80dB
2) Output Voltage Swing Range (OVSR) >= 3V
3) Slew Rate (SR) >=10V/us for 10 pF Capacitor
4) Differential Input Resistance (Rid) >= 1Meg
5) Input Common Mode Range (ICMR) >= 3V
6) Common Mode Rejection Ratio (CMRR) >= 60dB
7) Unity Gain-Bandwidth: (GB) >= 100 MHz with a 10 pF load capacitance.
8) Phase Margin: f(GB) >= 60° with a 10 pF load capac itance.
9) Power dissipation: Pdiss <= 1mW.

The amplifier is to be powered from a 3.3 volts power supply and with a current reference of 10µA. The capacitors can be designed using poly1-poly2. The current sources/sinks required for biasing can be derived from the given current reference using current mirrors. Please use TSMC CMOS 0.35-µm technology.

Description Of Design Stages

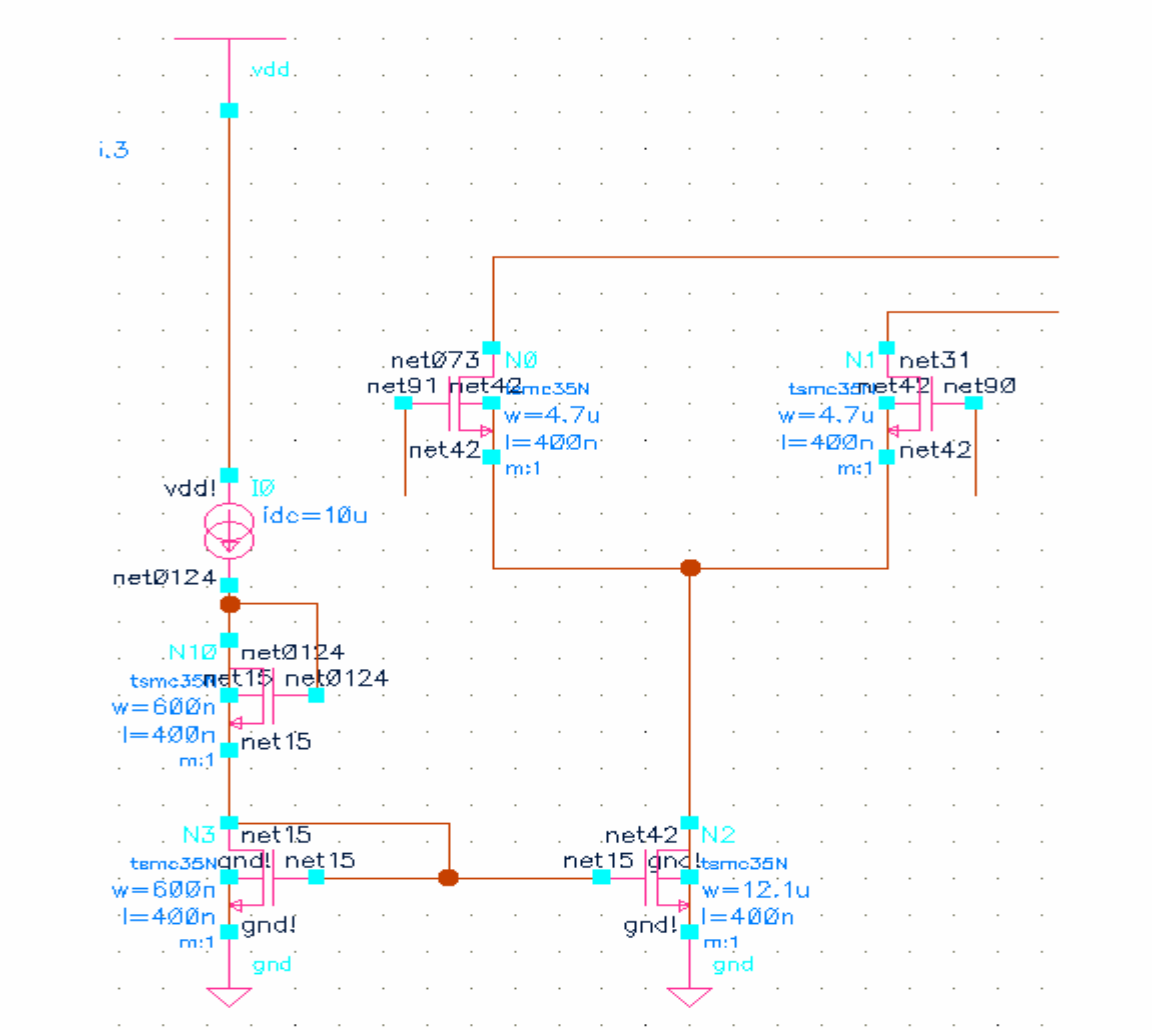
The folded cascode operational amplifier implemented has three stages.

1) Differential Input Stage
2) Folded Cascode Load Stage
3) Output Stage

There are variety of structures available for all of the above three mentioned stages, each have some advantages and some disadvantages of its own. While designing the operational Amplifier meticulous choice of these configurations is essential for proper functioning of amplifiers. Following is the list of configurations considered for this design:-

1) Differential Input Stage

This stage is responsible for accepting differential inputs and amplifies each of them there by passing them to cascode load stage. Following is stage used in this design

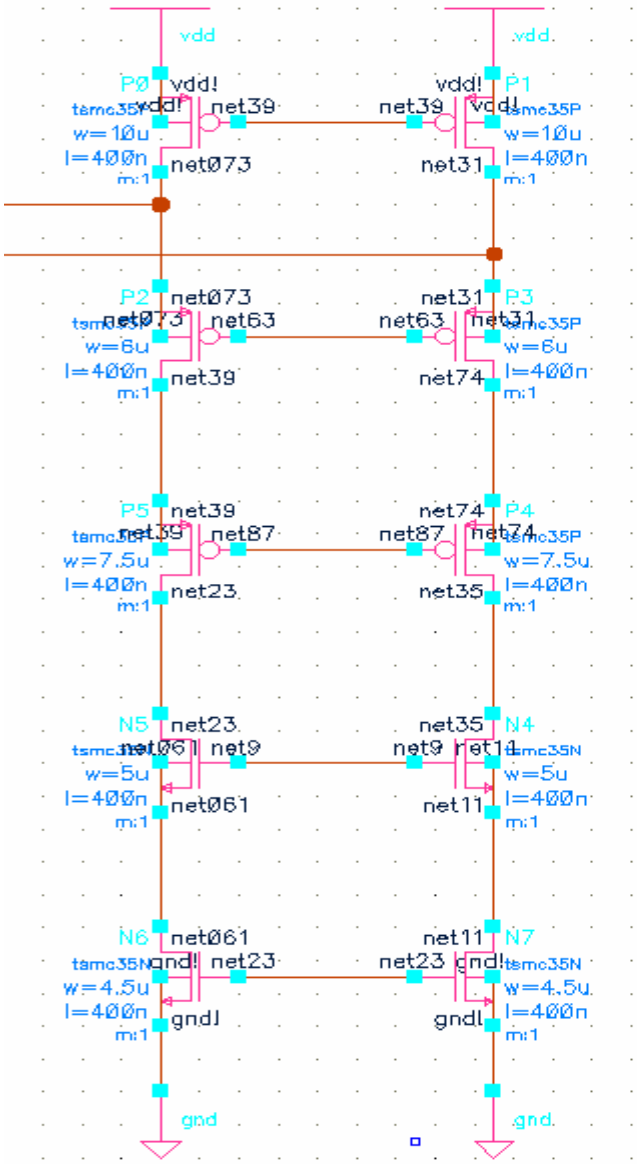


It is a NMOS differential amplifier whose tail current is supplied through a current mirror. The other alternative available is a PMOS differential pair, but since NMOS have higher mobility than PMOS so they provide better current switching speed and there by high slew rates and better gain. How ever both of them can be incorporated in the same stage to enhance input common mode range i.e. input can swing to negative values as well. This design is already meeting ICMR requirements so only NMOS differential pair is used in it.

2) Folded Cascode Load Stage:-

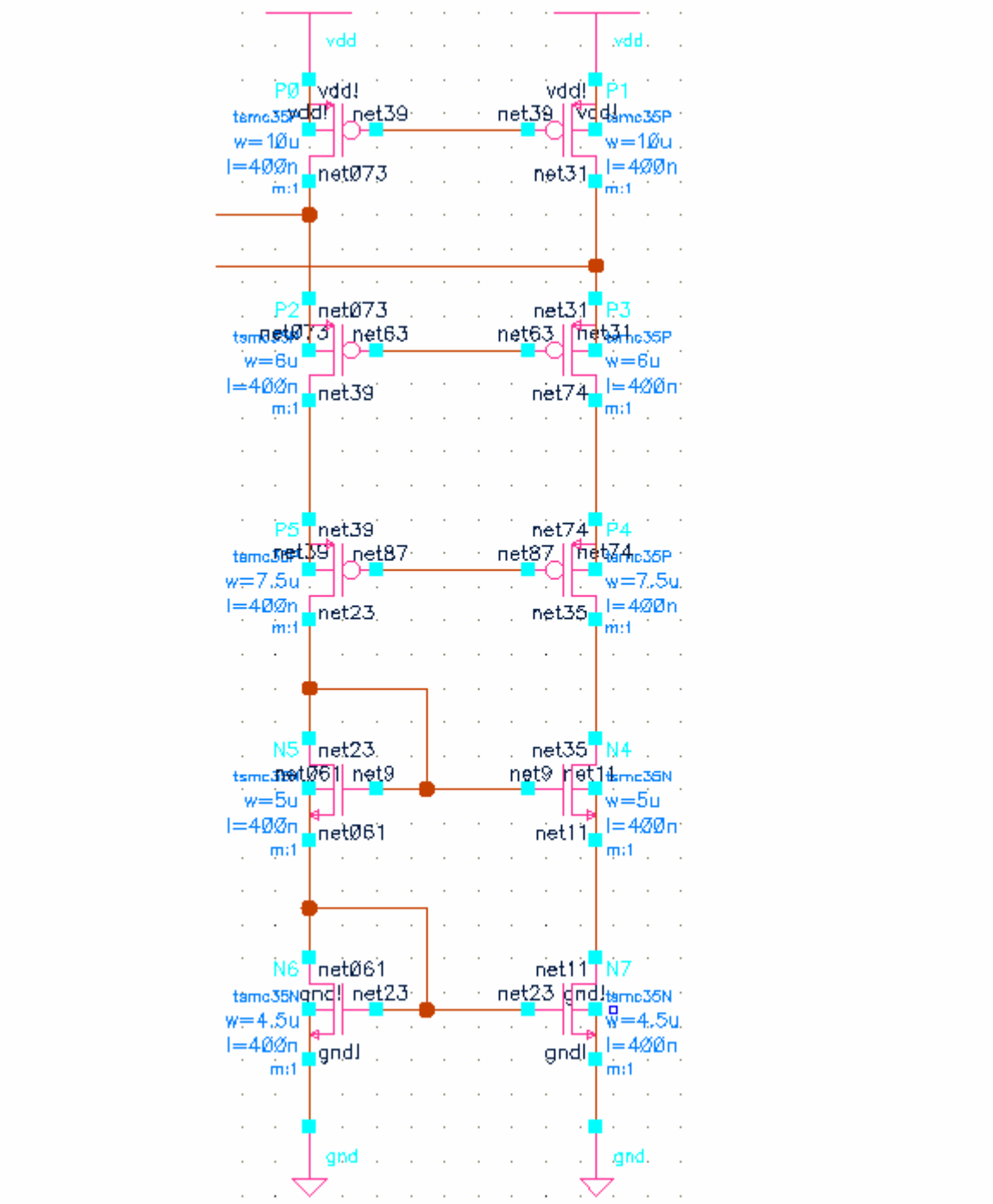
This stage provides the required load and output resistance stage before output stage. High output resistance of this stage would yield high gain from this stage, so emphasis of this stage is to achieve high output resistance without degrading phase response of the system. Following configurations were considered:-

A) High Gain-Low Swing-High Power Cascode Stage (HGLSHP)



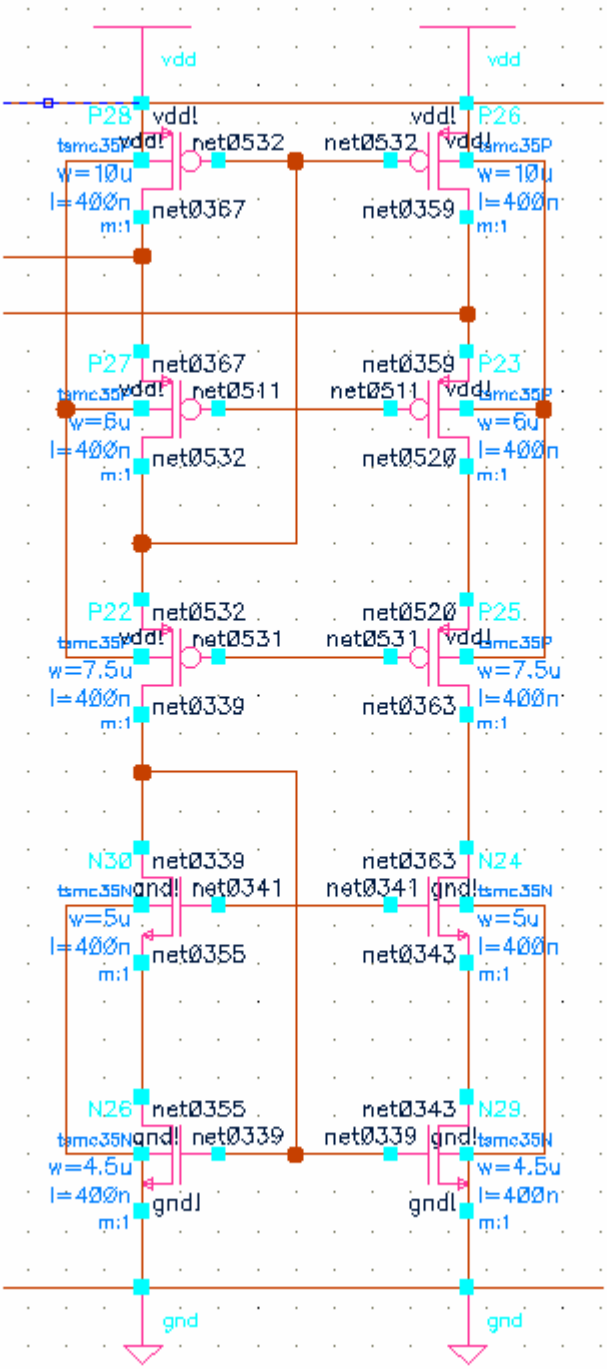
This stage contains three PMOS pairs cascoded over NMOS pairs. The pairs are separately biased there by consuming high power. The output resistance looking into net 35 is very large as it would have source degenerated transistors providing high gain to output stage. However the maximum output swing available at net 35 (which is output point) is low as it would have reduction of Von of five devices from VDD. The output will be differential from this stage which then will have to be converted to single ended output in output stage.

B) High Gain-Low Swing-Low Power Cascode Stage (HGLSLP)



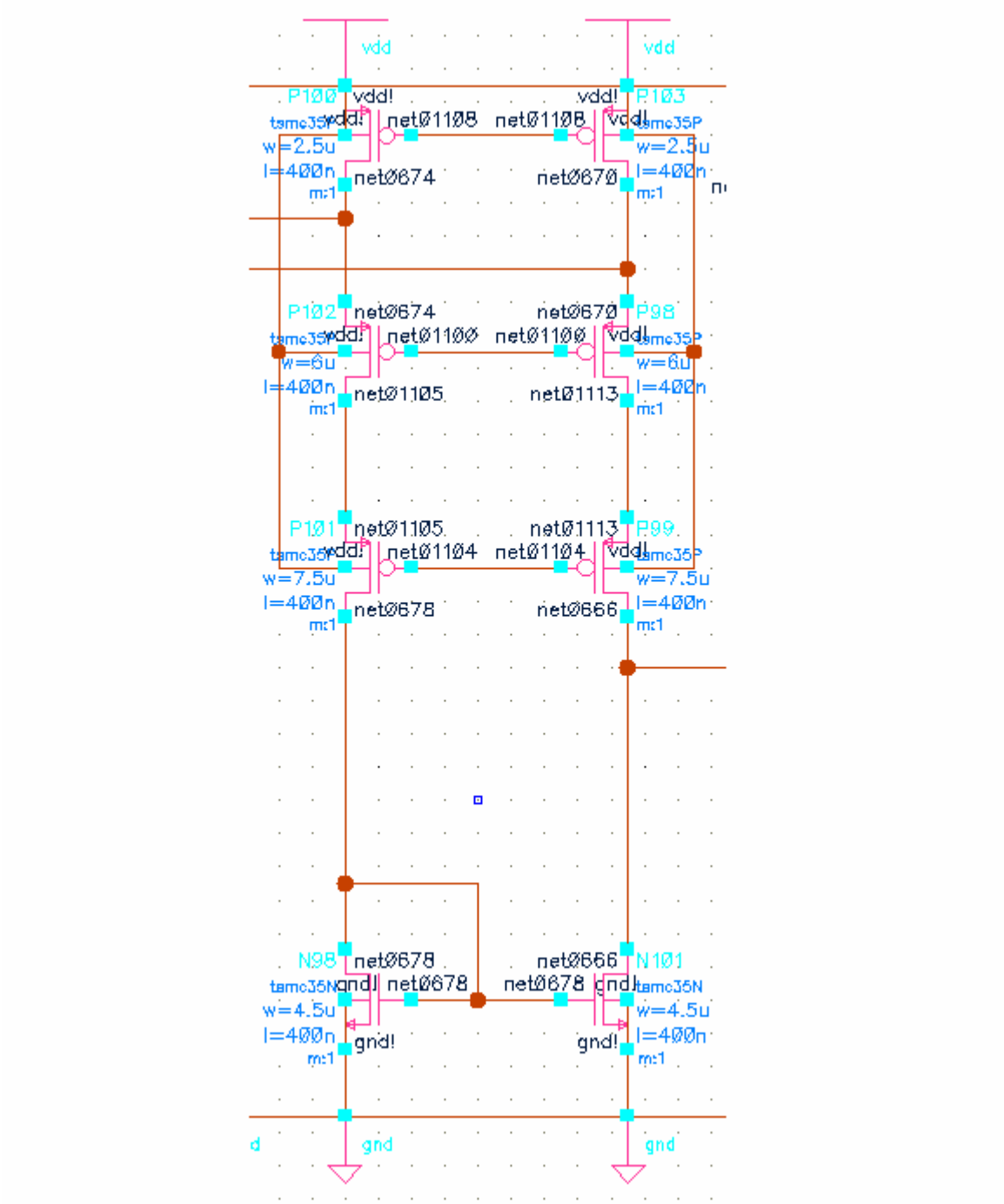
If we connect last two NMOS pair of previous configuration as current mirror then the biasing of these two will be automatic and there by reducing substantial current consumption using less power. The output resistance is still the same there by providing high gain. How ever due to mirroring of bottom two transistors would induce a mirror pole in AC response of this circuit degrading phase response substantially. The output voltage swing in this configuration is reduced by a drop of two Vthn of bottom two transistors. Further more this circuit will provide single ended output to final stage.

C) High Gain-High Swing-Low Power Cascode Stage (HGHSLP)



The main drawback of previous configuration was low voltage swing. Instead of using a simple current mirror for transistors a low voltage current mirror; this would enhance output swing range as it will have only Von of five transistors deducted from VDD. The gain of this configuration would be same as earlier and power consumption of this would be little less than previous one as biasing is reduced for only three MOS and rest of them are automatically biased. However this configuration would induce two mirror poles in AC response which would be heavily detrimental to phase response which will be discussed later in this report.

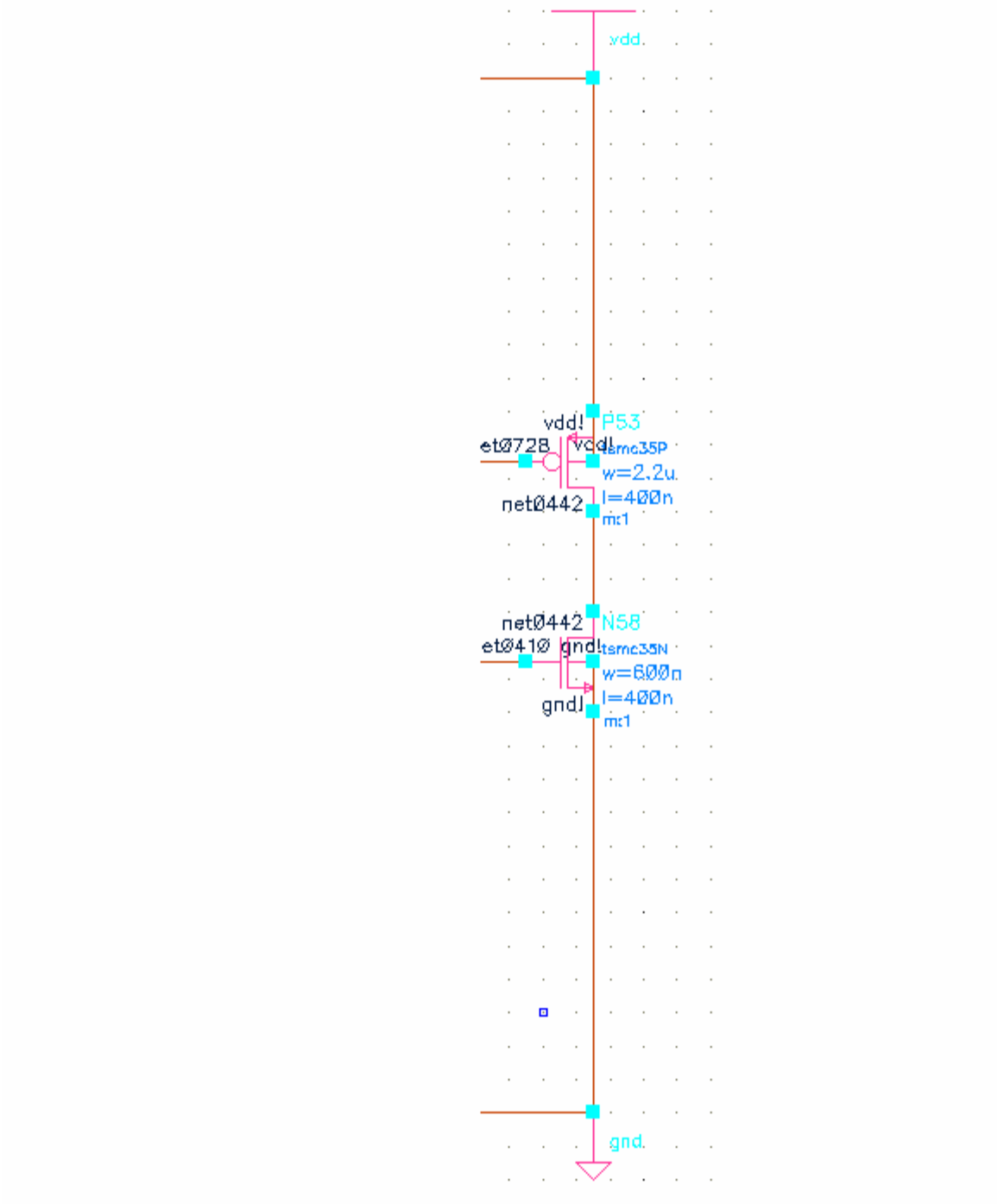
D) Low Gain-High Swing-Low Power Cascode Stage (LGHSLP)



This configuration is finally implemented in the design. The configurations earlier discussed had high output resistance there by contributing heavily to first pole of the AC response. Further the current mirror in the signal path induced a non dominant pole close to low frequency range which degraded phase response rapidly causing the system to be unstable. This configuration is the middle approach which sacrifices the gain for better unity gain band width and stability. The output resistance of this configuration is low as compared to previous ones causing gain to decrease. Power dissipation is low as number of cascodes is reduced. Swing range is enhanced with reduction of cascodes.

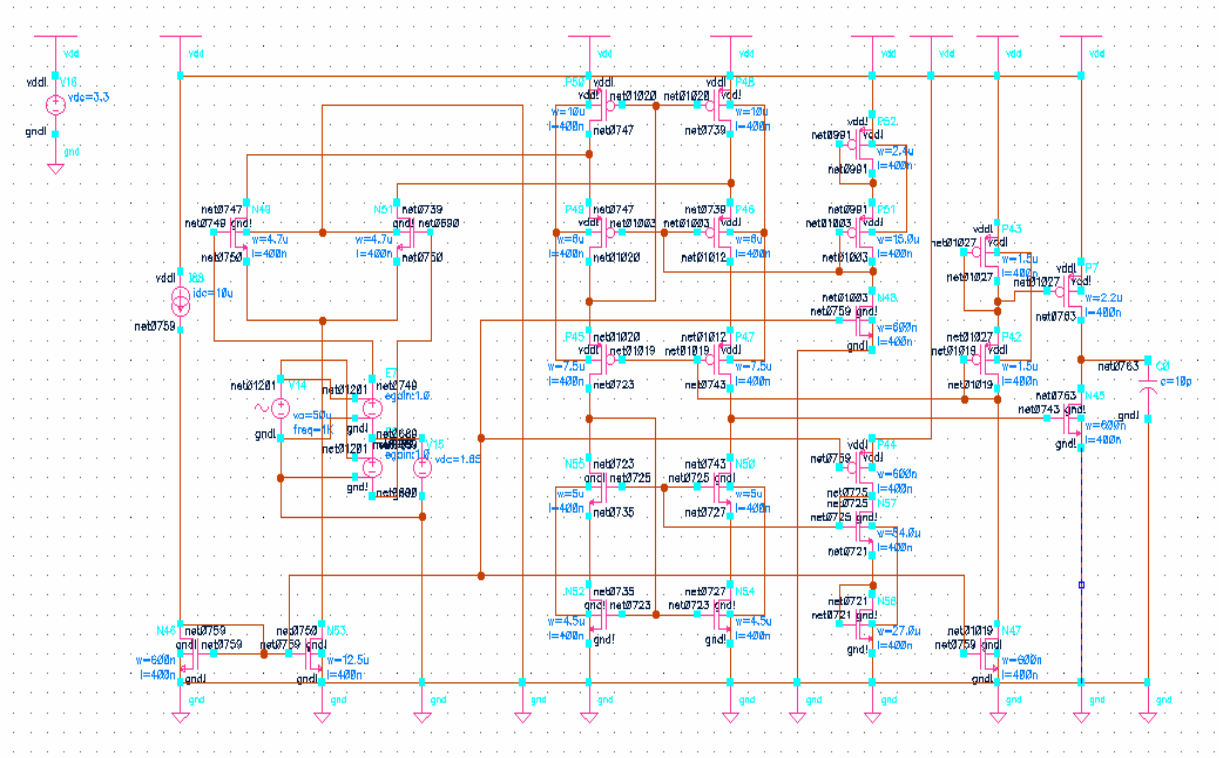
3) Output Stages:-

The main function of output stage will be to enhance overall OVSR and simultaneously providing gain enhancement to previous stage. However it would induce extra pole in the AC response of the circuit. It is also desirable that this stage should consume low current The output stage used in this design is a common source amplifier with a current source load. Output is taken from joining point of output stage. The upper transistor is acting as a current source and bottom transistor is acting as a driver.



Test Structure:-

The following test structure was tested initially to verify the postulations made above.



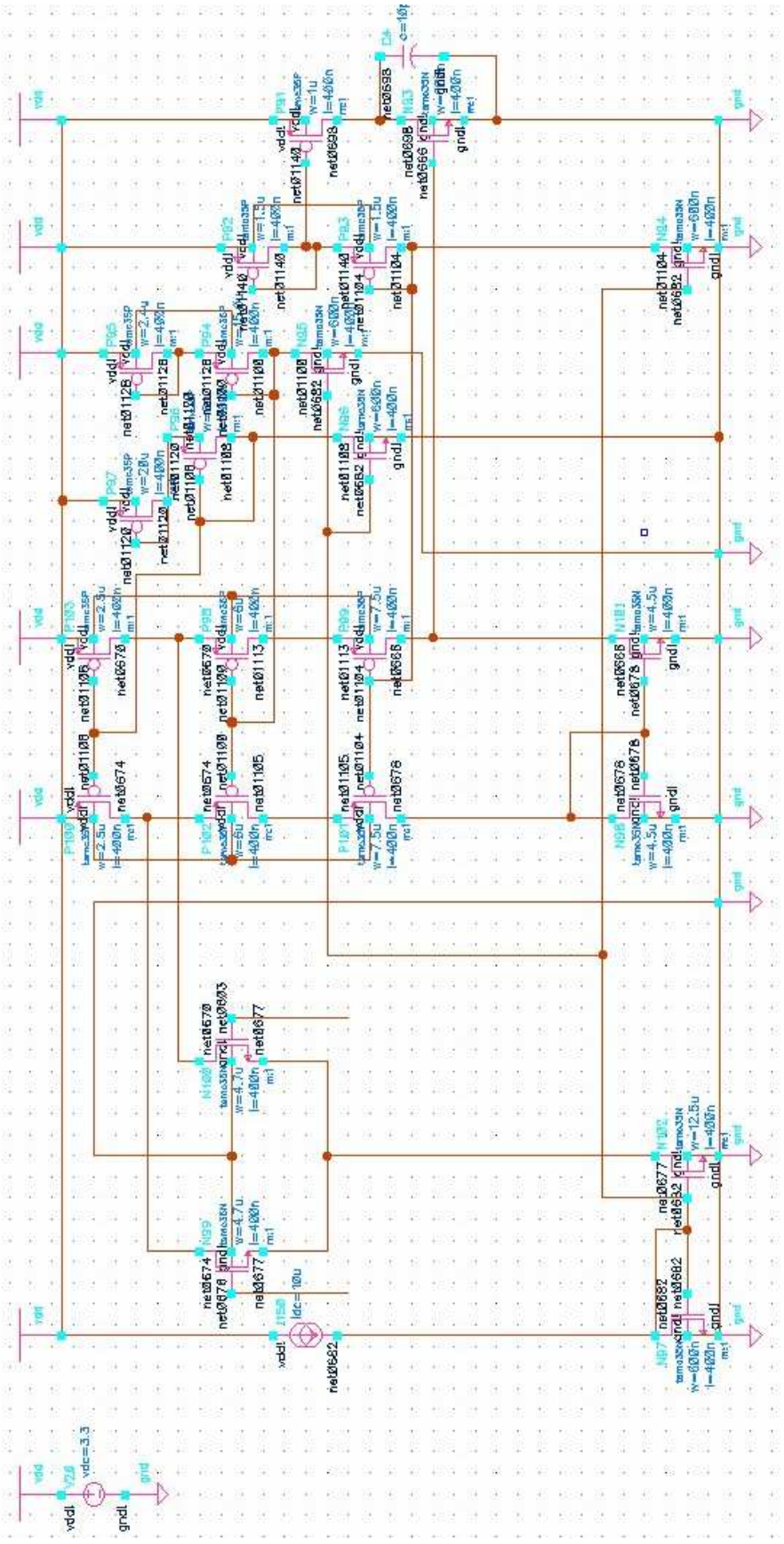
This structure consisted of differential input stage as two NMOS transistors carrying 50 micron of current each, the folded cascode stage comprised of low voltage current mirror as load, the current consumed in this branch is approximately 50 microns each branch. The current mirrors used approximately 10 microns of current each. The output stage was common source stage consuming 12 microns of current. The overdrive assigned to each cascode pair varied as 0,5V, 0.3V, 0.3V, 0.2V, 0.2V to obtain maximum voltage swing from first stage. The sizing of transistors was done once current and overdrive voltages have been assigned. Note that the current mirrors uses a diode connected load to have better control over Vgs of respective current mirror.

Test Results:-

This design provided a gain of 63dB from first stage and 20 dB from second stage making overall gain as 83dB with a common mode rejection of 116dB. OVSR, ICMR were greater than 3V. Current consumed was 230 microns well below maximum limit of 303 microns. Unity gain bandwidth obtained was 67MHz. Slew rates obtained were in excess of 10V/usec and differential input resistance was greater than 1Meg. However the parameter of concern was phase margin which was very less as expected due to two mirror poles. It cause system to operate just above instability i.e. phase margin of 6 degree.

So some changes were made in circuit and following is final circuit.

FINAL CIRCUIT



This structure consisted of differential input stage as two NMOS transistors carrying 50 micron of current each, the folded cascode stage comprised of four MOS cascoded with the bottom one as a current mirror to provide single ended output, the current consumed in this branch is approximately 50 microns each branch. The current mirrors used approximately 10 microns of current each. The output stage was common source stage consuming 12 microns of current. The overdrive assigned to each cascode pair varied as 0,5V, 0.3V, 0.2V, 0.2V to obtain maximum voltage swing from first stage. The sizing of transistors was done once current and overdrive voltages have been assigned. Note that the current mirrors uses a diode connected load to have better control over Vgs of respective current mirror.

Test Results:-

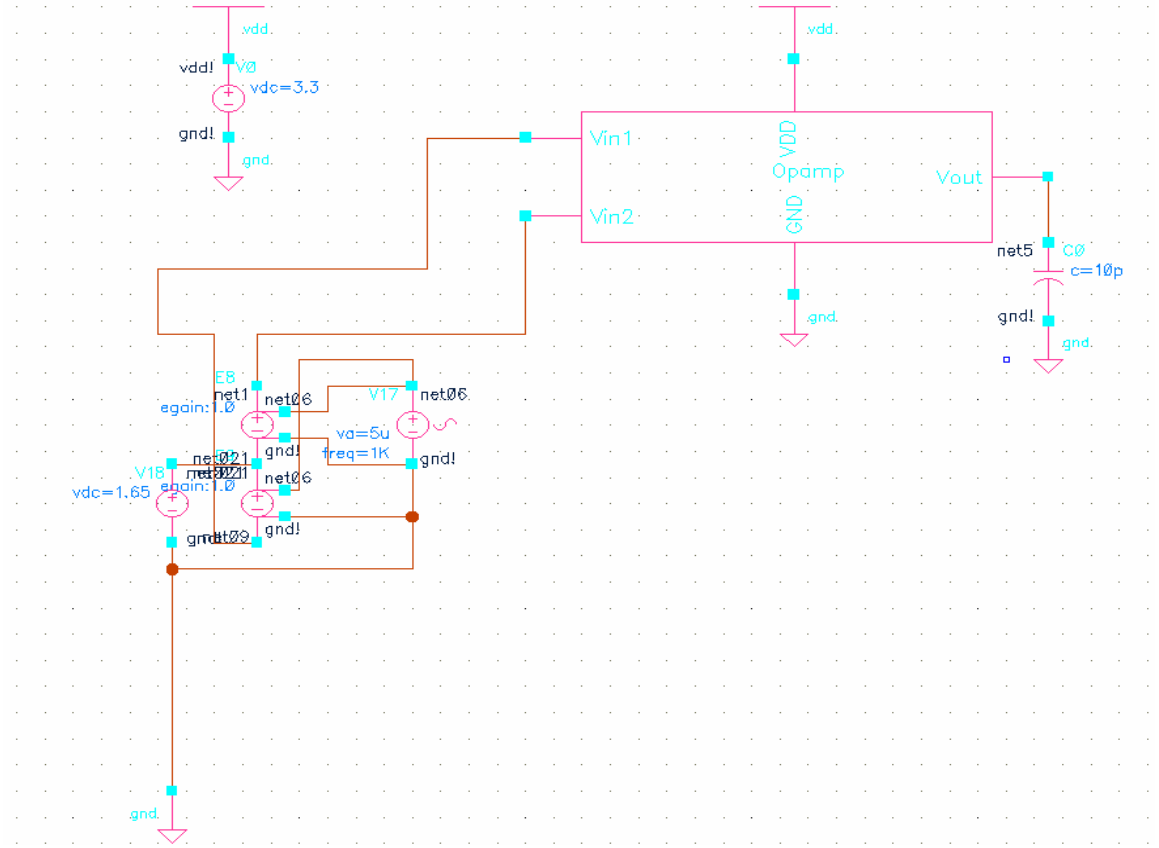
This design provided a gain of 36dB from first stage and 20 dB from second stage making overall gain as 56dB with a common mode rejection of 165dBdB. OVSR, ICMR were greater than 3V. Current consumed was 230 microns well below maximum limit of 303 microns. Unity gain bandwidth obtained was 40MHz. Slew rates obtained were in excess of 10V/usec and differential input resistance was greater than 1Meg. The phase margin was much better than previous test structure as expected which came out to be 45 degree making design relatively stable.

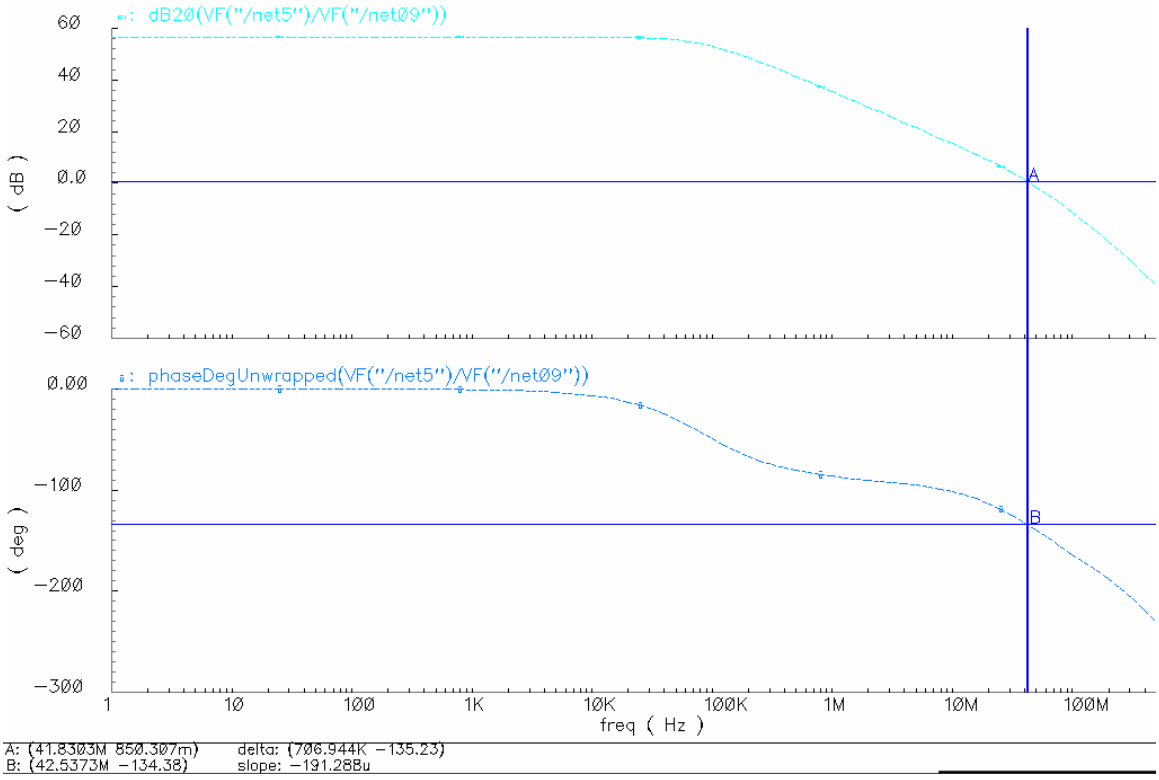
Following are detailed test results

Transistor Sizes	Width	Length
Differential Pair (both)	4.7 micron	0.4 micron
PMOS Cascode Pair 1st	2.5 micron	0.4 micron
PMOS Cascode Pair 2nd	6.0 micron	0.4 micron
PMOS Cascode Pair 3rd	7.5 micron	0.4 micron
NMOS Cascode Pair 1	4.5 micron	0.4 micron
Output Stage		
Driver NMOS	0.6 micron	0.4 micron
Load PMOS	1.0 micron	0.4 micron
Tail Current Source NMOS	12.5 micron	0.4 micron

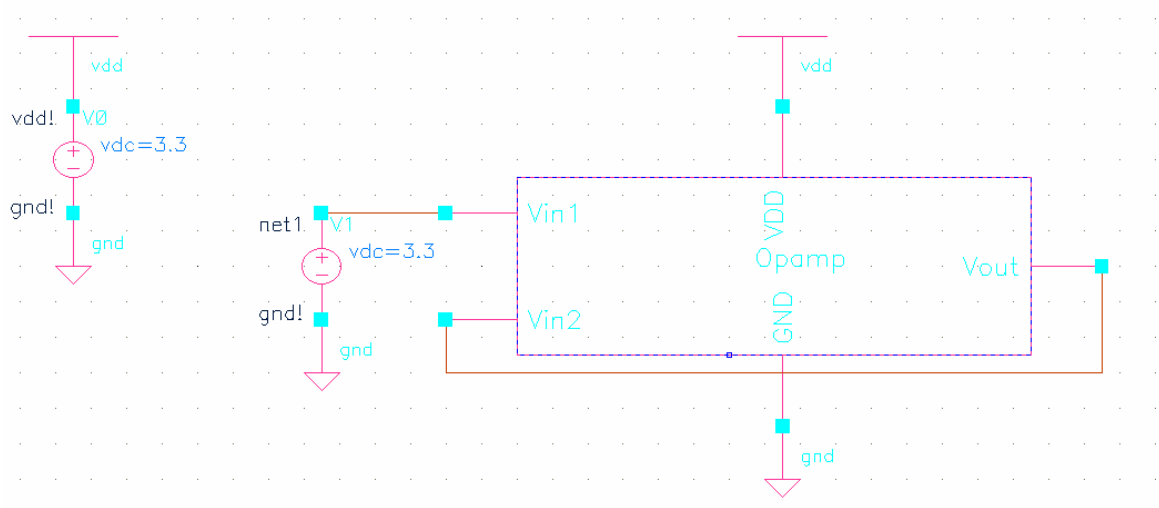
Biasing Transistor sizes can be viewed from the schematic

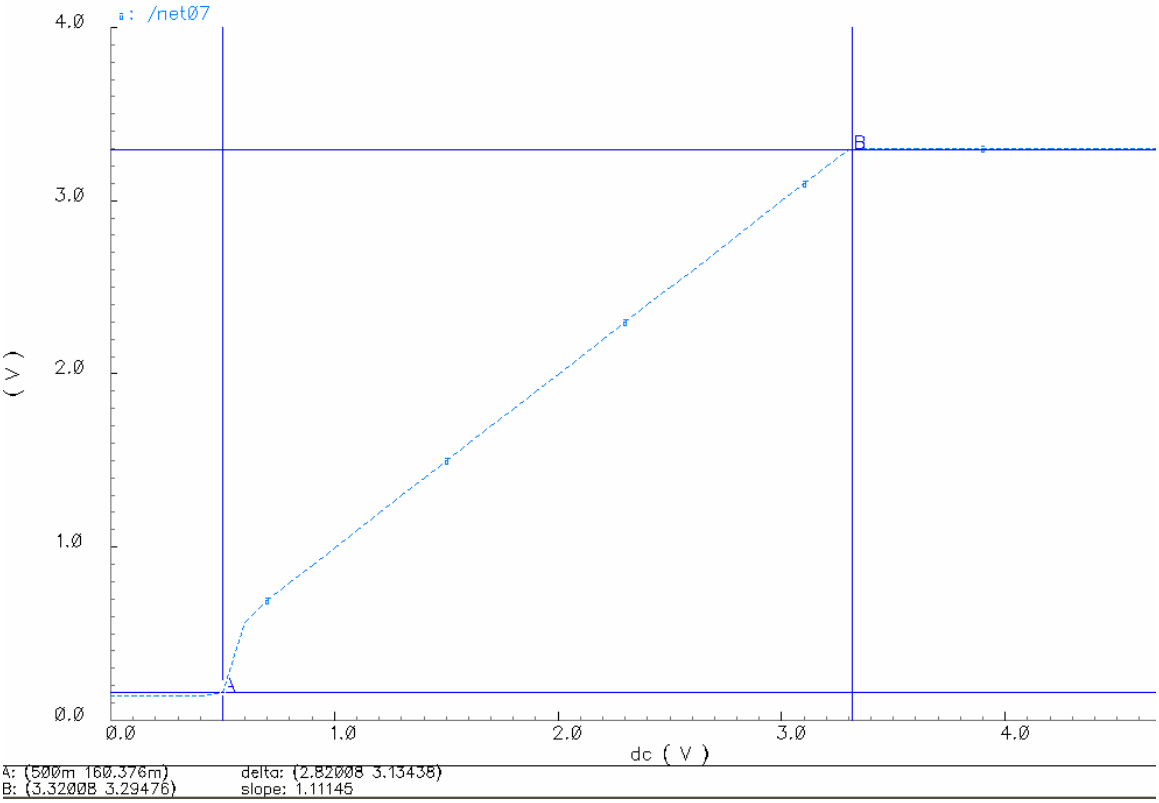
Test For Differential Voltage Gain, Unity Gain Bandwidth, Phase Margin



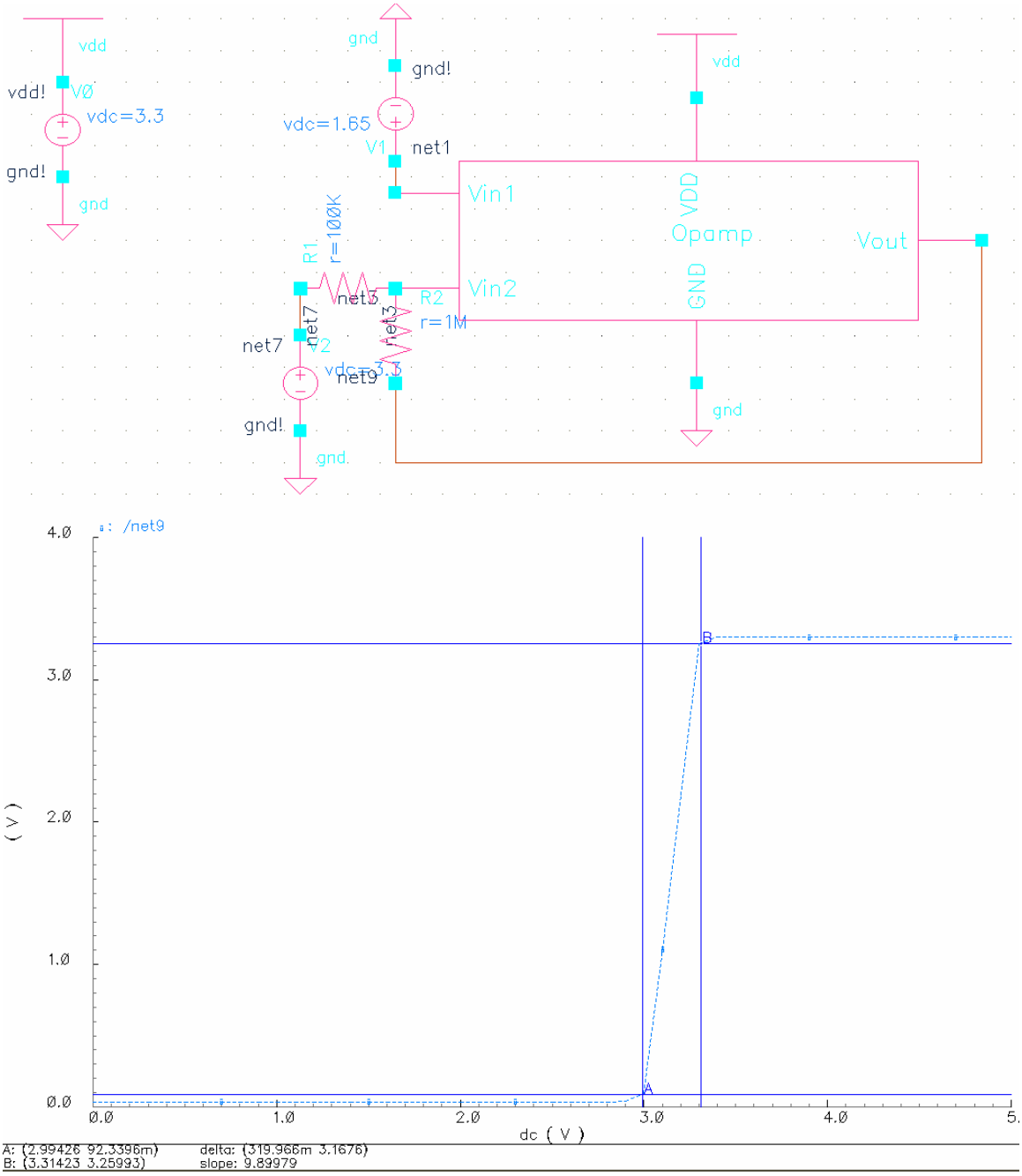


Test For Input Common Mode Range

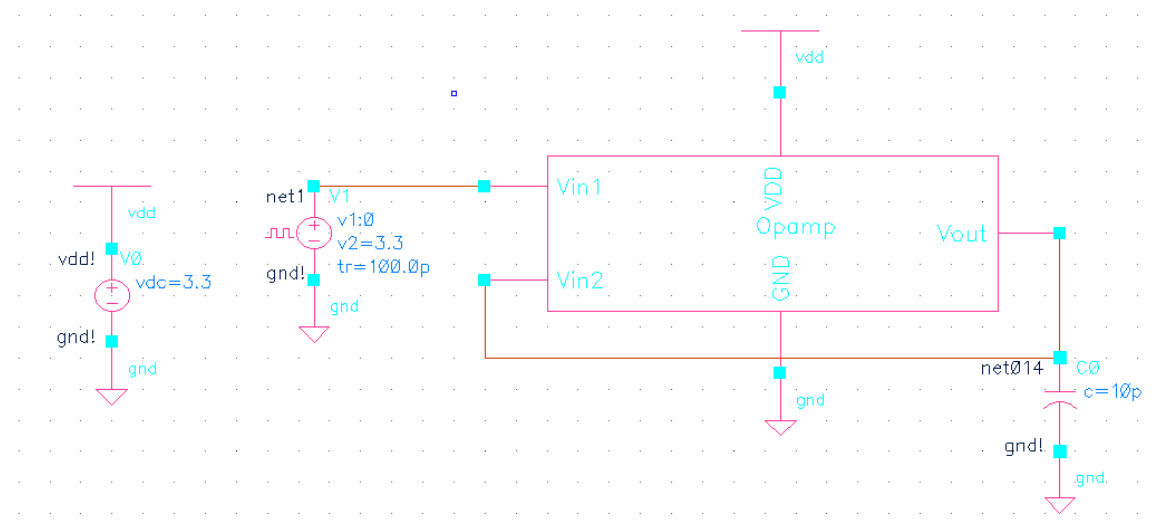


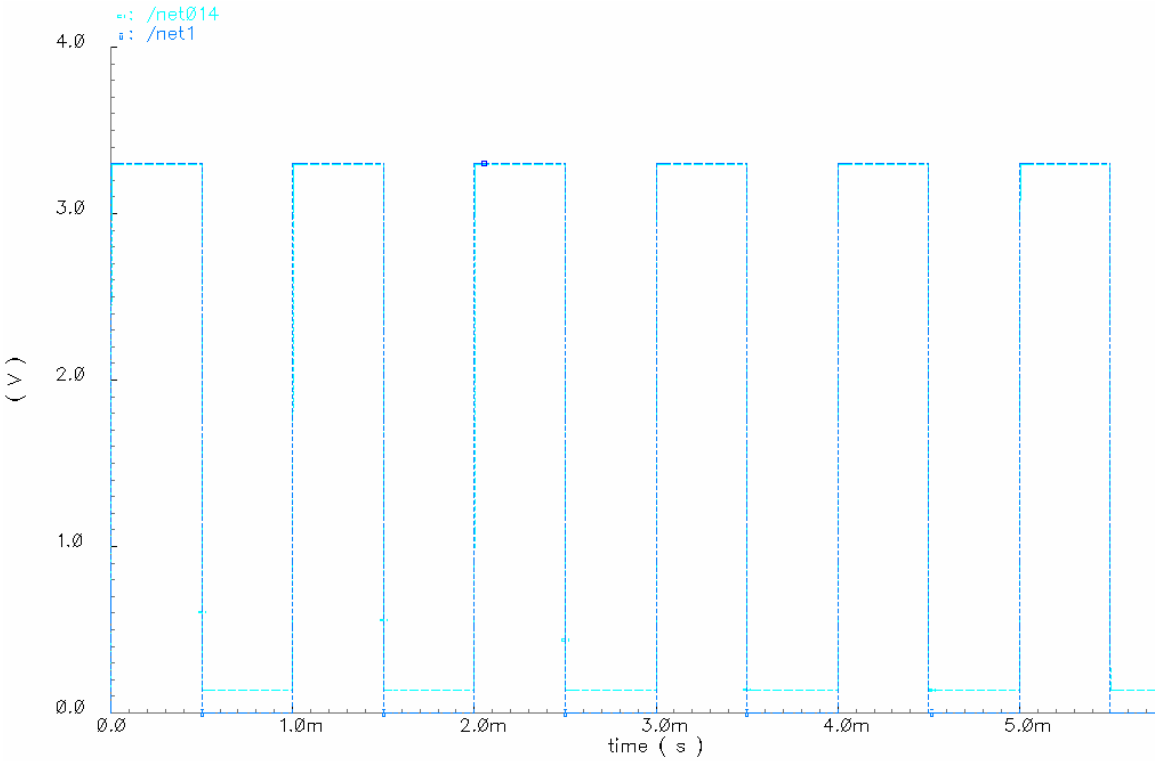


Test For Output Voltage Swing Range

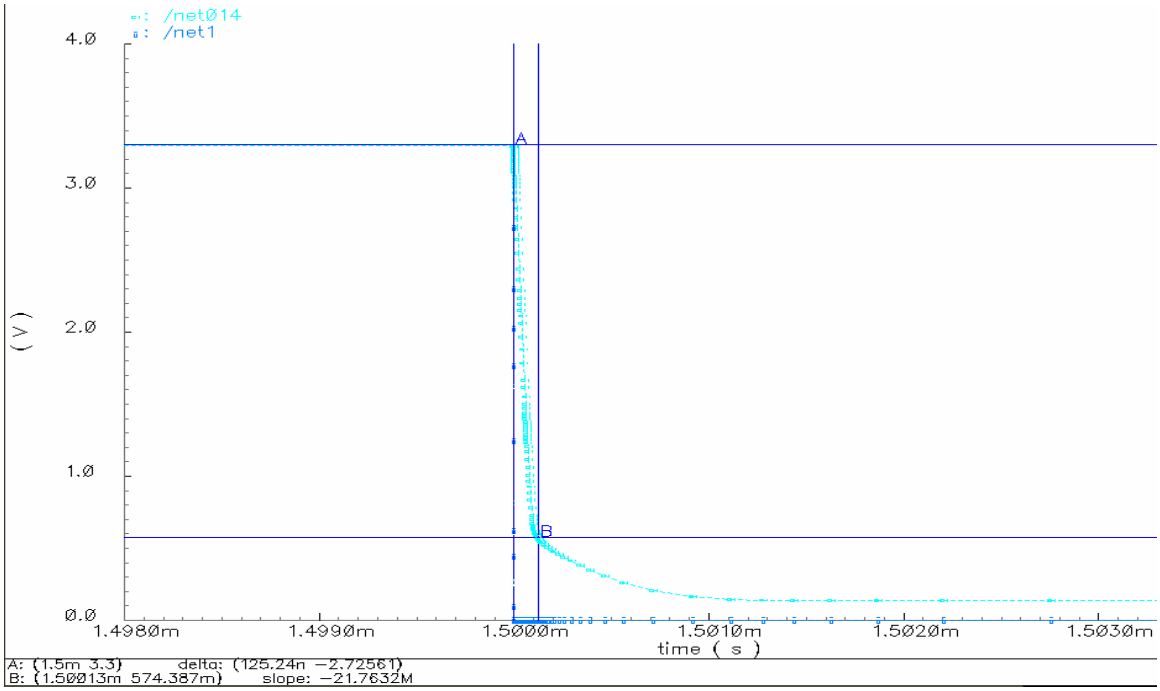


Test For Slew Rate

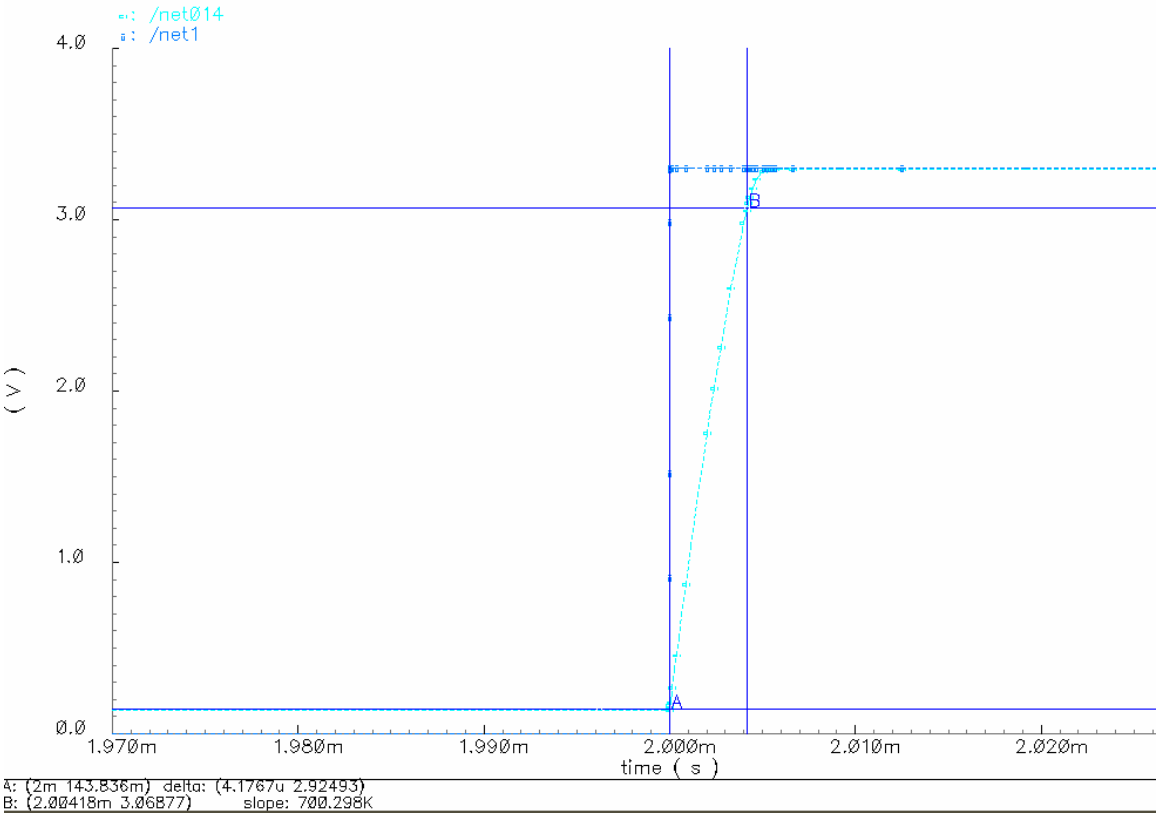




Slew Rate For Falling Edge

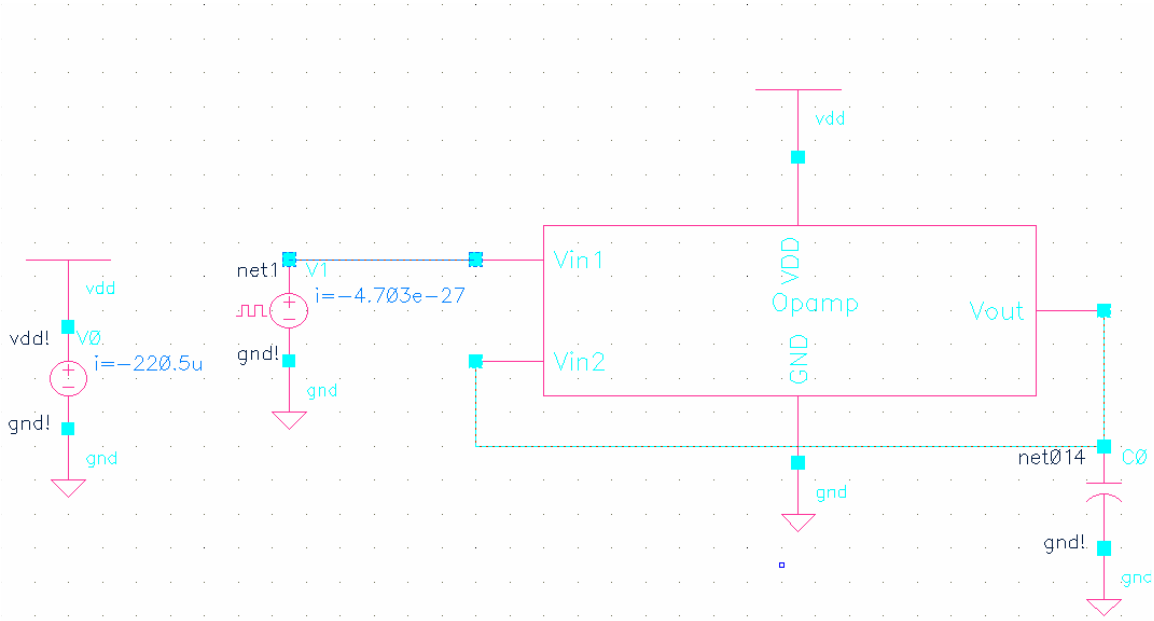


Slew Rate For Rising Edge



Average Slew Rate is 11.23V/usec.

Test For Power Dissipation

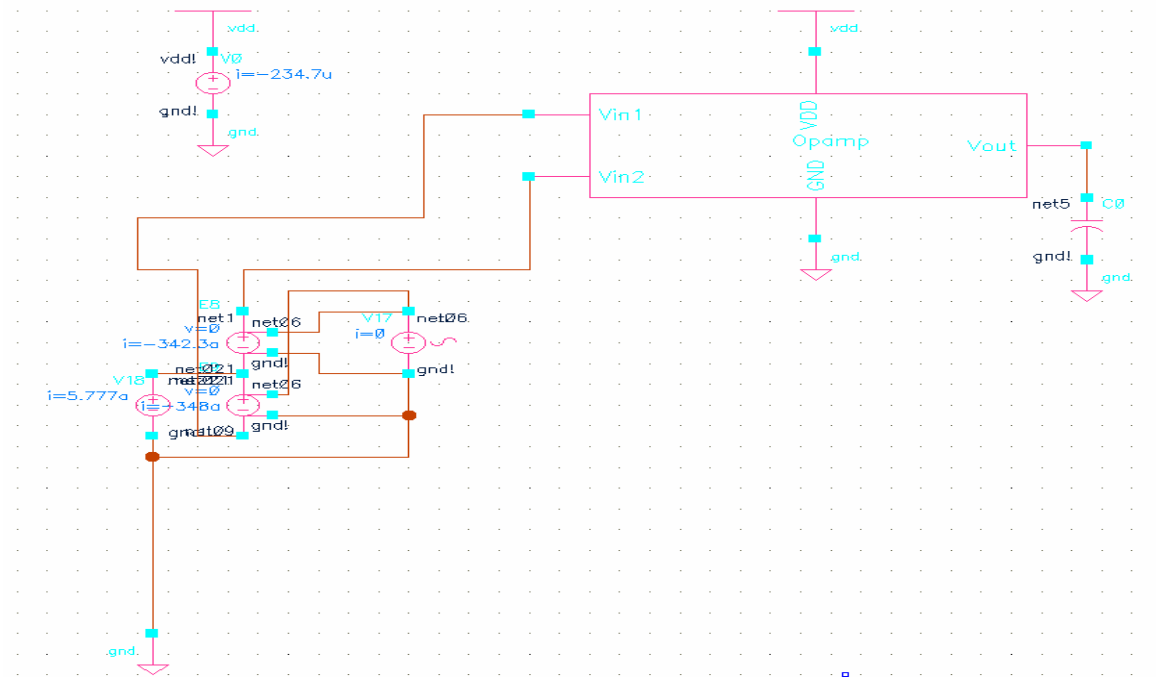


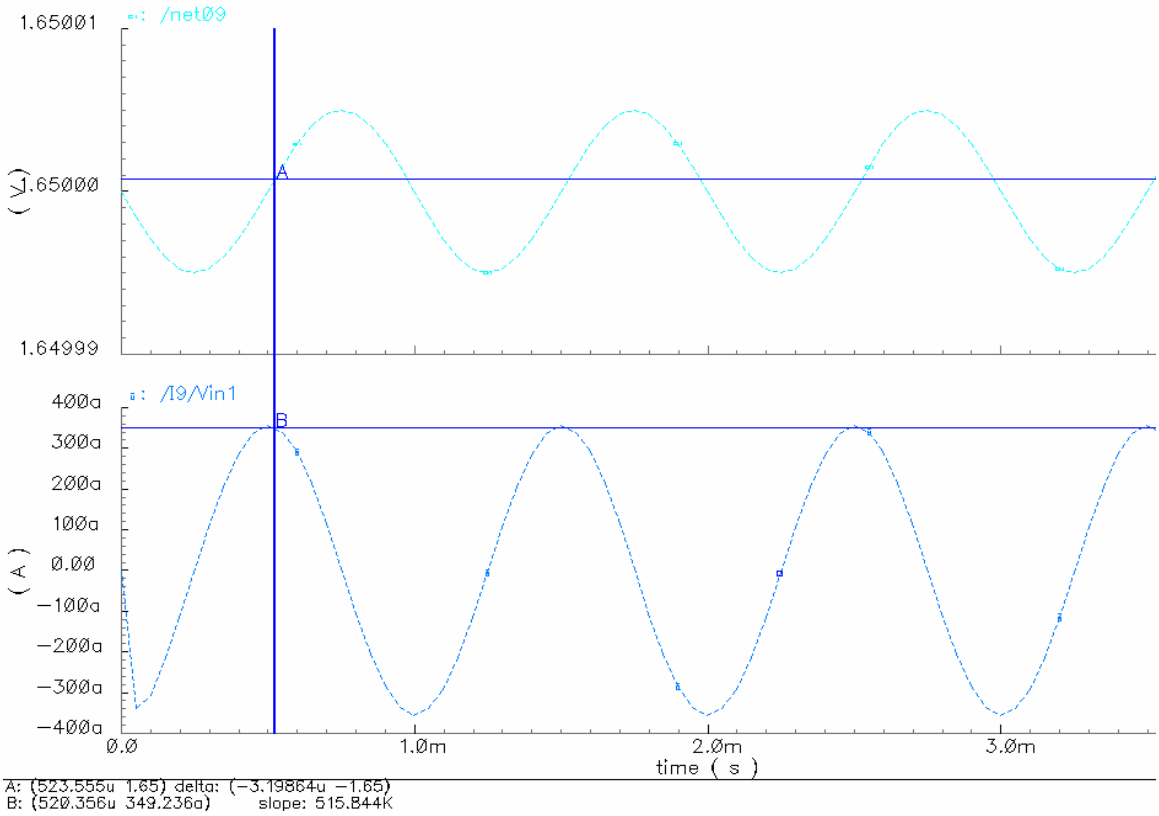
As we can see that circuit is consuming 220.5 microns of current from source and VDD is 3.3V. So power dissipation is

Pdiss = I * VDD

0.7276 m Watts

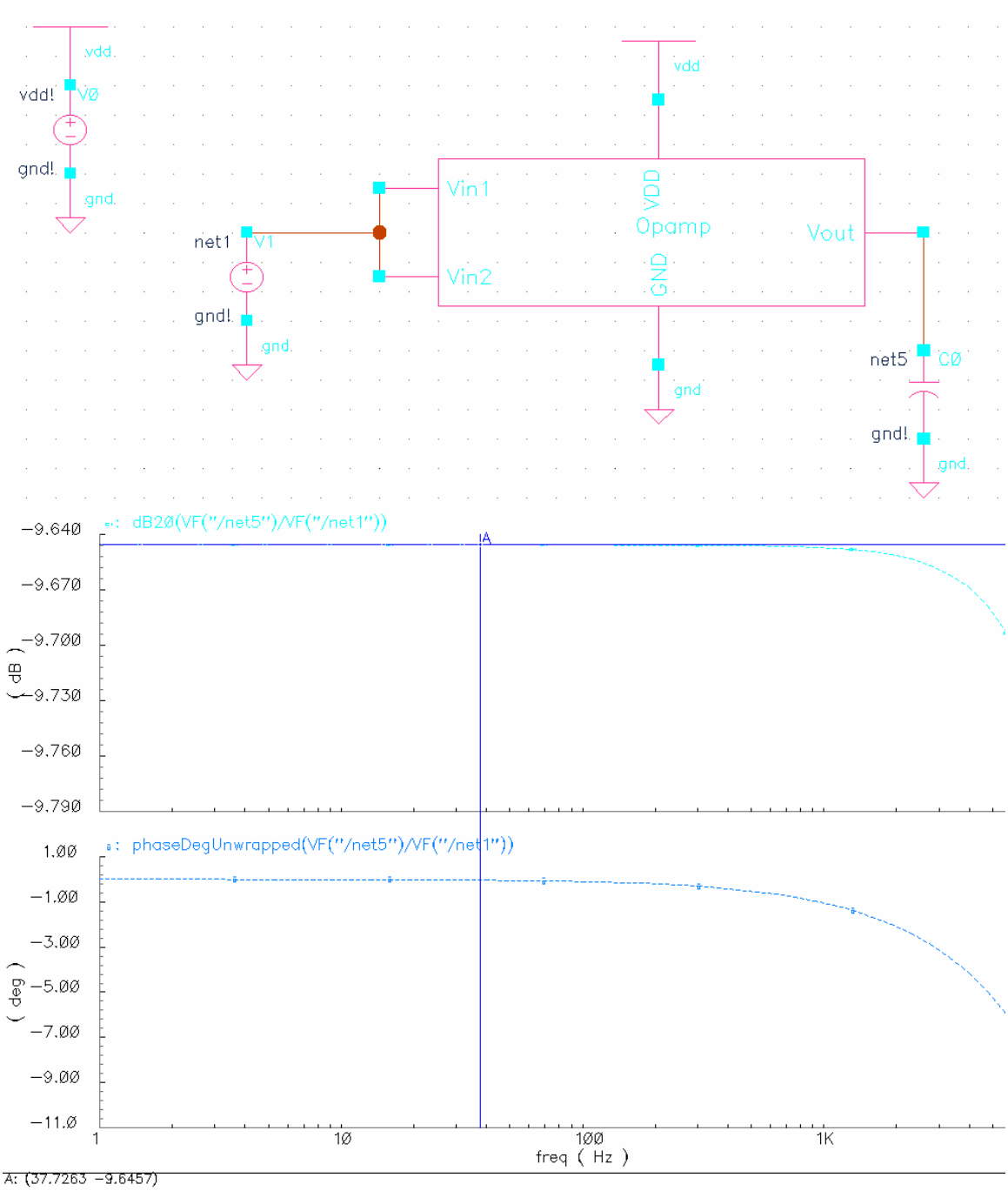
Test For Differential Input Resistance





Differential input resistance is Vin/Iin = 1.65/349.23a = 47.2Meg

Test For Common Mode Rejection Ratio



The input applied has a DC bias voltage of 2V with an ac magnitude of 1V. The graphs shows AC gain for common mode input, the differential gain is 56dB. So CMRR will be

CMRR = 56-(-9.64) = 65.64dB