Full Custom Design of a Two-Stage Fully Differential CMOS Amplifier with High Unity-Gain Bandwidth and Large Dynamic Range at Output

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***Abstract*— This paper presents the full custom design of a two-stage fully differential CMOS amplifier with outstanding characteristics of high unity-gain bandwidth and large dynamic range at output. Both the theoretical calculations and computer-aided simulation analysis are given in detail. The simulation results in CSMC 0.6μm CMOS process from a 5V voltage-supply demonstrate that the designed amplifier has satisfied state-of-the-art design specifications with a dedicated optimization technique: The amplifier exhibits a large output swing of nearly ±4.75V, a fast settling time of less than 13.4ns to the 0.05% accuracy; While the open-loop amplifier has a considerable gain as high as 86.8dB, the differential AC loop unity-gain band-width reaches 966MHz and the dynamic range at output gets 84.4dB. In this paper, we also present how to efficiently design and further optimize the circuit topology and parameters in order to meet some strict specifications given in advance for a specific engineering project.**

I. INTRODUCTION

As for various recently-developed high-performance integrated electronic systems or subsystems, e.g. A/D converter, switched-capacitor filter, RF modulator and audio system, CMOS operational amplifiers with high unity-gain bandwidth and large dynamic range are necessitated. Currently there have been many CMOS op amps designed to meet those requirements [1]-[3]. In [1], a gain-boosted two-stage fully differential op amp from 5V power supply with 512MHz unity-gain bandwidth and 6V output swing was presented. In [2], a telescopic op amp from a supply of 3V with an output swing of 2.45V was developed.

According to the comparison of performance of various op-amp topologies existed, this paper presents the full custom design of a telescopic two-stage fully differ-rential CMOS amplifier with outstanding characteristics of high unity-gain bandwidth and large dynamic range at output. As for state-of-the-art design specifications given in advance, both the theoretical calculation and simulation analysis are given in detail in CSMC 0.6μm n-Well double-poly double-metal CMOS process.

The preliminary custom design specifications of the op amp are given in Table I as below.

TABLE I. CUSTOM DESIGN SPECIFICATIONS OF THE AMPLIFIER

Specification Names	Values
Supply V_{DD}	V_{DD}=5V
Dynamic Range at Output (DR)	$DR = 10\lg\frac{P_{peak-signal}}{P_{noise}} \geq 70dB$
Closed-loop Gain (G_{Cl})	$G_{Cl}\geq 2$
Settling Accuracy (ε)	ε≤0.05%
Settling Time (T_S)	T_S≤30ns
Feedback Capacitance (C_f)	C_f=0.5pF
Load Capacitance (C_L)	C_L =3pF
Power Consumption	Minimization

II. THEORETICAL ANALYSIS FOR SELECTING CIRCUIT TOPOLOGY

A. Determine the necessary open-loop gain (A_o)

First, starting from the closed-loop gain baseline ($G_{Cl}\geq 2$), we can yield the input capacitance approximately

$$C_i \approx C_f \times G_{Cl} = 1pF \tag{1}$$

As illustrated in Fig.1, the closed-loop gain is equal to [4]

$$G_{Cl} = \frac{C_i}{C_f}\frac{A_o}{\frac{1}{F}+A_o} \tag{2}$$

Where F is the feedback factor and

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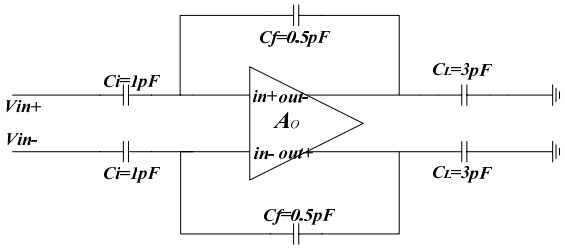


Fig.1. Simulation setup for the open-loop & closed-loop amplifier

$$F = \frac{C_f}{C_f + C_i + C_{gs}} \approx \frac{1}{3} \tag{3}$$

Since $A_O F >> 1$, (2) can be transformed to

$$G_{Cl} = \frac{C_i}{C_f}\frac{A_o}{\frac{1}{F} + A_o} \approx \frac{C_i}{C_f}(1 - \frac{1}{FA_o}) \tag{4}$$

Here assuming that the Static Settling Accuracy is half of the total Settling Accuracy, we now obtain the Static Settling Accuracy (ε_s) as

$$\varepsilon_s = \frac{1}{A_o F} = \varepsilon / 2 \le 0.025\% \tag{5}$$

Thus, the open-loop gain of the amplifier is required as

$$A_O = \frac{1}{F\varepsilon_s} = \frac{1}{F \bullet \varepsilon / 2} \ge 12000 \Leftrightarrow 81.58dB \tag{6}$$

B. Determine the related parameters for the given settling time specification

The settling time of the amplifier is required to be T_S≤30ns that we can further deduce from [5] as

$$\begin{aligned} T_S &= -\frac{1}{FA_o S_p}\ln(\varepsilon - \frac{1}{FA_o}) \\ &= -\frac{1}{F \bullet GBW}\ln(\varepsilon - \varepsilon_s) \le 30ns \end{aligned} \tag{7}$$

Where $\varepsilon_s = \varepsilon / 2 \le 0.025\%$ is shown in (5), GBW is the gain-bandwidth product. Then we'll have

$$GBW = \frac{-1}{F \bullet T_S}\ln(\varepsilon - \varepsilon_s) \ge 829.4MHz \tag{8}$$

Thus, the equivalent transconductance of the amplifying circuits should be

$$G_m = GBW \bullet C_L \ge 2.488mS \tag{9}$$

It might be as well if assuming $G_m/I_d=10V^{-1}$, then we'll get the condition for bias current at each branch:

$$I_d \ge 248.8\mu A \tag{10}$$

However, 248.8μA is a relatively ideal value for the bias current not in consideration of other parasitic capacitors. The current required in the final design should be a little larger.

C. Determine the necessary output voltage swing($V_{o,sw}$)

Here we consider an ideal case: the noise produced in the amplifier is given by [4]:

$$V_{on}^2 \approx \frac{4}{3} \bullet \frac{K_b T}{C_L} \bullet \frac{1}{F} = 177.4(nV^2 / Hz) \tag{11}$$

As for this custom design amplifier, the dynamic output range is specified as $DR = 10\log\frac{P_{peak-signal}}{P_{noise}} \ge 70dB$, thus

$$\begin{aligned} &\frac{P_{peak-signal}}{P_{noise}} = \frac{V_{O,Swing}^2 / 2}{V_{on}^2} \ge 10^7 \\ &\Rightarrow V_{O,Sw} \ge \sqrt{2V_{on}^2 \bullet 10^7} = 1.89V \end{aligned} \tag{12}$$

Add more neglected noise in; the output swing should be much larger than this ideal calculated baseline value.

D. Selection of the amplifier topology

In order to achieve the most efficient design based on the above analysis results, we'd outline the comparison of performance of various amp topologies [1]-[7] in Table II.

TABLE II. COMPARISON OF PERFORMANCE OF VARIOUS OP-AMP TOPOLOGIES

	Gain	Speed	Output Swing	Noise	Power Consumption
Telescopic					
Folded-Cascode					
Multi-Stage					
Gain-Boosted					

LOWEST LOW MEDIUM HIGH HIGHEST

Now look at expressions (6)(9)(12) listed above, we conclude that the amplifier specifications emphasize on the large output swing, the high open-loop gain on the order of $(g_m r_o)^3$, the unity gain bandwidth on the order of 800MHz and the low noise performance. As seen from Table II, the telescopic and multi-stage topologies seem to be more suitable for the design. If pure telescopic, it will suffer from low output swing and medium gain despite meeting the custom design specifications yet. While as for the multi-stage topology, especially more than two stages, the stability problem will become severe for us.

Hence, we'll depict the two-stage topology method for the amplifier design in this paper.

III. TWO-STAGE AMPLIFIER SCHEMATIC DESIGN

A. Main Amplifier Schematic

Fig.2 illustrates the main amplifying circuit schematic.

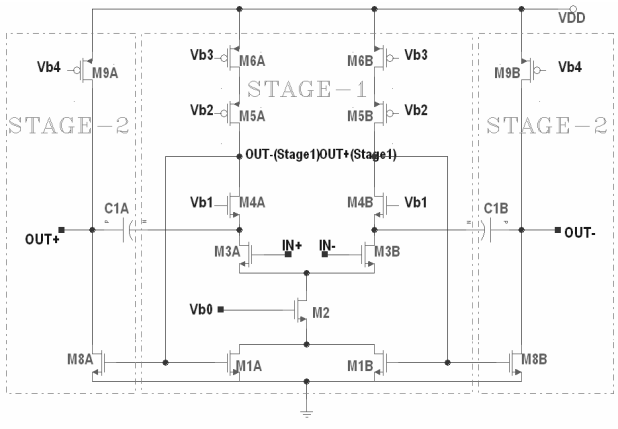


Fig.2. Main amplifier schematic.

The two stages are arranged as follows:

STAGE-1 is a typical telescopic architecture, for it can easily provide a sufficient gain for the total circuits and consumes low power. Note that, the output of Stage-1 acts as common-mode feedback to M1A/M1B, both of which work in the triode region for tuning the tail current. STAGE-2 is a simple Common-Source structure which mainly provides high output swing for the final amplifier. Two extra capacitors C1A/C1B are added between Stage-1 and Stage-2 for the sake of cascade compensation.

B. Biasing Network Schematic

Fig.3 shows the biasing network schematic for the main amplifier presented above. V_{b1}, V_{b2}, V_{b3}, V_{b4}, V_{b5} are the biasing voltages corresponding to those of Fig.2.

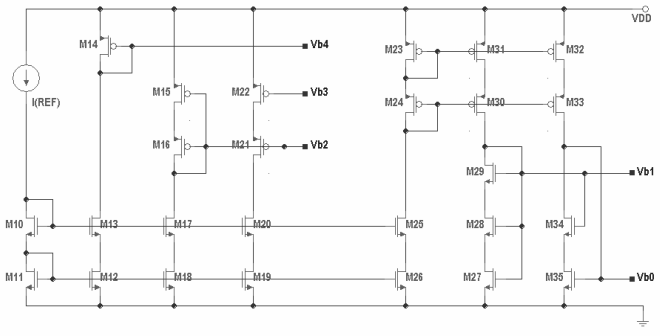


Fig.3. Biasing network schematic.

C. Total Circuits Topology of the Two-Stage Amplifier

As of now, the two main parts of the final amplifier, i.e. amplifying circuits and biasing network, have already been given. Fig.4 shows the holistic topology of the custom design two-stage amplifier in accordance with the specifications.

IV. SIMULATION RESULTS

A. Device Parameters

Under the specifications of open-loop gain, unity-gain bandwidth and output swing analyzed in Section II, the device parameters for Fig.2 and Fig.3 are calculated with the way referring to [4]. Table III gives the device parameters for the main amplifying circuits.

B. Test Options

The simulation setup is illustrated in Fig.1, where "A_o" is the differential amplifier shown in Fig.4. The custom design CMOS amplifier has been demonstrated using CSMC 0.6μm CMOS process from a single 5V voltage-supply.

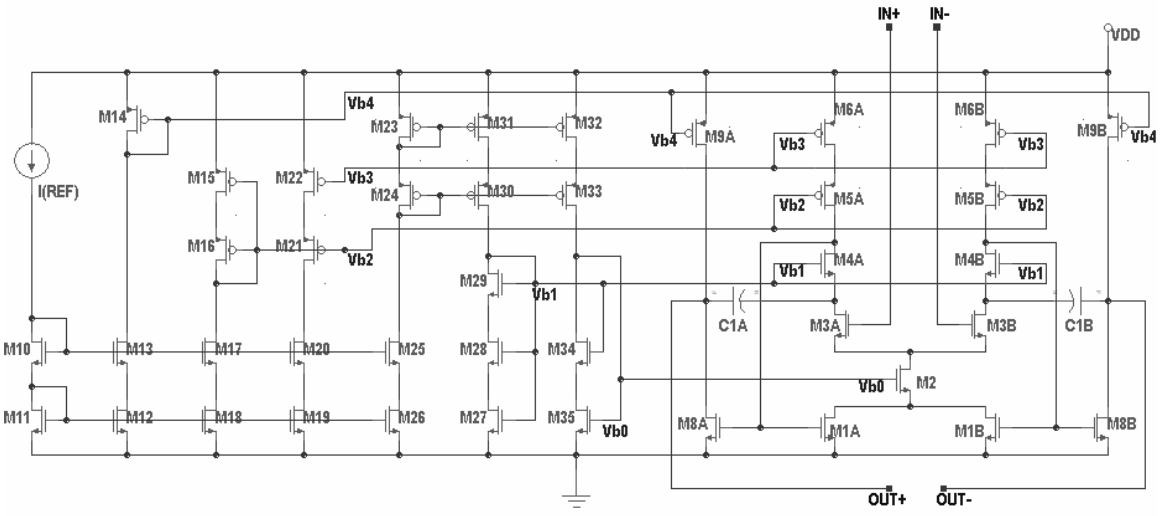


Fig.4. Holistic topology of the custom design two-stage amplifier

TABLE III. DEVICE PARAMETERS FOR THE MAIN AMPLIFIER PART

Device	Type	W(um)	L(um)	REMARK
M1A,M1B	N	90	0.6	Triode
M2	N	70	0.6	Saturation
M3A,M3B	N	300	0.6	Saturation
M4A,M4B	N	278	0.6	Saturation
M5A,M5B	P	300	1.0	Saturation
M6A,M6B	P	220	1.2	Saturation
M8A,M8B	N	150	0.6	Saturation
M9A,M9B	P	600	0.6	Saturation

C. Differential AC Open-Loop Frequency Response

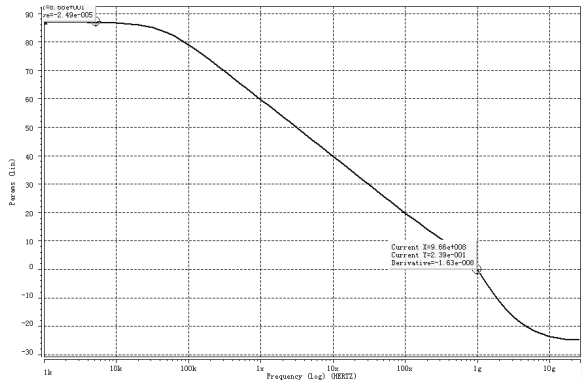
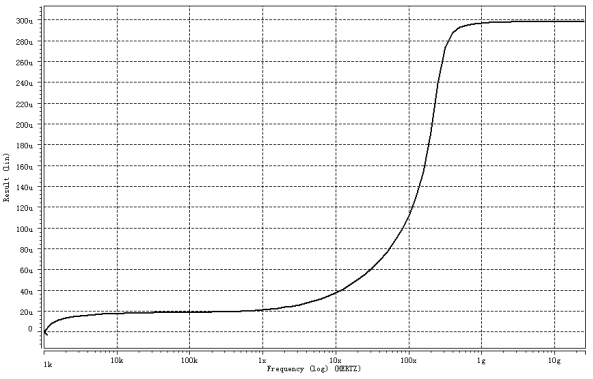
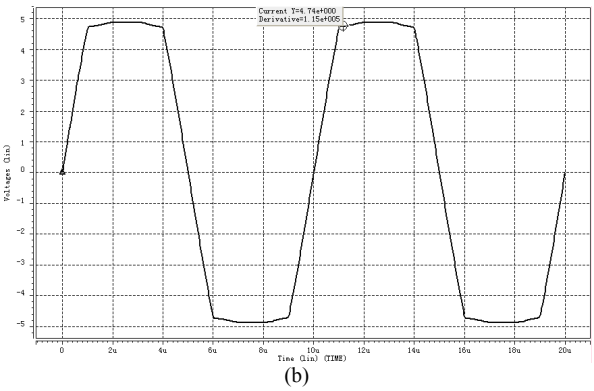


Fig.5. differential AC Open-Loop Gain-Frequency Response

The amplifier has an open-loop AC gain of 86.8dB while the unity-gain bandwidth reaches 966M*Hz* above with an approximate 51 degree phase margin.



(a)



(b)

Fig. 6. (a). Total Integral Output Voltage Noise. (b). Output Swing.

Fig.6 shows the output dynamic range of the op amp. It turns to be with a highest output swing of nearly ±4.75V, much higher than the required specification and it's also the highest value among what have been reported. Thus, the dynamic range is calculated to be 84.4dB.

The general performance of the full custom design CMOS amplifier has been listed in Table IV.

TABLE IV. SUMMARY OF THE OP-AMP RESULTS

Parameter	Simulation Performance	Specification
Differential AC Open-Loop Gain	86.8dB	>81.6dB
Differential AC Open-Loop Unity Gain Bandwidth	966MHz	>829MHz
Phase Margin	~51 degree	——
Dynamic Range	84.4dB	>70dB
Output Swing	±4.75V	>±1.89V
Positive Settling Time to 0.05% Accuracy	13.4ns	<30ns
Power Supply	+5V	+5V

V. CONCLUSIONS

This paper presents the full custom design of a two-stage fully differential amplifier; both the hand calculations and computer-aided simulation results are given in detail. The results show that the designed amplifier has successfully satisfied all of the specifications given in advance. Especially, with the optimal design procedure and specific techniques, the amplifier reaches very large output swing of nearly ±4.75V and fast settling time of 13.4ns to 0.05% accuracy. In addition, the open-loop amplifier also has a considerable gain of as high as 86.8dB and the differential AC loop unity-gain bandwidth of 966MHz. The output swing and unity-gain bandwidth is one of the best performances that have been reported.

REFERENCES

[1] R. Sun and L. Peng, "A gain-enhanced two-stage fully-differential CMOS op amp with high unity-gain bandwidth," in *Proc. IEEE International Symposium on Circuits and Systems*, vol.2, AZ, USA, May 2002, pp. 428–431.

[2] K. Gulati and H.S. Lee, "A high-swing CMOS telescopic operational amplifier," *IEEE Journal of Solid-State Circuits*, vol.33, Issue 12, Dec. 1998, pp. 2010–2019.

[3] W.W. Sue, Z.M. Lin and C.H. Huang, "A high DC-gain folded-cascode CMOS operational amplifier," in *Proc. IEEE Southeastcon '98*, Orlando, FL, USA, Apr. 1998, pp. 176–177.

[4] B. Razavi, *Design of Analog CMOS Integrated Circuits*, New York: McGraw-Hill, 2001.

[5] P.R. Gray, P.J. Hurst, S.H. Lewis and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits,* Forth Edition. John Wiley &Sons, Inc., 2001.

[6] B.J. Hosticka, "Improvement of the Gain of CMOS Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. SC-14, Issue 6, Dec. 1979, pp.1111-1114.

[7] E. Sackinger and W. Guggenbuhl, "A High-Swing, High-Impedance MOS Cascode Circuit," *IEEE Journal of Solid-State Circuits*, vol. 25, Issue 1, Feb. 1990, pp.289-298.