A High Speed Operational Amplifier

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***Abstract*—This paper presents a design of a single stage operational amplifier with a high dc gain and a large unity gain bandwidth. The design was implemented using a folding cascode topology with the addition of gain boosting amplifiers for increased gain. The results show that a gain greater then 75 dB was achieved with unity gain frequency above 1 GHz and a phase margin greater then 65 degrees.**

Index Terms— Phase Margin, Unity gain, Bandwidth, Gain boosting, Cascode, Operational Amplifier

I. INTRODUCTION

HIGH speed high gain amplifiers have many uses in analog circuits which include Sample and Hold circuits, photo-detector amplifiers, fast settling digital to analog converters and buffered amplifiers[1].
The such circuits is becoming more difficult with the trend being toward lower supply voltages and shorter channel lengths. These trends result in trade offs between, gain, speed and output swing. A two stage design is capable of achieving a high gain and large output swing in [2], however, the second stage introduces a pole at a low frequency that affects the frequency response by lowering the unity gain frequency and phase margin .In [3] a single stage telescopic cascode design is described that achieves a higher frequency response and consumes less power than other topologies. The drawback of this architecture is that it severely limits the output swing, hence with a low voltage supply of two volts it is not feasible to pursue this design approach. A folded cascode topology improves on the latter design in that the output swing is increased by one Vdsat [2], while maintaining the same gain at approximately $(gmro)^2$ which is the square of the intrinsic MOS transistor gain. The gain of a folded cascode is maximized at around 50 dB and falling short of the predefined design objectives. An approach to circumvent this problem is presented in [4], where the principle of gain boosting is utilized to increase the dc gain while maintaining a large output swing. This report will show an implementation of the technique described in [4] and present results of the dc, ac and output swing measurements.

II. THEORY OF OPERATION

A. Folded Cascode

The folded cascode topology provides high output swings and is ideally suited to operate in low voltage supply circuits. Figure 1 shows a standard folded cascode single stage amplifier. The maximum output swing that is allowed by this architecture is given by (1).

$$Vos = Vdd - Vod3 - Vod\ 5 - |Vod7| - |Vod9| \quad (1)$$

Vos refers to the output swing and Vod is the overdrive voltage. The small signal gain of the folded cascode architecture is given by (2).

$$Av = Gm*Rout$$

$$= gm1*\ gm3(ro3(ro1||ro5)\ )gm7(ro7ro9) \quad (2)$$

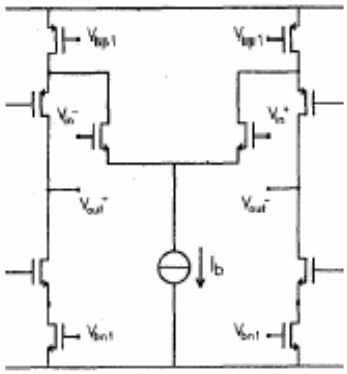

Figure 1. Folded cascode architecture

B. Gain Boosting

In order to achieve a high voltage gain from the folded cascode amplifier the out impedance needs to be maximized. Increasing output impedance requires long channel lengths which add capacitance and slow down the design. One way to circumvent this problem is shown in Figure 2, this particular circuit is called a regulated cascode and the main goal behind it is to further increase the output impedance without increasing the channel lengths. The relationship between the increased impedance and the gain of the gain boosting amplifier is approximately given by (3).

$$Rout \approx Aadd*gm1*ro1*ro2 \quad (3)$$

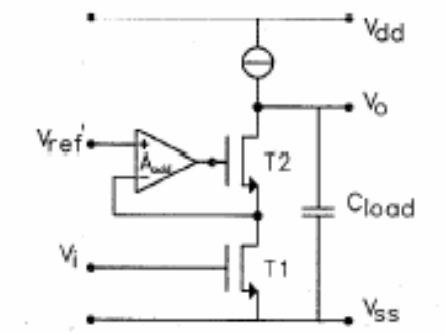

Figure 2. Cascoded gain stage with gain enhancement [4]

In order to ensure that the overall system is stable, unity gain frequency of the gain boosting amplifier needs to be less than the second pole but greater than first pole of the folding cascode amplifier. Figure 3 shows the benefit of implementing the gain boosting technique. Original gain here has bee greatly increased at DC and at no cost of the over all

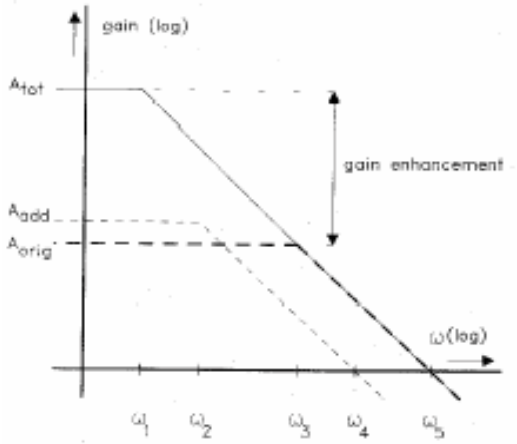

Figure 3. Gain Bode plots of the original cascaded gain stage (Aorig), the additional gain stage (Aadd), and the improved cascaded gain stage (Atot) [4]

unity gain frequency.

III. Design Implementation

A. Input stage

The purpose of the input stage of the amplifier is to receive a differential signal that would then be amplified by a folded cascode topology. The input stage transistors as shown in Figure 4 were designed so as to achieve the desired unity gain frequency (fu) of 1 Ghz. The relationship between the unity gain frequency and the gm (tranconductance) of the input transistors is described by (4), where CL is the load capacitance. The gm of the input transistors is 6.28 mS for a load capacitance of 1pF. The input stage can be implemented using either NMOS or PMOS transistors. The greater mobility of the NMOS devices provides a higher gain, however, this lowers the pole at the folding point [2 p. 304], thereby reducing the phase margin. For this reason PMOS transistors were used for the input stage keeping in mind that the reduction in gain can be compensated by the gain boosting technique. With a tail current of 3.5mA for high gain the W/L ratio was 14.

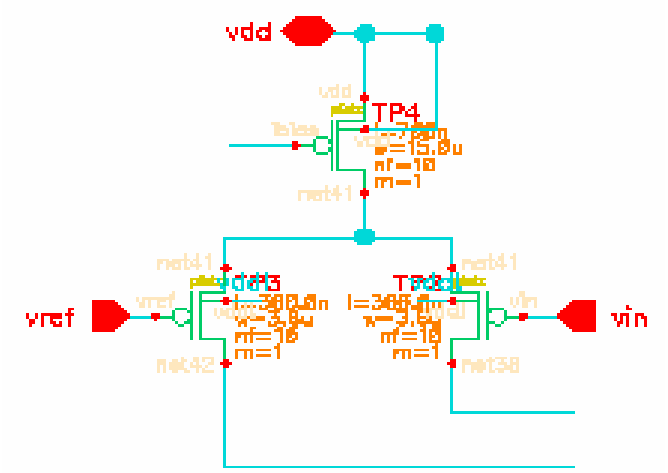

Figure 4. Input stage of folded cascode amplifier. The inputs were selected to be PMOS so as to keep the pole at the folding point farther away

$$Gm1 = CL*fu/(2*pi) \qquad (4)$$

B. Gain and Output stage

The gain stage amplifies the input signal and provides the maximum output swing while maintaining all transistors operating in the saturation region. The folded cascode gain stage with PMOS input transistors is shown in Figure 5. Vb1 and Vb2 were chosen such that the lower part of the swing is equal to Vod3+Vod5, where Vod = Vgs – Vth (overdrive voltage of the transistors). Similarly, the upper part of the swing is given by Vdd - |Vod7| - |Vod9|. Since M5 carries a large current Vod5 was set to 0.4 and all other transistors were set to 0.3. The total calculated output swing is 0.7V. The small signal gain of the folded cascode amplifier is Av ≈ 50dB before gain boosting amplifiers were used.

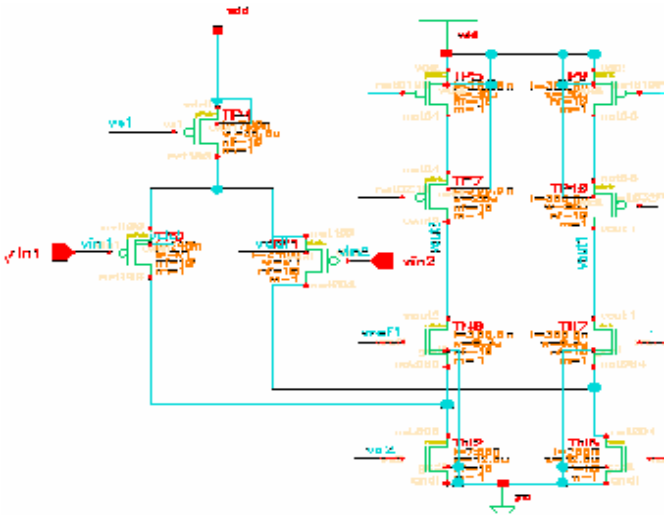

Figure 5. Folded cascode amplifier

C. *Common Mode Feedback (CMFB)*

The purpose of the CMFB is to regulate the common mode output voltage (Vcmo) and maintain at an optimal level. The common mode output voltage level was determined to keep the upper NMOS and PMOS transistor in saturation, which is given by (5).

$$V_{od3} + V_{od5} < V_{cmo} < V_{dd} - |V_{od7}| - |V_{od9}| \quad (5)$$

To allow for maximum output swing, we take a value of 1 volts for Vcmo

Without CMFB the output common mode voltage would fluctuate which in turn causes either the upper or lower transistors to leave the saturation region. The CMFB circuit is shown in Figure 6, it uses NMOS transistors as input devices because Vcmo ≈ 1V which is high to be used with PMOS inputs. This circuit basically senses the output voltages and compares the common mode voltage with Vcmo and any difference is then fed back as a bias voltage to the upper transistors which in turn adjust the current in a direction that achieves the desired common mode output voltage.

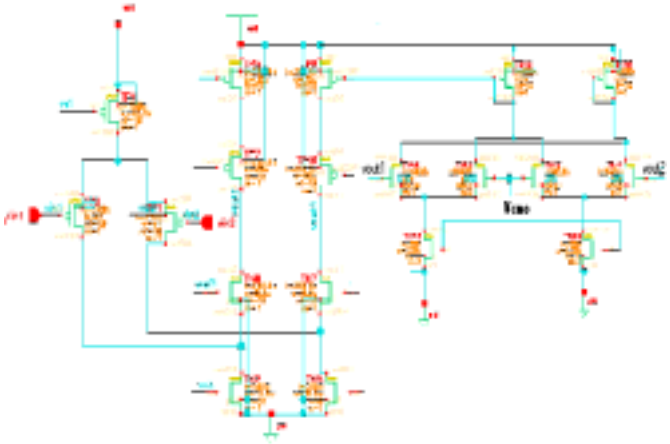

Figure 6. Folded cascode amplifier with common mode feedback.

D. *Gain boosting stage*

The gain boosting stage increases the effective output resistance by the gain of the boosting amplifier, therefore increasing the overall gain of the folded cascode design. Since the gain of the folding cascode architecture is approximately 50 dB then the gain of the gain boosting amplifier is required to be greater than 25dB in order to achieve an overall gain of 75 dB. A differential input single ended output folding cascode topology was used to implement the gain boosting amplifier as shown in Figure 7. The NMOS inputs were used for the upper transistors and PMOS for the lower transistors to get a maximum voltage swing. The gain boosting amplifier utilizes an active current mirror, therefore it does not require the use of common mode feedback. This design achieved a gain of 30 dB for each amplifier.

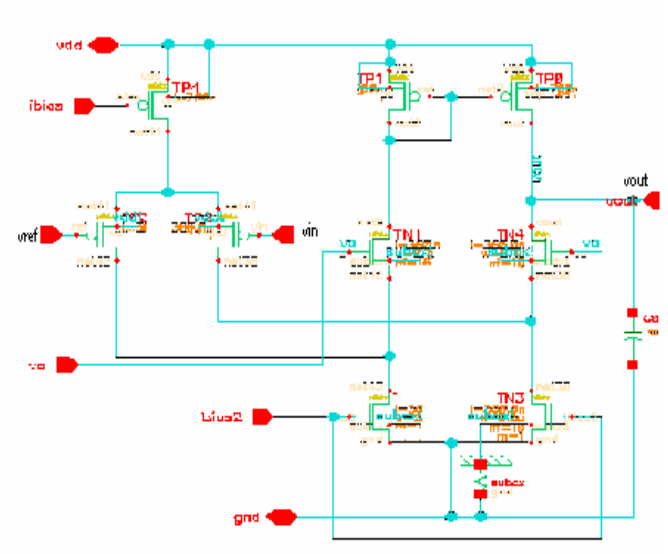

Figure 7. Bottom gain boosting amplifier. This is a single ended folding cascode design with active current mirror.

E. *Compensation*

The amplifier was originally designed with a unity gain frequency greater than 1Ghz so as to leave a margin or error when adding the gain boosting stage and the tempreture variation. The phase of the amplifier w/o gain boosting was designed to be less than 115 degrees at 1 GHz.

In order to achieve the desired phase margin of 65 degrees and a unity gain frequency greater than 1 GHz, capacitors were placed at the output of the gain boosting amplifiers. This will make the 3dB frequency of the gain boosting stage greater than the 3dB frequency of the original gain stage and less than the second pole of the original stage .This is illustrated in Figure 8.

To reduce the overall unity gain of the amplifier to where the phase margin is greater than 65 degrees a capacitor was placed between the differential outputs as shown in Figure (8).

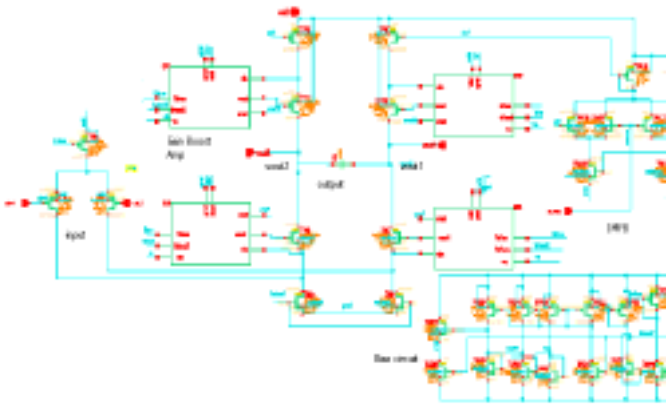

Figure 8. Schematic of the complete design of the amplifier including the compensation capacitor between the differential output voltages.

IV. Measurement and Results

Table 1 summarizes the overall performance of the amplifier with Vdd and temperature variation. The simulation shows that we have excess in gain and phase margin specification. The amplifier consumes power around 28 mW, which needs further reduction.

TABLE I
SUMMARY OF FINAL RESULTS

Temp. ©	Vdd (volts)	Gain (dB)	Phase Margine (degrees)	Power (mW)	Unity Gain (Ghz)
27	2.2	88.2	66	30	1.1
	2	86.6	66	27.1	1.076
	1.8	83.4	66	24.2	1.06
85	2.2	86	65	32	.975
	2	83.9	65	27.2	.971
	1.8	79.7	65	24.3	.97

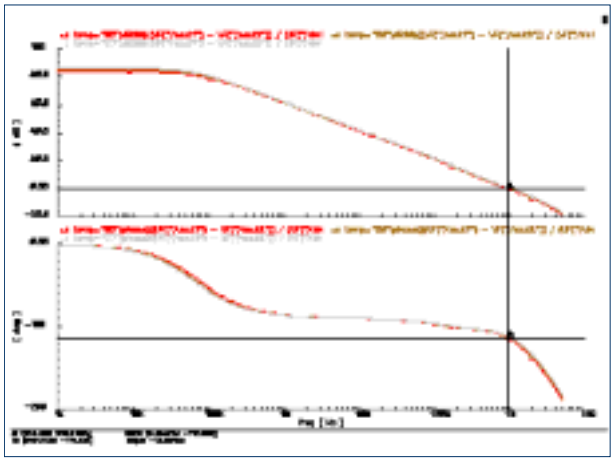

Figure 10. Gain and phase plots with temperature variation.

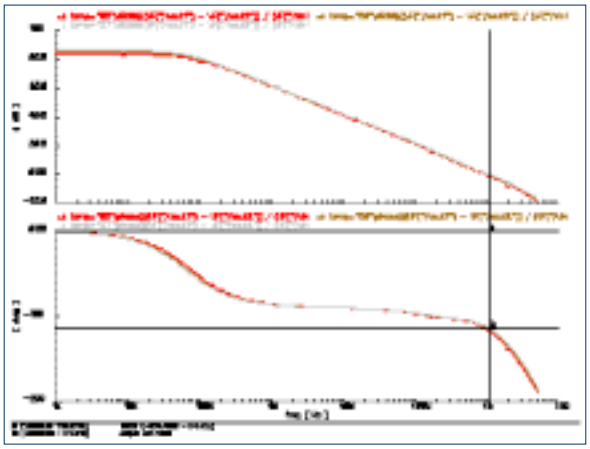

Figure 11. Gain and phase plots with Vdd variation.

Figure 11 and Fig. 12 show the magnitude and the phase of the gain with temperature and Vdd respectively. Fig. 12 shows that Vdd variation has no great effect on the overall performance.

The variation of the input common mode by +/-.3 v has been tested. It has almost no effect on the overall performance.

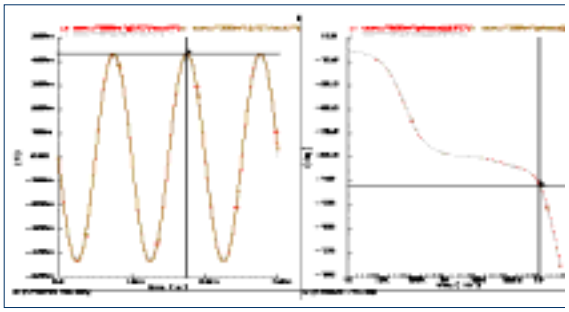

Figure 12. Transient and phase response with input common mode variation +- .3 volts.

Figure 12 shows the output in time domain and the phase of the output at the same time.

Figure 13 shows the voltage swing of the amplifier. The amplifier can give a voltage swing of .8 volts without distorting the output.

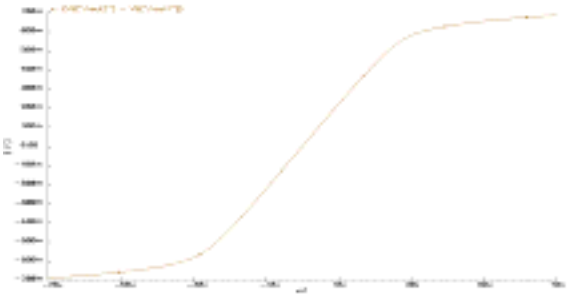

Figure 13. Output voltage swing is fom -0.4V to +0.4V.

Appendix

Our simulation file is stored in the following folder.
afs/engin.umich.edu/class/f03/eecs413/group15/amp34

Acknowledgment

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References

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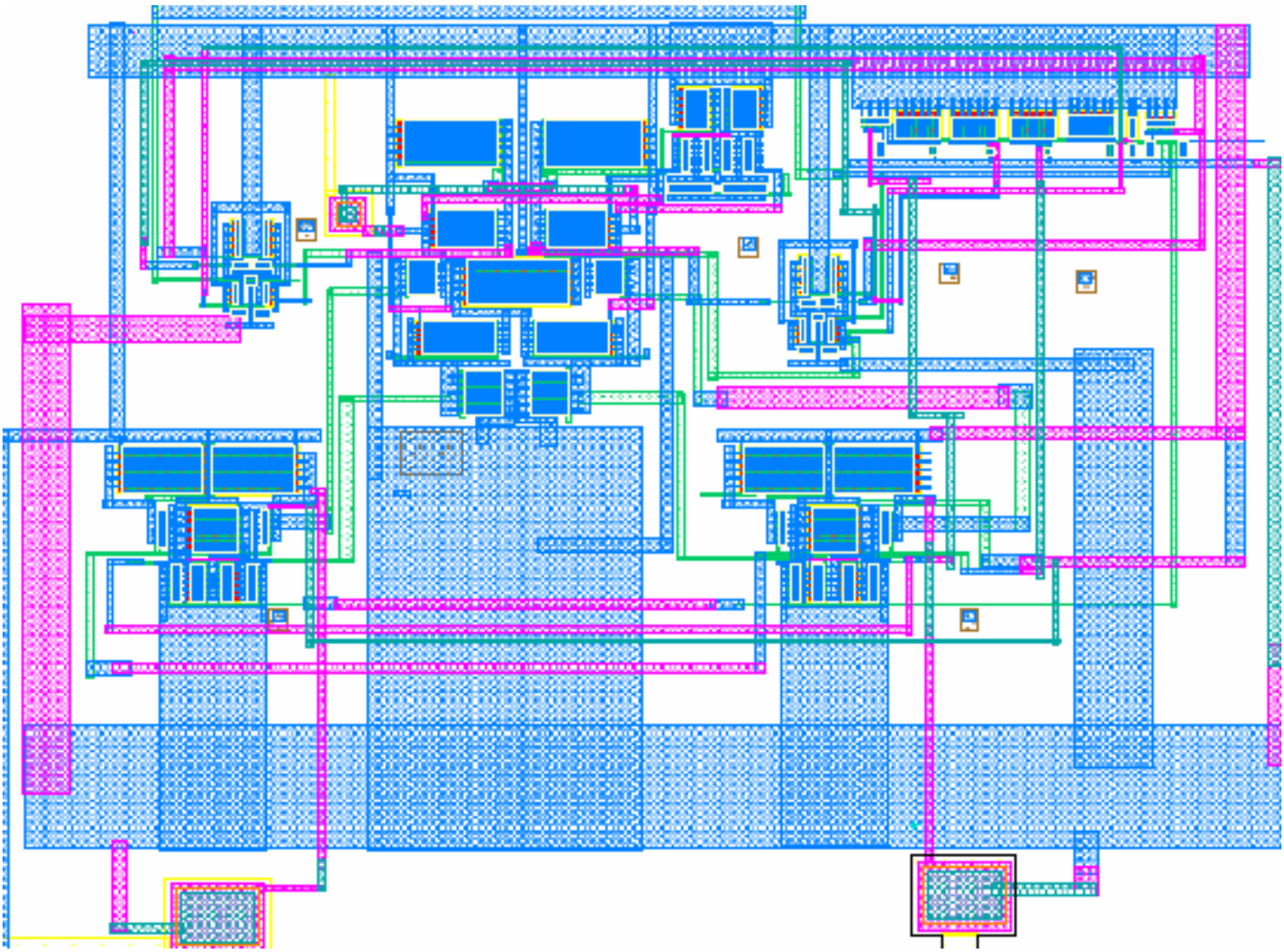

Figure 14. Final layout of the Op-Amp design