HIGH GAIN LOW POWER OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION TECHNIQUES

by

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GRADUATE COMMITTEE APPROVAL

of a dissertation submitted by

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ABSTRACT

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Doctor of Philosophy

This dissertation discusses and compares the existing compensation methods for operational amplifiers. It explores a method to stabilize the op amps without sacrificing bandwidth to the same degree that commonly used methods do. A creative design methodology combining intuition, mathematical analysis, and mixed level simulation is explored for the new compensation scheme. The mixed level approach, associating system level simulation for most circuits along with device level simulation for some critical analog circuit paths, is presented to verify the behavior of new design concepts in an effective way. This approach also provides sufficient accuracy to predict the circuit performance realistically. The new feedforward compensation method overcomes the serious drawback of the widely used pole splitting method, which greatly narrows the bandwidth. It can improve the phase margin as well as optimize the bandwidth of the op amp. The proposed feedforward compensation method can be easily applied to the popular two gain stage op amp architectures with very little alteration.

MOS devices are used in the weak inversion region or the subthreshold inversion region to minimize dc source power. A feasible configuration for high gain, low power op amp design utilizing subthreshold operation along with active operation is proposed. This op amp uses composite cascode connections for the differential input stage, a common source second stage, and a current mirror. A prototype of the op amp was fabricated in a 0.25 μm CMOS process. The proposed op amp produces an open loop gain above one million with low power consumption around 110 μW and shows a favorable slew rate and GBW product compared to other amplifiers driving large capacitive loads. In addition, the composite cascode amplifier requires a compensation capacitor of only 3.5 pF which allows a very small op amp cell. This design is intended for applications where simplicity of layout, small cell size, and low power are important. The open loop gain of this design is comparable to bipolar op amps and exceeds all known reported CMOS designs using the classic Widlar architecture. The fabricated op amp test results show that the BSIM3 model in CADENCE Spectre Spice Simulation matches closely to the experimental results in spite of the low current weak inversion operation of the composite cascode output device and thus provide confidence in the simulation for other similar designs. While facing the challenge of measuring the op amp open loop characteristics at decreased power supply voltages, a few viable techniques were developed to measure the op amp open loop parameters using typically available bench test equipment.

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Chapter 1

Introduction

Operational Amplifiers (Op amps) are one of the most widely used building blocks for analog and mixed-signal systems. They are employed from dc bias applications to high speed amplifiers and filters. General purpose op amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly. Nowadays, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip. While many digital circuits can be adapted to a smaller device level with a smaller power supply, most existing analog circuitry requires considerable change or even a redesign to accomplish the same feat. With transistor length being scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to improve upon.

The classic Widlar op amp architecture, originally developed for bipolar devices, has required modification for use with CMOS devices. In particular, it has proved difficult to match the open loop gain of bipolar op amps with CMOS technology [3, 4]. This is due to the inherently lower transconductance of CMOS devices as well as the gain reduction due to short channel effects that come into play for submicron CMOS processes. As a result, gain boosting schemes have been reported [5, 6] to improve the gain. These gain enhancing methods often require more complicated

circuit structures and higher power supply voltage, and may produce a limited output voltage swing. Multiple stage amplifiers may be used for higher gain analog circuit designs. Nevertheless, multistage amplifiers generally are difficult to compensate. Many compensation schemes for multistage amplifiers have been investigated and reported [3–5, 7]. Techniques similar to those used in general feedback control systems have been adapted to use with electronic amplifiers. These methods include lead-lag networks, pole splitting, nested Miller compensation as well as signal level variable components. However, most compensation methods require more circuit area and more complex design than the dominant pole approach used in the classic op amp architecture. Special problems of integrated circuit amplifiers which include lack of large sized capacitors, parasitic coupling, and package parasitics and on/off chip load problems make the compensation more difficult than discrete component amplifiers.

The most widely used method of compensating integrated circuit op-amps is undoubtedly pole splitting in which the amplifier stage with the smallest bandwidth is further narrow-banded by a compensating capacitor that creates a well-defined dominant pole that sets both open and closed loop bandwidth of the overall amplifier. This method was featured in the original 741/101 bipolar op-amps designed by Robert Widlar and was widely mimicked in later CMOS op amp designs. This method of compensation is in fact so ubiquitous in the integrated circuit industry that most modern textbooks on integrated circuit op amp design do not include discussion of any alternative methods of compensation.

This thesis is concerned with the compensation techniques for operational amplifiers and will explore new and novel methods of achieving compensation in feedback amplifiers that do not limit the bandwidth of closed loop performance to the same degree that commonly used methods do. Specific tools and methodologies will be developed to allow comparison of the new methods with standard methods of compensation. The proposed active feedforward is used to compensate the multistage operational amplifier with good phase margins as well as drastic improvement of the

bandwidth of the amplifier compared to the most widely used pole splitting Miller capacitor compensation approaches.

As mentioned above, the trend for low power applications demands novel op amp architectures. In control and instrumentation applications where high accuracy is required, high gain op amp designs are necessary. Other high-gain CMOS op amps have been investigated in previous work [8–14], but most were unable to achieve gains higher than 100 dB. A few achieved a gain ranging from 120 dB to 130 dB. These CMOS op amp designs use up to 5 cascaded gain stages to achieve the high gain. The highest reported was the simulated 140 dB in [10]. In general, high gain architectures need more complicated compensation to stabilize the op amp and generally require more than one compensation capacitor.

This thesis discusses the design of a high gain, general purpose op amp with the structural simplicity of the classical Widlar architecture. The proposed op amp structure applies composite cascode connections in both the input stage and the second stage to achieve a gain of around 120 dB with low power consumption. The op amp employs the traditional two gain stages followed by a near unity gain buffer stage. This op amp overcomes some limitations of conventional CMOS cascodes by enhancing the gain without using additional bias circuits and requires only a small bias headroom voltage.

Analog circuit design requires a good understanding of how the system and circuit work. Unlike digital circuitry which works with two distinct states, many parameters are under consideration for analog circuits which work with continuous values. Digital circuit design may be quickly validated on a computer with the help of well-developed CAD tools. Due to the multi-dimensional variables of an analog circuit, any slight change in the analog configuration like current, voltage, a transistor parameter, a device model, a manufacturing process, or a modified layout may cause significantly different performance. In general, this low level device modeling makes analog design more complicated and challenging than digital design. For analog design engineers, a good design methodology including intuition, mathematical methods, and

system level simulation combined with device level simulation is essential for creative analog designs. The proposed mixed mode design methodology, which is comprised of mathematical derivation, system level simulation, and device level simulation, will be demonstrated in this thesis.

1.1 Research Contributions

Several original contributions are made and documented in this dissertation. It covers improved frequency compensation for general purpose operational amplifiers and suggests a creative architecture of a high gain low power operational amplifier with composite cascode connections. Moreover, an experimental prototype of the composite cascode op amp has been fabricated in TSMC 0.25μm process to verify the low current design exploiting subthreshold transistor operation along with strong inversion operation. In addition, a mixed mode design method combining the system level and device level simulations for innovative analog circuit design is also suggested. A detailed description of the contributions will appear in the corresponding chapters.

- *Current Compensation Methods Investigation*

Though compensation has been a well-studied topic of analog circuit design for many years, an up-to-date comparison and investigation of modern compensation methods has not been done. This survey summarized some popular compensation methods used in op amps and pointed out their advantages and disadvantages. A guide on how to to use different compensation methods based on the output load and other specifications is given.

- *Feedforward Compensation Method*

This proposed feedforward compensation method is fully compatible with the classical general purpose operational amplifier configuration. This architecture also has the advantage of stabilizing the op amp without reducing the bandwidth as much as most commonly used compensation methods do.

- *System-Level and Combined Device/Transfer Function Simulation Methodology*

A design method which integrates intuition, mathematical derivations, system level simulations, and combined device/transfer function simulations is introduced. The proposed system-level and device-level mixed-mode simulation can give insights of creative thoughts, and simplify the analysis by using ideal blocks for some circuitry while providing necessary device model properties.

• *Stability Analysis of the Feedforward Architecture*

A closed loop stability criteria is derived and a design guideline for maximally flat frequency response is suggested to provide circuit stability. Mathematical derivations along with simulation results are presented to correlate the theory with the implementation.

• *MOSFET in Subthreshold Inversion Used for Low Power Op Amp Designs*

Operating a MOSFET in the weak inversion region or subthreshold region is very useful for low power applications. A wise choice of the quiescent current as well as the proper $\frac{W}{L}$ aspect ratios of the transistors can make some of the devices operate in the strong inversion region while other devices operate in the subthreshold region. A current mirror using the composite cascode connection is also proposed to bias the circuit.

• *Architecture of A High gain Composite Cascode Operational Amplifier*

A two-gain stage op amp which consists of a differential input composite cascode stage operating at a bias current of 3.65 μA and a common source composite cascode second stage provides an open loop gain around 120 dB with 110 μW power consumption. With the high output impedance and the low current of the composite cascode connections, a high gain stage is possible with small chip area and power dissipation. This high impedance load also leads to flexible and simple compensation schemes. A phase margin of 43° is achieved using conventional Miller compensation with a capacitor of only 3.5 pF while driving a 100 pF load. A journal paper on this part of the research has been submitted.

• *Modified Composite Cascode Operational Amplifiers for Different Applications*

The proposed op amp which employs composite cascode connections for both differential input stage and second gain stage along with a source follower output stage could be easily modified to adapt to different operating conditions. The second stage could be implemented with a regular common source stage to increase the bandwidth. The source follower stage could be replaced with a class AB output stage for rail-to-rail output swing.

• *Practical Test Methods of High Gain Op Amps*

As commonly known, it becomes more difficult to measure the op amp characteristics, especially the open loop gain, as power supply voltages continue to decrease. When the multiplication of input referred noise and the open loop gain of the op amp [6, 15] exceeds the power supply voltage, it is difficult to directly test the open loop gain of the op amp. In addition, if the signal magnitude is smaller than the noise magnitude at the input, the output waveform would have little meaning. This work deals with the practical bench test of the open loop gain of the op amp and presents several simple but reliable test methods of op amp open loop gain using typically available bench test equipment.

1.2 Dissertation Outline

The research presented in this dissertation covers studies related to the frequency compensation methods of operational amplifiers, gain boosting schemes of operational amplifier design, and low voltage low power analog circuit design. Each chapter presents the analysis of the problem and the development of solutions. A brief outline of each chapter is described below.

Chapter 2 covers the general background information for frequency compensation. The basics of the feedback control stability theory associated with negative feedback amplifiers are reviewed. Other existing frequency compensation methods are discussed with their suitability for different circumstances.

Chapter 3 proposes an active feedforward compensation technique to overcome the bandwidth reduction resulting from commonly used compensation methods like

pole splitting. The guidelines of the compensation method are derived through a stability analysis. A mixed mode design methodology is applied to analyze the compensation approach. The design methodology integrates intuition and mathematical analysis along with the system/device level simulation.

In Chapter 4, three different inversion regions of MOSFET operation are reviewed and different op amp gain boosting techniques are introduced. Besides multistage amplifiers with more than three gain stages, conventional cascode, folded cascode, and enhanced impedance methods are investigated along with their advantages and limits. The limit of low voltage analog design is discussed with a few possible low voltage design techniques.

In Chapter 5, the high gain lower power operational amplifier with composite cascode connection is proposed. The subthreshold operation of the MOSFET is emphasized in the composite cascode application. The hardware implementation of the op amp prototype is demonstrated. Measured results are presented along with the simulation results to demonstrate the performance of this op amp design. The variations of the operational amplifier architecture for different circumstances are also discussed in this chapter.

Chapter 6 addresses the issues of testing and characterizing the high gain low voltage op amps. The challenge of measuring the gain of high gain op amps increases as the power supply voltages decrease. Several simple bench test methods are investigated and proposed to characterize the op amp characteristics, in particular the open loop gain. These practical techniques do not require sophisticated instrumentation or complicated lab setup. The setup of the test and the debugging of the practical problems encountered in test are presented.

Lastly, Chapter 7 contains a summary of the research presented. Contributions are enumerated again and possible directions of future research are discussed.

Chapter 2

Frequency Compensation Techniques

2.1 Introduction

In general, operational amplifiers are amplifiers with an open loop gain high enough to ensure the closed loop transfer characteristic with negative feedback is approximately independent of the op amp gain. An adequately high gain is the key requirement of an op amp to utilize the negative feedback configuration.

2.2 Feedback Circuit Theory

Fig. 2.1 shows a general negative feedback system, where A is the forward gain network and F is the feedback network from the output back to the input terminal. The feedback signal V_f(s), which is equal to F(s)V_o(s), is subtracted from the source signal V_i(s) to generate the feedback error signal V_e(s), which is the input to A. That is

$$V_e(s) = V_i(s) - F(s)V_o(s). \tag{2.1}$$

Thus,

$$V_o(s) = A(s)(V_i(s) - F(s)V_o(s)) \tag{2.2}$$

$$\tag{2.3}$$

and

$$G(s) \equiv \frac{V_o(s)}{V_i(s)} = \frac{A(s)}{1 + A(s)F(s)}. \tag{2.4}$$

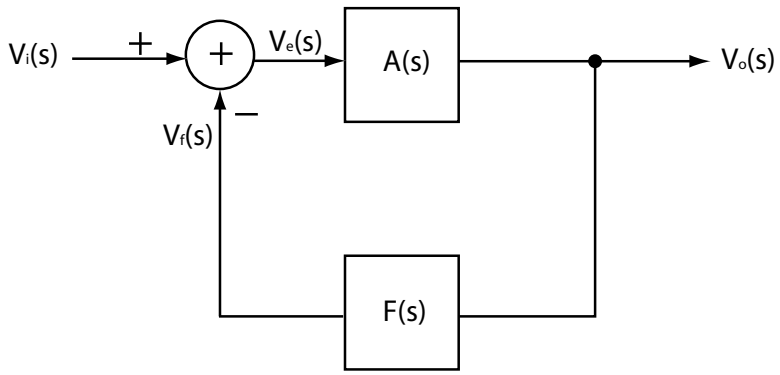


Figure 2.1: General negative feedback system

The quantity A(s)F(s) is called the loop gain and is equivalent to the transmission around the feedback loop. As represented by the configuration of a feedback amplifier in Fig. 2.1, A(s) is usually the open loop transfer function and G(s) is the closed loop transfer function. If the loop gain is very high, G(s) is mainly controlled by the feedback network F(s) since $G(s) \approx \frac{1}{F(s)}$ when $A(s)F(s) \gg 1$.

The negative feedback decreases the gain, but it provides a few other benefits such as gain desensitivity, bandwidth extension, impedance modification, and nonlinearity reduction. A sensitivity factor is defined in terms of the differential change of a dependent variable divided by the differential change of an independent variable. Assume G is a function of A, the sensitivity of G relative to A is

$$S_A^G = \frac{\frac{\partial G}{G}}{\frac{\partial A}{A}} = \frac{A}{G}\frac{\partial G}{\partial A}. \tag{2.5}$$

The sensitivity of G in Eq. (2.4) following Eq. (2.5) is derived as

$$S_A^G = \frac{1}{1+AF}. \tag{2.6}$$

In the open loop situation, the sensitivity S_A^G is one since there is no feedback and F equals zero. It is clear that negative feedback reduces the sensitivity of the feedback amplifier to the variations of the amplifier gain A by the factor 1+AF. The overall gain becomes very stable as 1+AF approaches large values.

The sensitivity of G with respect to the changes in the feedback factor F is

$$S_F^G = -\frac{AF}{1+AF} \approx -1. \tag{2.7}$$

The sensitivity S_F^G is less advantageous compared to S_A^G since S_F^G approaches minus one. This result is straightforward since the overall gain is mainly determined by F. To improve the behavior of the system, the feedback network F must be less sensitive to device parameters than the amplifier A. Fortunately, this is the case for most circumstances since the feedback network F usually consists of stable passive devices rather than the active devices of the amplifying element.

Certain configurations of feedback amplifier extend the bandwidth over the open loop amplifier. Assume the amplifier A has a one pole transfer function

$$A(s) = \frac{A_0}{1+s/p_0}, \tag{2.8}$$

where A_0 is the midband gain of the amplifier and p_0 is the 3-dB bandwidth. Applying Eq. (2.4), the closed loop gain is found to be

$$G(s) = \frac{\frac{A_0}{1+s/p_0}}{1+\frac{A_0F}{1+s/p_0}} \tag{2.9}$$

$$= \frac{\frac{A_0}{1+A_0F}}{1+\frac{s}{(1+A_0F)p_0}}. \tag{2.10}$$

The 3-dB bandwidth is increased from p_0 to $(1 + A_0F)p_0$ at the cost of a proportional reduction in the gain. Eq. (2.10) implies that the gain-bandwidth product of a one pole system is a constant with feedback, which allows gain and bandwidth to trade off directly by feedback.

Feedback also changes the circuit input and output terminal impedances. With voltage or current quantities as output signals, the feedback networks used to sense the output signal are defined as voltage (shunt) or current (series) connections at the output respectively. With voltage or current quantities provided at the summing terminal, the connections are defined as voltage (series) or current (shunt) types at the input. The voltage (shunt) feedback at the output decreases the output impedance while the current (series) feedback at the output enhances the output impedance. On the other hand, the input impedance to the voltage (series) feedback amplifier is raised while the current (shunt) feedback at the input decreases the input impedance. In conclusion, series feedback increases the impedance while shunt feedback decreases the impedance for both the input and output terminals. Different feedback circuits could be chosen if higher or lower impedance is desired.

Another important effect of a negative feedback system is the reduction of the nonlinearity in analog circuits. There is always nonlinear distortion of the circuits because of the nonlinear amplifying devices. When the nonlinearity is small, the input-output transfer curve is approximately linear. But for large signal swings, the output shows a distorted shape. The change of the small signal gain with the input dc level demonstrates the nonlinear property of the amplifier circuit. The static nonlinearity is denoted as the maximum deviation of the curve from the ideal straight line

$$\%\ nonlinearity = \frac{\Delta V_{max}}{V_{out,max} - V_{out,min}}. \tag{2.11}$$

Where $V_{out,max}$ represents the maximum value of the output signal, $V_{out,min}$ means the minimum value of the output signal, and V_{max} is the maximum difference between the actual output curve and the straight line drawn from $V_{out,min}$ to $V_{out,max}$.

We can express the nonlinear transfer function $V_o = f(V_i)$ by a Taylor series expansion about the quiescent point $V_{oQ} = f(V_{iQ})$ as

$$\begin{aligned} V_o &= V_{oQ} + (V_i - V_{iQ}) \cdot \frac{dV_o}{dV_i}\Big|_{V_i=V_{iQ}} + \frac{(V_i - V_{iQ})^2}{2!} \cdot \frac{d^2V_o}{dV_i^2}\Big|_{V_i=V_{iQ}} + \cdots \quad (2.12) \\ &= V_{oQ} + a_1(V_i - V_{iQ}) + a_2(V_i - V_{iQ})^2 + \cdots . \quad (2.13) \end{aligned}$$

Applying a single sinusoidal input around the quiescent point (V_{iQ}) to the nonlinear circuit induces an output spectrum consisting of the input fundamental frequency as well as higher order harmonics. Assuming $V_i = V_{iQ} + v_i cos(\omega t)$ and applying Eq. (2.13) gives

$$\begin{aligned} V_o - V_{oQ} &= a_1 v_i cos(\omega t) + a_2 {v_i}^2 \frac{1 + cos(2\omega t)}{2} \quad (2.14) \\ &\quad + a_3 {v_i}^3 \frac{3cos(\omega t) + cos(3\omega t)}{4} + \cdots \end{aligned}$$

and

$$\begin{aligned} V_o - V_{oQ} &= (\frac{1}{2} a_2 {v_i}^2 + \cdots) \quad (2.15) \\ &\quad + (a_1 v_i + \frac{3}{4} a_3 {v_i}^3 + \cdots) cos(\omega t) \\ &\quad + (\frac{1}{2} a_2 {v_i}^2 + \cdots) cos(2\omega t) \\ &\quad + (\frac{1}{4} a_3 {v_i}^3 + \cdots) cos(3\omega t) + \cdots . \end{aligned}$$

Eq. (2.16) can be rewritten in a simplified form

$$V_o - V_{oQ} = A_0 + A_1 cos(\omega t) + A_2 cos(2\omega t) + A_3 cos(3\omega t) \cdots , \quad (2.16)$$

where the term A_0 shows a dc part introduced to the output signal by the even order harmonics due to nonlinearity and represents the shift from the ideal quiescent output V_{oQ}. A_2, A_3, $\cdots$ represent the amplitudes of higher order harmonic components generated by the nonlinear transfer characteristic. This property is called "harmonic

distortion" and this dynamic nonlinearity can be expressed by "total harmonic distortion" (THD) in the following form

$$THD = 10\log\frac{power\ in\ harmonics}{power\ in\ fundamentals} \quad (2.17)$$

$$= 10\log\frac{A_2^2 + A_3^2 + \cdots}{A_1^2}. \quad (2.18)$$

Harmonic distortion is undesirable in most applications. A THD of about 0.01% (-80 dB) is essential for high quality audio products and a THD around 0.1% (-60 dB) is necessary for video products.

As mentioned, nonlinearity can be regarded as the variation of the small signal gain with the input dc level. Negative feedback keeps the overall closed loop gain nearly constant and almost independent of the amplifier open loop gain. This means that negative feedback reduces distortion resulting from the change in the slope of the amplifier transfer curve. Mathematical analysis of the effect of a feedback system on the nonlinearity of a circuit is very complex and can be found in [16, 17]. The second order harmonic typically causes more distortion than the other harmonics and it is one of the reasons that the input differential stage is popularly used in order to get rid of the even harmonics.

2.3 Stability of Feedback Systems

Negative feedback is widely used due to the properties discussed in the preceding section, such as gain desensitization, bandwidth extension, impedance modification, and nonlinearity reduction. Nonetheless, the negative feedback on the frequency response of a circuit may lead to instability. The feedback circuit may oscillate.

The closed loop transfer function of the feedback system shown in Fig. 2.1 is expressed as Eq. (2.4). If F(s) is independent of frequency, it can be simplified as F. Eq. (2.4) can now be expressed as

$$G(s) = \frac{A(s)}{1 + FA(s)}. \quad (2.19)$$

If $\text{FA(s)}|_{(s=j\omega_1)} = -1$, the overall gain approaches infinity. In this case, the system is not stable since any small noise will be amplified till the circuit starts to oscillate even without the presence of an input signal. This unstable condition called "Barkhausen's Criteria" is expressed as

$$|FA(j\omega_1)| = 1 \tag{2.20}$$

and

$$\angle FA(j\omega_1) = -180^\circ. \tag{2.21}$$

When $\angle FA(j\omega_1) = -180^\circ$, the total phase shift at the inverting input is 0° or 360° since the negative feedback already provides 180° phase shift. This means that the original negative feedback at low frequency becomes positive feedback at some higher frequency ω_1. In this situation, if the loop gain at this frequency is greater than unity, the signal will be amplified to cause oscillation.

The necessary and sufficient requirement for a feedback system to be stable is that all the poles of the overall closed loop transfer function have negative real parts. On the Laplace plane, this demonstrates that all the poles of the system are in the left half plane. It may be difficult to analyze the stability of a complex system from the closed loop poles since finding the zeros of the denominator 1+FA(s) of the overall transfer function is complicated. It is more straightforward if we can predict the closed loop stability from the open loop frequency response since the poles of the open loop transfer function are usually known.

The Nyquist criterion is applied to determine the stability of the feedback system. The Nyquist diagram is a plot which shows the change of the loop gain FA(s) in magnitude and phase with respect to frequency ω on a polar plot. If all the poles of the loop gain are in the left half plane, a feedback system is unstable if the Nyquist plot of the loop gain encircles the point $(-1,\ 0)$. It is clear that Barkhausen's criteria is a simpler version of the Nyquist criterion.

Measuring the phase margin (PM) of the open loop gain response is a good quantitative way to express the degree of the stability of a feedback circuit. As shown in Fig. 2.2, the phase margin is specified as 180° plus the actual phase shift at the unity gain frequency ω_t where $|FA(j\omega_t)| = 1$. The PM must be greater than 0° for no oscillation to occur. Gain margin (GM) is defined as the gain difference between the cross over frequency and the phase crossover frequency at which the phase reaches $-180°$. Both phase margin and gain margin are effective in predicting the stability of a feedback circuit. In the later sections, it is seen that the phase margin is one of the guidelines for designing and compensating operational amplifiers.

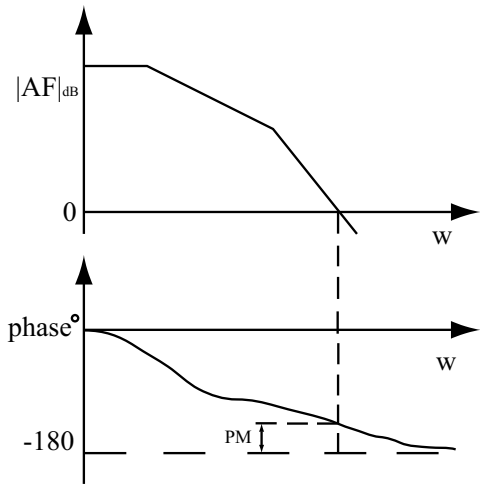


Figure 2.2: Phase Margin Plot

Root-Locus is one methodology used to judge the feedback amplifier stability and guide the compensation using frequency domain responses. Root-locus is the locus of poles traced by a feedback system as the constant part of the loop gain varies from zero to infinity. This technique involves the movements of the poles and zeros of the feedback amplifier in the s plane with respect to the variation of the loop gain. Rules have been established [15] to outline the root locus without complicated calculation of the positions of the poles.

2.4 Basic Frequency Compensation Techniques of Operational Amplifiers

The single stage amplifier typically has good frequency response and could achieve a phase margin of 90° assuming the gain bandwidth is ten times higher than the single pole. However, the dc gain of the single amplifier is generally not high enough and is even less for submicron CMOS transistors. In general, op amps require at least two gain stages. As a result, op amp circuits have multiple poles. The poles contribute to the negative phase shift and may cause $\angle FA$ to reach $-180°$ before the unity gain frequency. The circuit will then oscillate due to the negative phase margin. It leads to the necessity of altering the amplifier circuit to increase the phase margin and stabilize the closed loop circuit. This process is called "compensation". By intuition, two different approaches may be taken to stabilize the circuit. The most straightforward way is to make the gain drop faster in order for the phase shift to be less than $-180°$ at the unity gain frequency. This method achieves stability by reducing the bandwidth of the amplifier. The most popular pole splitting method uses this procedure. Another compensation method pushes the phase crossover frequency out by decreasing the total phase shift. In this case, the number of the poles of the op amp needs to be minimized while still providing enough gain. Pushing the phase crossover frequency out is the basic idea of approaches like introducing zeros to cancel the poles or using feedforward paths to improve the phase margin without narrow-banding the bandwidth as much as the pole splitting method does. As shown in later sections and chapters, the feedforward method modifies the open loop transfer function or the closed loop transfer function to increase the phase margin.

2.4.1 Parallel Compensation

Parallel compensation is a classical way to compensate the op amp. A capacitor is connected in parallel to the output resistance of a gain stage of the operational amplifier to modify the pole. It is not commonly used in the integrated circuit due to the large capacitance value required to compensate the op amp, which costs considerable die area.

2.4.2 Pole Splitting - Single Miller Compensation (SMC)

Early in 1967, Widlar designed the LM101/741 [18] op amp which employed the pole splitting frequency compensation method. This method was first used in Bipolar architecture and widely imitated in later CMOS op amp designs. It is covered in many articles and textbooks [15,19]. In 1974, Solomon reported a tutorial study on the monolithic op amp [20] and discussed the pole splitting technique. By putting a compensation capacitor between the input and output nodes of the second inverting stage of the op amp, the dominant pole is created due to Miller [15,21] feedback. This method maintains a high midband gain for the op amp since the capacitor does not affect the dc response of the amplifier. Fig. 2.3 shows the standard SMC topology.

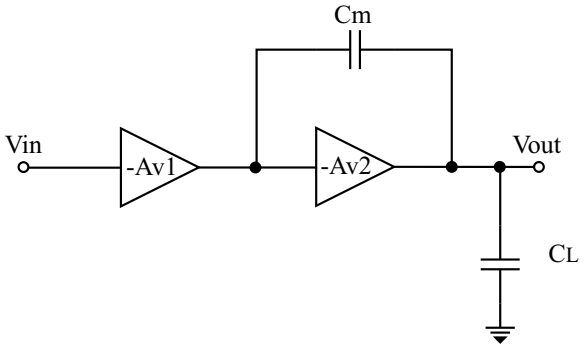


Figure 2.3: SMC

As the transistor gain of the second stage increases, the dominant pole decreases and the nondominant pole increases. In this way the two poles are being split apart and stabilize the feedback amplifiers by greatly narrowing the bandwidth. This simple pole splitting method also introduces a right half plane zero which causes negative phase shift, as a result, the stability is made a little poorer. The zero comes from the direct feedthrough of the input to the output through the Miller capacitor. To eliminate the RHP zero due to the feedthrough and increase the phase margin of the op amp, lead compensation which adds a nulling resistor in series with the compensation capacitor (SMCNR) to increase the impedance of the feedthrough path is

reported [4, 15]. Leung and Mok [22] investigated the effect of the nulling resistor to the positions of the poles as well as that of the zero and pointed out the pole splitting would break down if the resistor becomes too big. When the resistor gets very large, there is no pole splitting since the compensation capacitor is actually open circuit. Fig. 2.4 shows the popular SMCNR structure.

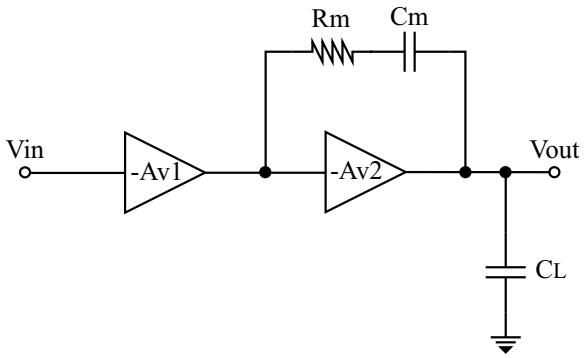


Figure 2.4: SMCNR

2.5 Other Multistage Operational Amplifier Compensation Techniques

Many gain boosting schemes have been reported [5] to improve the gain. In general, these gain enhancing designs require more complicated circuit structure and a larger power supply voltage, but generate smaller output swing. As a result, multiple stage amplifiers might be more suitable for low power, low voltage, high density analog circuit designs. The frequency response of the multistage amplifier is not as good as that of the single stage and this amplifier has a higher probability of oscillation in feedback circuits. One popular way to predict the closed loop stability is by measuring the phase margin of the open loop gain response. PM must be greater than 0° for no oscillation to occur. A good performing amplifier will need a PM of about 45° to 60°. Otherwise, the amplifier may exhibit ringing in the time domain and peaking in the frequency domain [15, 23].

2.5.1 Nested Miller Compensation (NMC) and the Variants

Multistage amplifiers have more poles and zeros than do single stage amplifiers. The frequency response and time response are far more complicated than those of the single stage op amps. As a result, all multistage amplifiers suffer closed loop stability problems. Single Miller compensation is used for the simple two-stage amplifier; while the extended version of the SMC compensation, nested Miller compensation (NMC) [15, 22, 24] is applied to amplifiers with three or more stages. Because of the rapid bandwidth reduction, op amps with more than four stages are rarely investigated. NMC exploits the nested structure of feedback capacitors to cause the pole splitting compensation. There are some drawbacks related to the NMC approach. The total of N-1 nested compensation capacitors must be placed between the dominant node and the other nodes to split the individual poles from the dominant output pole to stabilize an N stage op amp. Fig. 2.5 shows the structure of a three stage NMC op amp. The nesting topology of the compensation capacitor reduces the bandwidth substantially [5, 24, 25]. The specific configuration requires the compound noninverting gain stages to connect to the inverting output stage in order to secure negative feedback for the nested compensation loops. The necessity to drive the compensation capacitors along with the capacitive load requires the output stage to have a high transconductance to attain wide bandwidth and high slew rate. Consequently, elevated power consumption is unavoidable especially for large load capacitor.

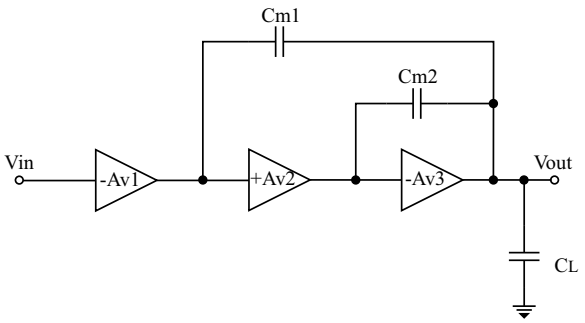


Figure 2.5: NMC

To address the bandwidth degradation problem, the variations of the NMC are developed. NMC using nulling resistor (NMCNR) [4, 15], reversed nested Miller compensation (RNMC) [19], multipath NMC (MNMC) [5, 22, 24, 26], hybrid NMC (HNMC) [5], nested Gm-C compensation (NGCC) [27] have been presented.

RNMC improves the bandwidth over NMC by the reversed compensation topology compared to NMC as shown in Fig. 2.6.

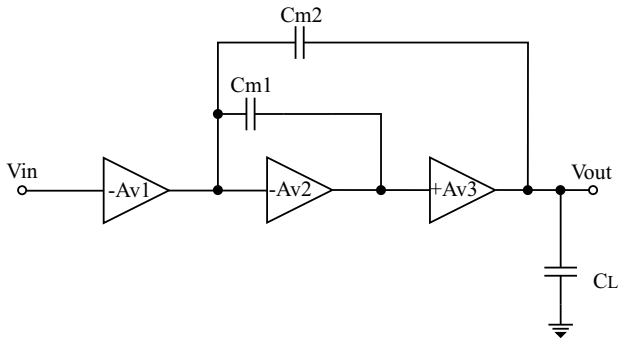


Figure 2.6: RNMC

The RNMC technique sets the second gain stage negative and the output stage positive. The Miller capacitor loop is around the second stage without connection to the considerable output capacitive load. HNMC combines the NMC and the RNMC topological properties in a multistage (above three) op amp. In this circumstance, the circuit could consist of only inverting amplifier except for the input stage.

The difference between NMC and MNMC is the added feedforward amplifier stage -Af1 connected between the input of the first stage and the input of the last stage of the multistage op amp as shown in Fig. 2.7. The feedforward stage added can produce a LHP zero to counteract the second nondominant pole to broaden the bandwidth. The increased circuit complexity and power consumption should be considered. Moreover, the pole zero doublets may seriously degrade the settling time of the amplifier [28].

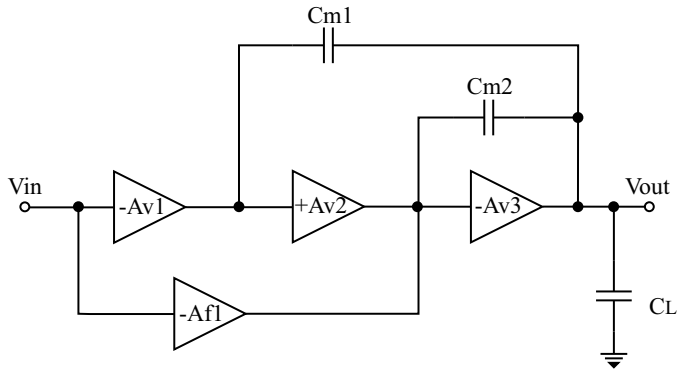


Figure 2.7: MNMC

The difference between NGCC and MNMC is that NGCC replicates the feedforward G_m N-1 times for an N stage op amp recursively as shown in Fig. 2.8 . Compared to MNC, NGCC has simpler stability conditions due to the much simpler transfer function which makes the op amp design more facile.

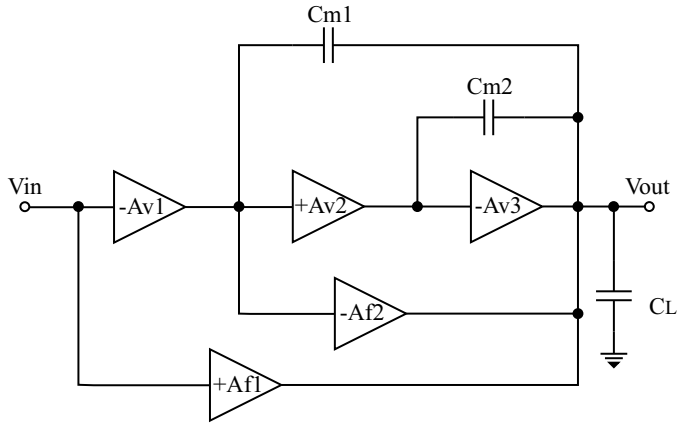


Figure 2.8: NGCC

The basic idea of most of these variations of the NMC schemes is not to drop the overall bandwidth of the multistage amplifiers by the pole zero cancellation in the passband caused by the feedforward path of the multipath topology. All of those compensation techniques mentioned above use Miller capacitors whose sizes are related to the load capacitor value. The required sizes of the compensation capacitors

would escalate with larger capacitive loads which make these techniques not suitable for low area need. The experimental results of the varied versions of NMC showed that the bandwidth does not get improved significantly for considerable capacitive loads [19, 22].

2.5.2 Single Miller FeedForward Compensation (SMFFC)

Many compensation techniques mentioned above are not suitable for large load capacitors. The demand for lower power consumption, lower chip integration area, capability for driving large capacitive loads, and stable high gain bandwidth of amplifiers calls for improved frequency compensation patterns. The topologies using a single Miller capacitor in three stage amplifiers could greatly reduce the needed sizes of the compensation capacitors compared to NMC related schemes and result in amplifiers with smaller chip area. The presented SMFFC and the modified SMC with the additional feedforward path from the output of the first stage to the output load stage [27] are designed for a particular three stage amplifier specifically in the case of large capacitive loads. The topology of the SMFFC op amp is represented in Fig. 2.9. Instead of using pole zero cancellation, SMC with one forward path adopts the separate pole approach [22] for compensation in the situation of large capacitive loads. SMFFC employs two forward paths and provide a LHP zero to compensate the first nondominant pole to alleviate the bandwidth reduction and improve the phase margin. The strictly rational selection of gains among the three stages is the key point for this SMFFC scheme. For the gain distribution like $A_{v1} \gg A_{v2} \geq A_{v3}$, the second and third poles of the amplifier would be placed at higher frequencies that lead to a coarse single pole system for an easier frequency compensation strategy. The appropriate selection of the moderate gain of the second stage will then decrease the compensation capacitor size. Unfortunately, this method does not truly resolve the compressed gain bandwidth issue due to the super high gain of the first stage and the nature of the pole separation. Gain enhanced feedforward path compensation

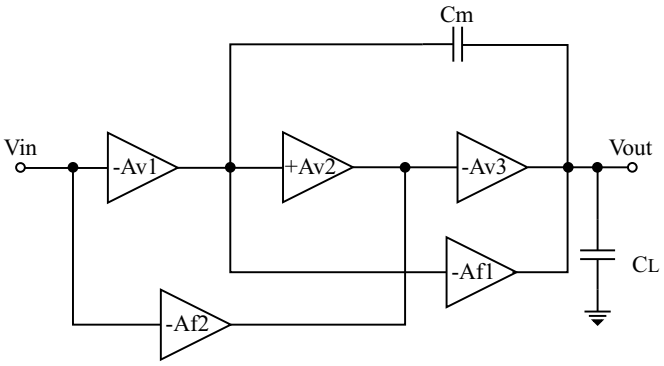


Figure 2.9: SMFFC

(GFPC) [29] is much like the modified SMC version with one feedforward path, but for two stage amplifiers.

2.5.3 Nonstandard NMC Schemes

The nonstandard NMC topologies have been investigated to deal with the drawbacks with the NMC and MNMC in order to be able to drive large capacitive loads. The reported strategies include damping factor control frequency compensation (DFCFC) [30], embedded RC compensation (ERC) [25], active feedback frequency compensation (AFFC) [31], and dual loop parallel compensation (DLPC) [32, 33]. The ERC duplicates the RC compensation process N-2 times for an N stage op amp. ERC compensation circuits do not load the output stage as NGCC circuit do. The noninverting gain stages are not necessary in ERC as in NMC or the standard variations of NMC. ERC topology extends the bandwidth via the zero pole cancellation through the embedded compensation network without connection to the output load. Usually ERC uses a low gain, high conductance output stage to have the similar loading isolation benefit as the buffer output stage of the Widlar architecture. DFCFC can substantially improve the bandwidth of a three stage amplifier with good frequency and transient responses when driving large capacitive loads. But it is not so effective for small capacitive load applications. Some other compensation methods turn out to be more suitable than DFCFC when driving a small capacitive load.

2.5.4 No Capacitor Feed Forward (NCFF)

One feedforward compensation scheme for multistage operational transconductance amplifiers with no Miller capacitors is proposed by Thandri and Silva-Martinez [34]. This NCFF method applies the feedforward path as shown in Fig. 2.10 to create LHP zeros. By using the positive phase shift of LHP zeros to cancel the negative phase shift of the poles, a high gain, high bandwidth amplifier with a good phase margin is developed. Thandri does mention some design considerations of the NCFF in the paper. For example, the feedforward and second stage must place the nondominant poles after the overall unity gain frequency of the amplifier to alleviate phase deduction; the pole zero cancellation should happen at high frequencies to achieve better time domain response. Some other constraints of the NCFF scheme not directly specified in the paper should also be recognized. The NCFF is not suitable for big capacitive loads as a result of the main design consideration mentioned. The transient response might be degraded severely by the pole-zero doublets [28]. A good performing amplifier should have both good frequency response and transient response. The complexity of the presence of extra poles and zeros can cause the design of the NCFF scheme to be very difficult and the undesired low frequency pole-zero doublets may lengthen the settling time of the amplifier or even make the closed loop unstable.

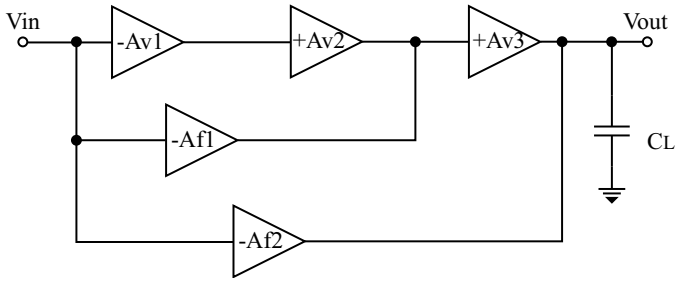


Figure 2.10: NCFF

2.5.5 Negative Miller Capacitance Compensation (NMCC)

The negative Miller capacitance compensates high speed CMOS op amps [35] that consists of an operational transconductance amplifier (OTA) and a buffer. The buffer with a dc gain of A is used to detach the OTA from the load. The OTA is compensated with a capacitor C_c connected between the input and output of the buffer. Assuming the op amp drives a load with a parallel combination of a resistor R_L and a capacitor C_L, the effective capacitance seen at the input of the buffer is $C_{in} = C_c(1-A)$ and $C_{out} = C_L + C_c(1-\frac{1}{A})$ at the output of the buffer. Since the gain of the buffer is positive and smaller than one, the reflected Miller capacitor $C_c(1-\frac{1}{A})$ at the output will be negative. The total effective output capacitance is reduced to be smaller than the original load capacitance due to the negative Miller capacitance. NMCC can be applied to drive a large capacitive load. The experimental results show that the NMCC design shifts the first nondominant pole to a higher frequency while keeping the position of the dominant pole almost the same. This NMCC scheme could increase both the bandwidth and phase margin.

Comer et al. [36] proposed a CMOS amplifier bandwidth extension method by utilizing a negative capacitance circuit. Negative capacitance can be generated by active circuitry using the Miller effect. The limitations of current IC technologies restrain the use of inductors and only small capacitors are available. With the innovative negative capacitor idea, compensation practice could shape the frequency response with more freedom.

2.6 Conclusion

This chapter introduces the background of feedback systems and the frequency compensation techniques for feedback operational amplifiers. To stabilize op amps, the common techniques are pole splitting and pole zero cancellation using a capacitor and resistor [3, 7]. This section discusses and compares the existing methods of achieving compensation for multistage amplifiers. It points out the advantages and disadvantages of the different compensation topologies in order to help the op amp

designers better understand and choose the appropriate structure for different circumstances. Some previous solutions are shown to illustrate the design issues related to the respective compensation configuration and to provide the necessary background.

Chapter 3

Creative Feedforward Op amp Compensation Design

3.1 Introduction

The operational amplifier is probably the most popular building block in analog circuits. As mentioned in chapter 2, the conventional pole splitting method [20] puts a compensation capacitor between the input and output nodes of the second inverting stage of the op amp to break away the two poles due to the Miller feedback. The dominant pole is created to stabilize the feedback amplifiers by further narrowing the small bandwidth. As presented in chapter 2, most modern compensation methods require specific design for the corresponding compensation topology and in general some particular design conditions are imposed. For example, the first gain stage must have a gain much higher than the other stages or the second nondominant pole must be set above the unity gain frequency. These requirements complicate the circuit design and make the compensation configuration not very suitable for the general purpose op amp. A creative compensation methodology which can stabilize the op amp without sacrificing the bandwidth too much but is also compatible with the classical op amp architecture would be useful. This thesis proposes an active feedforward compensation scheme which is suitable for the usual op amp structure with two gain stages followed by a buffer stage. This compensation scheme does not limit the bandwidth of the amplifiers as the most widely used pole splitting Miller capacitor compensation approach does. Instead, the new method stabilizes the feedback amplifiers by increasing the gain bandwidth as well as the phase margin.

A single stage amplifier has good frequency response and good phase margin. But the dc gain of the single amplifier is not high enough and is further reduced by

the short-channel effect of submicron CMOS transistors. As a result, a modern high gain op amp requires at least two gain stages. Due to the many poles and zeros of multistage amplifiers, their frequency response and time response are far more complicated than those of single stage op amps. All uncompensated multistage amplifiers suffer closed loop stability problems and need compensation. A multistage op amp with more than three gain stages is uncommon because of the highly increased complexity of compensation. Many compensation schemes for multistage amplifiers have been investigated and reported [3–5, 7]. Chapter 2 of this thesis gives a detailed survey of the current compensation methods and points out their suitability for different situations.

Pole splitting, the most often used compensation technique, rolls off the gain before the phase lag becomes too great. The common method of pole splitting is to use a compensation capacitor between the input and output nodes of the second inverting stage of the op amp. The dominant pole is created due to Miller feedback. The negative Miller capacitance compensation method (NMCC) employs the idea to compensate a high speed CMOS op amp [35] with negative capacitance generated from the buffer stage by the Miller effect to reduce the original output load capacitance.

While single Miller compensation is applied for the simple two-stage amplifier, the extended version of the SMC compensation, nested Miller compensation (NMC) [15, 22, 24] is applied for amplifiers with three or more stages. The biggest weakness of the nesting topology is that the multiple compensation capacitors reduce the bandwidth substantially [5, 24, 25]. To improve the bandwidth, the variations of the NMC like NMC using nulling resistor (NMCNR) [4, 15], reversed nested Miller compensation (RNMC) [19], multipath NMC (MNMC) [5, 22, 24, 26], hybrid NMC (HNMC) [5], and nested Gm-C compensation (NGCC) [27] have been presented. Almost all these compensation techniques use Miller capacitors whose sizes are dependent on the load capacitor value, which make them inappropriate for small die area need.

The nonstandard NMC topologies have been developed for large capacitive loads. The represented strategies include damping factor control frequency compensation (DFCFC) [30], embedded RC compensation (ERC) [25], active feedback frequency compensation (AFFC) [31], and dual loop parallel compensation (DLPC) [32, 33]. These techniques result in complicated design, higher power consumption, and extra die area.

Some novel compensation designs like using a single Miller capacitor in three stage amplifiers (SMFFC) [27] and no Miller capacitor feedforward compensation scheme (NCFF) [34] have been proposed since 2003. But the particular design conditions and the intricate positioning problem of the zeros with the poles limit the application on the general purpose op amp.

The proposed feedforward method is one that can improve the phase response without deteriorating the bandwidth. The feedforward architecture is much easier to design compared to other feedforward schemes. It is very convenient to develop the proposed active feedforward in the classical two-stage operational amplifier with capabilities to drive large capacitive loads. Most existing op amp structures may be easily adapted to apply the proposed feedforward configuration. The basic concept of feedforward is to add a signal with less phase shift to the amplified signal, so that the resulting output has an improved phase response. Detailed analysis will be given in the following sections.

3.2 Configuration of the Feedforward Compensation Op amp

To visualize the effect of feedforward compensation on a circuit, it is helpful to represent the gain and phase of a circuit as a vector. The amplitude and phase are both frequency dependent. As the frequency increases, the gain drops off and the phase lag increases. Suppose the vector V_1 in Fig. 3.1 represents the output of our amplifier at some critical frequency. Now a smaller vector V_2 with less phase shift is added to V_1, where V_2 represents the feedforward signal. The vector sum V_3 is seen to have a magnitude similar to V_1, but with less phase lag. V_3 represents a performance

improvement over that of V_1. The circuits used in implementing feedforward are shown in Fig. 3.2. A_1 is the amplifier to be compensated. Its gain and phase at the unity gain frequency have been represented as V_1. A_2 is the feedforward stage, and it is designed to generate V_2 to have a gain and phase that combine favorably with V_1. Traditionally, passive circuits have been used to generate the feedforward signal. In this design, active circuits are used due to the wide variety of signals that they can generate. If a high pass filter is used on the feedforward signal, it can be made to help at high frequencies without affecting the dc and low frequency accuracy of the amplifier.

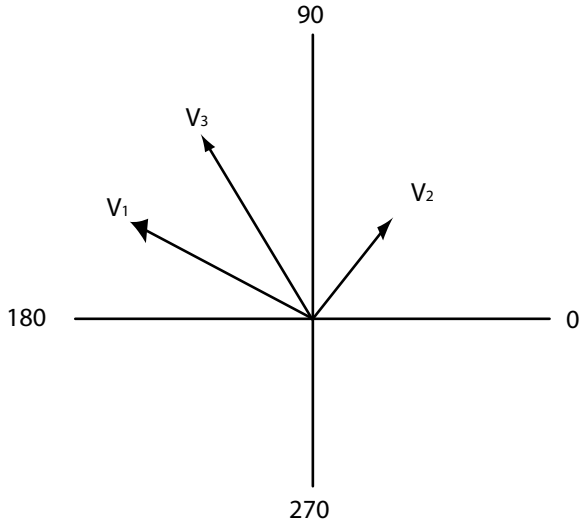


Figure 3.1: The phase diagram of feedforward

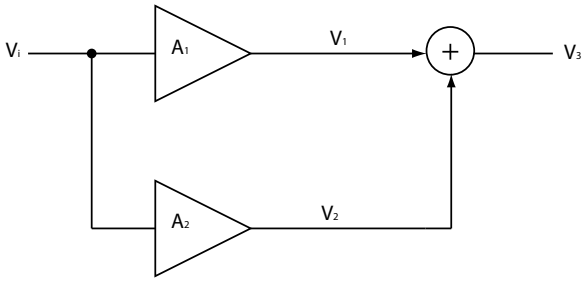


Figure 3.2: The block circuit of feedforward

3.2.1 Design Methodology

The design guide here is to apply the feedforward intuition on the system model and do the mathematical analysis to check if the idea works theoretically. After the feasibility is verified with theory, the feedforward scheme is then going to be evaluated by a system level simulation. Many different versions of SPICE simulators already have built-in system level models of the circuit blocks. System level simulation can be done within a short time compared to the device level simulation. For accuracy and other practical issues, a mixed simulation method combining the system level simulation with the device level simulation is a very efficient and viable way to assess the creative design method.

3.2.2 System Analysis of Feedforward Compensation

The analysis of the feedforward principle is started with a simplified system model assisted with mathematical analysis. Feedforward compensation is applied to the classical operational amplifier structure. A block diagram of a typical two-stage op amp is shown in Fig. 3.3. "Two stages" specifies the number of the gain stages in the op amp. A_{01} and A_{02} are the dc gains of the differential input stage and the inverting gain stage respectively. The frequency response of this multistage amplifier is modeled by cascading the dc gains and the two poles p_1 and p_2. The resulting open loop transfer function is

$$A(s) = \frac{A_0}{(1+s/p_1)(1+s/p_2)} \tag{3.1}$$

$$= \frac{A_{01}A_{02}}{(1+s/p_1)(1+s/p_2)}. \tag{3.2}$$

The corresponding unity feedback closed loop transfer function is

$$G(s) = \frac{A(s)}{1+A(s)} \tag{3.3}$$

$$= \frac{A_{01}p_1A_{02}p_2}{s^2+s(p_1+p_2)+(A_{01}p_1A_{02}p_2+p_1p_2)}. \tag{3.4}$$

This conventional 2-pole op amp model includes the additional nondominant poles from the inverting stage and the output buffer stage by patterning all nondominant poles (the third, fourth, and higher) into a single equivalent secondary pole p_2 [4]. In general, this model works reasonably well if the higher order nondominant poles are at frequencies greater than the unity gain frequency.

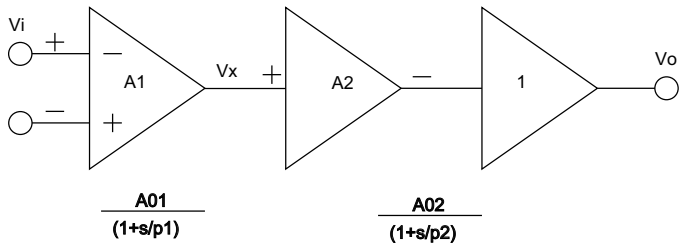


Figure 3.3: The typical two-stage operational amplifier model

A system level closed loop model of the feedforward compensation based on the conventional 2-pole model is shown in Fig. 3.4. The feedforward compensation consists of a lead network with a transfer function of $\frac{s}{s+\frac{1}{R_f C_f}}$, a negative wideband transconductance amplifier $-g_m$, and a feedback resistor R_b.

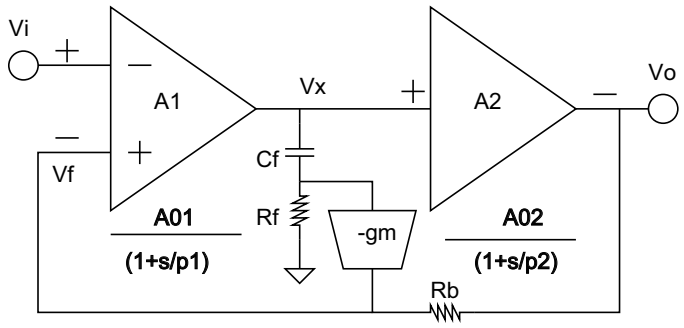


Figure 3.4: Simplified model of the feedforward compensated operational amplifier

The output voltage can be written as $V_o = -A_2 V_x$. The output voltage of the first stage is $V_x = -A_1(V_i - V_f)$. The feedback voltage after the feedforward

compensation is $V_f = V_o - V_x g_m R_b \frac{s}{s+\frac{1}{R_f C_f}}$. Manipulating the above equations results in

$$V_x = \frac{V_o}{-A_2} = -A_1(V_i - V_o + \frac{V_o}{-A_2} g_m R_b \frac{s}{s+\frac{1}{R_f C_f}}). \tag{3.5}$$

The closed loop transfer function $G_{cl}(s) = \frac{V_o(s)}{V_i(s)}$ of our feedforward compensation configuration becomes

$$G_{cl}(s) = \frac{A_1 A_2}{A_1 A_2 + 1 + A_1 g_m R_b \frac{s}{s+\frac{1}{R_f C_f}}}, \tag{3.6}$$

where $A_1(s) = \frac{A_{01}}{1+\frac{s}{p_1}}$ and $A_2(s) = \frac{A_{02}}{1+\frac{s}{p_2}}$. The closed loop transfer function is given as

$$G_{cl}(s) = \frac{A_{01} A_{02}}{A_{01} A_{02} + (1 + s/p_1)(1 + s/p_2) + A_{01} g_m R_b (1 + s/p_2) \frac{s}{s+\frac{1}{R_f C_f}}} \tag{3.7}$$

$$= \frac{A_{01} p_1 A_{02} p_2}{s^2 + s\left(p_1 + p_2 + A_{01} p_1 g_m R_b \frac{s+p_2}{s+\frac{1}{R_f C_f}}\right) + (A_{01} p_1 A_{02} p_2 + p_1 p_2)}. \tag{3.8}$$

3.3 Stability Analysis

To simplify the analysis, we assume the pole generated by the lead circuit $\frac{1}{R_f C_f}$ equals p_2 even though it does not need this constraint in practice. The transfer function thus becomes

$$G_{cl}(s) = \frac{A_{01} p_1 A_{02} p_2}{s^2 + a_1 s + a_0} \tag{3.9}$$

where $a_1 = p_1 + p_2 + A_{01} p_1 g_m R_b$ and $a_0 = A_{01} p_1 A_{02} p_2 + p_1 p_2$. Since the order of the denominator in Eq. (3.9) is higher than that of the numerator, the stability condition can be found from the coefficients of the denominator by applying the Routh-Hurwitz stability criterion [37].

The Routh-Hurwitz stability criterion is a necessary and normally sufficient method to establish the stability of a single-input, single-output, linear time invariant control system. Certain calculations using only the coefficients of a given polynomial can determine if the system is stable or not. The criterion establishes a systematic way to show that the linearised equations of motion of a system have only stable solutions e^{pt}, that is where all p have negative real parts. A tabular method can be used to determine the stability when the roots of a higher order characteristic polynomial is difficult to obtain. For an n - th order polynomial with the form of

$$A(s) \quad = \quad a_n x^n + a_{n-1} x^{n-1} + ... + a_1 s + a_0, \tag{3.10}$$

if any of the coefficients is zero or negative and at least one of the coefficients is positive, then there is at least one root that is imaginary or that has positive real parts in the right half plane. Therefore, the system is unstable.

If all coefficients are positive, the "Routh Array" can be formed by arranging the coefficients in rows and columns as Table 3.1.

Table 3.1: Routh Array

s^n:	a_n	a_{n-2}	a_{n-4}	...
s^{n-1}:	a_{n-1}	a_{n-3}	a_{n-5}	...
s^{n-2}:	b_1	b_2	b_3	...
s^{n-3}:	c_1	c_2	c_3	...
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
s^2:	d_1	d_2		
s^1:	e_1			
s^0:	f_1			

The third row elements of the array are computed by

$$b_i \quad = \quad \frac{a_{n-1} a_{n-2i} - a_n a_{n-2i-1}}{a_{n-1}}. \tag{3.11}$$

The procedure begins with $i = 1$ and is repeated until $b_i = 0$ for higher values of i. The fourth row of the array can be calculated by the formula

$$c_i = \frac{b_1 a_{n-2i-1} - b_{i+1} a_{n-1}}{b1}. \tag{3.12}$$

This process continues until f_1 has been calculated.

When completed, the number of sign changes in the first column will be the number of non-negative poles. The Routh-Hurwitz stability criterion states that the number of roots with positive real parts is equal to the number of changes in sign of the coefficients in the first column of the matrix. A stable system has all of its poles in the left half plane. This means that all coefficients a_i must be positive and all terms in the first column of the matrix must be positive for the system to be stable.

The Routh array of this closed loop transfer function is shown in the following Table 3.2.

Table 3.2: The Routh Array of Proposed Feedforward Compensation

s^2:	1	$A_{01}p_1A_{02}p_2 + p_1p_2$
s^1:	$p_1 + p_2 + A_{01}p_1g_mR_b$	0
s^0:	$A_{01}p_1A_{02}p_2 + p_1p_2$	0

The necessary and sufficient condition for the amplifier to be stable is that all the coefficients of the denominator must be positive. This gives the stability condition of amplifiers compensated by the negative transconductance $-g_m$ amplifier stage as

$$g_mR_b > \frac{-(p_1 + p_2)}{A_{01}p_1}. \tag{3.13}$$

For the amplifier compensated by the positive transconductance g_m amplifier, the amplifier is stable if and only if

$$g_m R_b < \frac{(p_1 + p_2)}{A_{01} p_1}. \tag{3.14}$$

It is apparent that amplifiers compensated by the negative transconductance amplifier stage automatically satisfy the Routh stability while amplifiers compensated by the positive transconductance amplifier stage only satisfy the Routh stability for a very limited range. To ensure stability and facilitate the tuning of the compensation network to get the best frequency and transient responses, the negative wideband transconductance amplifier is chosen to be applied for feedforward compensation.

3.3.1 Damping Analysis

A transfer function is given in the form of

$$\begin{aligned} H(s) &= \frac{A_0 \omega_0^2}{s^2 + 2\xi\omega_0 s + \omega_0^2} \\ &= \frac{A_0 \omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}, \end{aligned} \tag{3.15}$$

where the damping factor ξ is related to the quality factor Q as $\xi = \frac{1}{2Q}$. The poles of Eq. (3.15) are given by

$$\begin{aligned} p_{1,2} &= -\xi\omega_0 \pm \omega_0 \sqrt{\xi^2 - 1} \\ &= -\frac{\omega_0}{2Q} \pm \frac{\omega_0}{2Q} \sqrt{1 - 4Q^2}. \end{aligned} \tag{3.16}$$

It is clear that the poles are complex only when the damping factor $\xi < 1$ or $Q > \frac{1}{2}$ and this case is called underdamped. The case of $\xi = 1$ or $Q = \frac{1}{2}$ is called critically damped and the poles are two identical real numbers. While the case of $\xi > 1$ or $Q < \frac{1}{2}$ is called overdamped and the poles are two distinct real numbers. If $\xi = Q = \frac{1}{\sqrt{2}}$, the magnitude of the real part of the complex poles equals to that of the imaginary part. For the second order system, it is said to have maximally flat response.

3.3.2 Maximally Flat Response

To facilitate the analysis, the closed loop transfer function of Eq. (3.8) can be written in the form of

$$G_{cl}(s) = \frac{\frac{A_{01}p_1A_{02}p_2}{A_{01}p_1A_{02}p_2+p_1p_2}}{s^2\frac{1}{A_{01}p_1A_{02}p_2+p_1p_2} + s\frac{p_1+p_2+A_{01}p_1g_mR_b}{A_{01}p_1A_{02}p_2+p_1p_2} + 1}. \quad (3.17)$$

The poles of this transfer function are typically complex. If the feedforward compensated amplifier in feedback configuration is designed to have maximally flat response, the denominator of the transfer function should have the format of the second-order Butterworth polynomial with cutoff frequency w_0 as

$$B(s) = s^2\left(\frac{1}{{w_0}^2}\right) + s\left(\frac{\sqrt{2}}{w_0}\right) + 1. \quad (3.18)$$

where,

$$w_0 = \sqrt{A_{01}p_1A_{02}p_2 + p_1p_2} \quad (3.19)$$

and

$$g_mR_b = \frac{\sqrt{2(A_{01}p_1A_{02}p_2 + p_1p_2)} - p_1 - p_2}{A_{01}p_1}. \quad (3.20)$$

Eq. (3.19) and Eq. (3.20) as well as the assumption $\frac{1}{R_fC_f} = p_2$ could be the design guides to select certain values for maximally flat response. But it is not necessary for feedforward compensation design to follow these requirements. According to the specific needs of an application, a variety of choices are available.

3.4 Frequency and Transient Domain Simulation

It is straightforward to make a quantitative comparison of the frequency and step responses of the different amplifier compensation techniques on op amps with similar architectures. In order to explain how the different compensation methods

modify the closed loop transfer function and how the altered poles affect the feedback amplifier response, a two-stage op amp is used as an example.

3.4.1 Example 1 - Conventional Feedback Amplifier (Uncompensated)

Consider the conventional amplifier of Fig. 3.3 with feedback factor F chosen to be one. Given the overall open loop dc gain of 5000, assume the first stage has a gain of 100 with the bandwidth of 1 MHz and the second stage has a gain of 50 with the bandwidth of 2 MHz. This will provide the overall gain of 5000 with stage bandwidths of 1 MHz and 2 MHz respectively. A frequency normalization factor which equals to $2\pi \times 10^6$ is assumed. The open loop transfer function is in the form of

$$A(s) = \frac{10^4}{(s+1)(s+2)}. \tag{3.21}$$

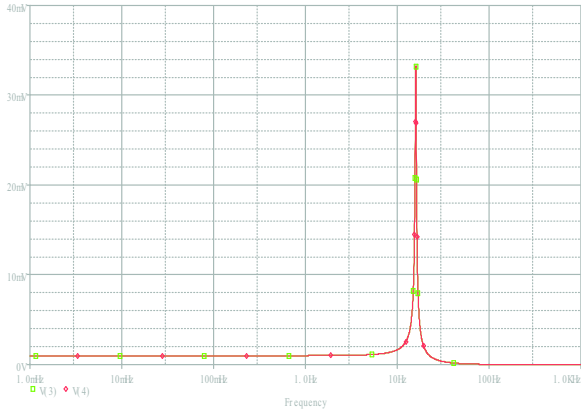
The frequency in the factorized form of Eq. (3.21) is the normalized frequency w_n. The normalized frequency is related to the actual frequency w_{act} by

$$w_n = \frac{w_{act}}{2\pi \times 10^6}. \tag{3.22}$$

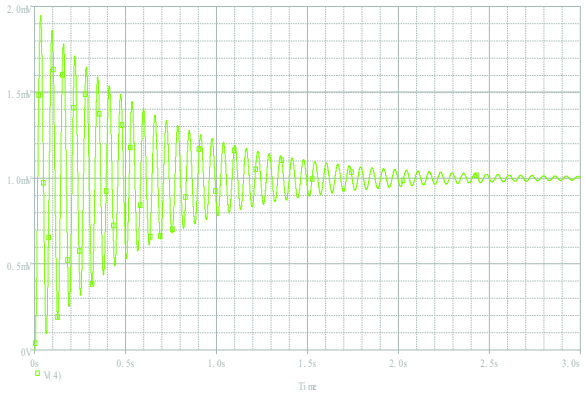
According to Eq. (3.3), the closed loop gain of the feedback amplifier is then expressed as

$$G(s) = \frac{10^4}{s^2 + 3s + (10^4 + 2)}. \tag{3.23}$$

From Eq. (3.23), the square of the first order coefficient of the denominator of G(s) is much less than that of the constant term. According to Eq. (3.15), it is obvious that the unity gain feedback has ξ much less than one and the poles by Eq. (3.16) are very close to the imaginary axis of the complex plane. As a result, it leads to underdamping and circuit instability. The simulation results displayed in Fig. 3.5



(a)



(b)

Figure 3.5: Uncompensated responses in frequency domain and time domain (a)Frequency response (b)Transient response

clearly demonstrate the peaking in the frequency domain and ringing in the time domain.

3.4.2 Example 2 - Pole Splitting (Simple Miller Capacitor Compensation)

If we use SMC to do pole splitting and assume that the smaller pole p_1 is further narrowed down to the dominate pole $\frac{p_1}{k}$ while p_2 is kept the same, the closed loop gain becomes

$$G(s)_{SMC} = \frac{A_{01}\frac{p_1}{k}A_{02}p_2}{s^2 + s(\frac{p_1}{k} + p_2) + (A_{01}\frac{p_1}{k}A_{02}p_2 + \frac{p_1}{k}p_2)}. \tag{3.24}$$

Applying Eq. (3.24), Eq. (3.23) is altered to

$$G(s)_{SMC} = \frac{\frac{10^4}{k}}{s^2 + s(\frac{1}{k} + 2) + (\frac{10^4+2}{k})}. \quad (3.25)$$

To achieve a maximally flat response, k is chosen to be 5000. The closed loop gain for this case where the second stage remains unchanged but the first stage is narrow banded from 1 MHz to 200 Hz (normalized frequency is changed from 1 to $\frac{1}{5000}$) becomes

$$G(s)_{SMC} = \frac{2}{s^2 + 2.0002s + 2.0004}. \quad (3.26)$$

3.4.3 Example 3 - Proposed Active Feedforward

If $\frac{1}{R_f C_f}$ is set equal to p_2 and $g_m R_b = 1.3844$ for maximally flat response according to Eq. (3.20), the resulting normalized gain function may then be expressed as

$$G(s)_{FF} = \frac{10^4}{s^2 + 141.44s + (10^4 + 2)}. \quad (3.27)$$

Comparing Eq. (3.27) to Eq. (3.23), the only difference is the first order coefficient of the denominator. The damping factor ξ changes from 0.03 to 0.707. The change from 3 to 141.44 of the first order coefficient sets the real parts of the complex poles away from the imaginary axis and stabilizes the amplifier. The resulting frequency responses of the SMC method in (3.26) and feedforward in (3.27) are shown in Fig. 3.6.

Since the feedforward scheme stabilizes the op amp without shrinking the bandwidth, it has higher gain bandwidth compared to the pole splitting SMC method. Fig. 3.6 shows the normalized bandwidth increment from 224.834 mHz to 15.898 Hz (denormalized bandwidth increment from 224.834 kHz to 15.898 MHz).

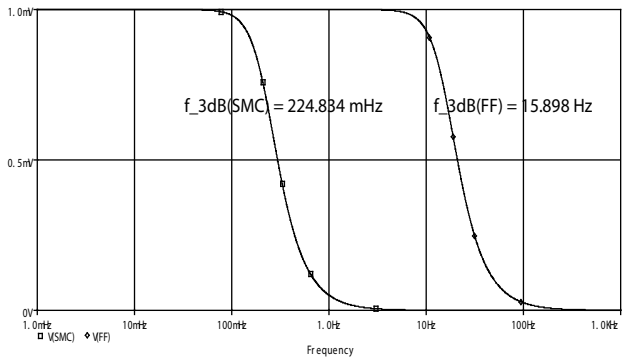


Figure 3.6: Frequency Responses of SMC and FF

One important parameter of a feedback amplifier is the settling time of the transient response. The settling time is defined as the time taken for the amplifier to settle to within a certain percent of its final value in order to avoid errors in processing signals. A longer settling time means that the analog signal processing speed is low. Fig. 3.7 shows the 1% settling time of transient response of a negative feedback op amp.

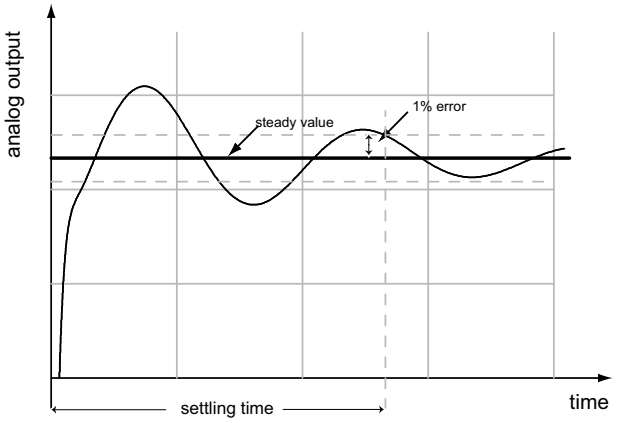


Figure 3.7: Settling Time of Feedback Op Amp Step Response

These closed loop functions for the SMC circuit (3.26) and the feedforward circuit (3.27) have transient responses shown in Fig. 3.8.

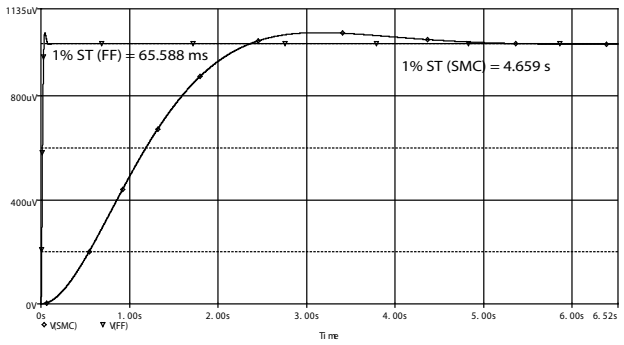


Figure 3.8: Step Responses of SMC and FF

Due to frequency normalization, the actual time t_{act} is related to the normalized time t_n by $t_{act} = \frac{t_n}{2\pi \times 10^6}$. It is clear that feedforward also achieves faster settling time. The step responses shown in Fig. 3.8 indicate that the normalized 1% settling time changes from 4.659 s given by pole splitting method to 65.588 ms given by the proposed feedforward method (actual settling time changes from 741.5 ns to the much faster 10.44 ns).

3.5 Open Loop Analysis

One popular way to predict the closed loop stability is by measuring the phase margin of the loop gain response. In general, a good performing amplifier needs a phase margin about 45° to 60° and a gain margin above 10 dB. Otherwise, the amplifier would possibly exhibit ringing in the time domain and peaking in the frequency domain [15, 23].

The proposed feedforward stage does not change the gain from the differential input stage to the output stage. In fact, the feedforward stage feeds a modified output instead of the exact output voltage back to the inverting input terminal in order to change the closed loop transfer function. The ratio of the altered feedback voltage to the positive input voltage forms the loop gain of the feedforward compensated op amp. As shown in Fig. 3.4 but with V_f not connected to the inverting input terminal,

the loop gain $A_{ol}(s) = \frac{V_f(s)}{V_i(s)}$ is given by

$$A_{ol}(s) = A_1 A_2 + A_1 g_m R_b \frac{s}{s + \frac{1}{R_f C_f}}. \tag{3.28}$$

Assuming $\frac{1}{R_f C_f} = p_2$, the loop gain leads to

$$A_{ol}(s) = \frac{A_{01} p_1 A_{02} p_2 + s A_{01} p_1 g_m R_b}{(s + p_1)(s + p_2)}. \tag{3.29}$$

If we treat $A_{ol}(s)$ in Eq. (3.29) like the conventional open loop gain comprised of the ratio of the output voltage to the input voltage without feedback connected to the input stage, the resulting closed loop gain from $A_{ol}(s)$ is $G_{clol}(s) = \frac{A_{ol}(s)}{1 + F A_{ol}(s)}$. And the closed loop transfer function in the case of the maximum feedback (F = 1) would be

$$G_{clol}(s) = \frac{A_{01} p_1 A_{02} p_2 + s A_{01} p_1 R_b g_m}{s^2 + a_1 s + a_0}, \tag{3.30}$$

where $a_1 = p_1 + p_2 + A_{01} p_1 g_m R_b$ and $a_0 = A_{01} p_1 A_{02} p_2 + p_1 p_2$. Comparing $G_{clol}(s)$ of Eq. (3.30) with $G_{cl}(s)$ of Eq. (3.9), the only difference is the additional term $A_{01} p_1 g_m R_b s$ which appears in the numerator of Eq. (3.30). It becomes natural that the open loop parameters of the feedforward amplifier, for example, the phase margin (PM) and the gain margin (GM) at the unity gain cross over frequency [19, 37] can still be used to predict proper closed loop behavior of the proposed active feedforward compensation scheme.

3.6 Generic Op amp Device Simulation Results

After the theoretical fundamental of the proposed feedforward compensation technique is verified with mathematical analysis and system level simulation, a mixed simulation which combines system level simulation with detailed device level simulation would be applied to further verify the performance of the design. The behavior simulation of the system is a very efficient way to test the basic idea of a circuit de-

sign. But due to the lack of detailed device characterization, sometimes system level simulation has the tendency to predict the circuit performance in a very idealistic way. Considering the complicated device physics properties, device level simulation which uses comprehensive transistor models like the advanced BSIM3 model with over a few tens of parameters is more accurate to describe and predict the circuit function. But in general device level simulation is very time consuming and makes designers take many circuit details under consideration before making the basic circuit work, not to mention losing the insights of some creative design ideas. A good mixed simulation with the system level description as well as the accurate device level models for some critical analog blocks would be productive for implementing ingenious circuit design and to be able to provide sufficiently accurate circuit performance prediction.

We use the popular 2-stage generic op amp as a vehicle to test the performance of the different compensation methods. To compare the simulation results between the conventional pole splitting by Miller capacitor feedback and the proposed feedforward compensation method, the 2-stage op amp design in [4] is chosen as a test bench. The schematic of the op amp is shown is Fig. 3.9.

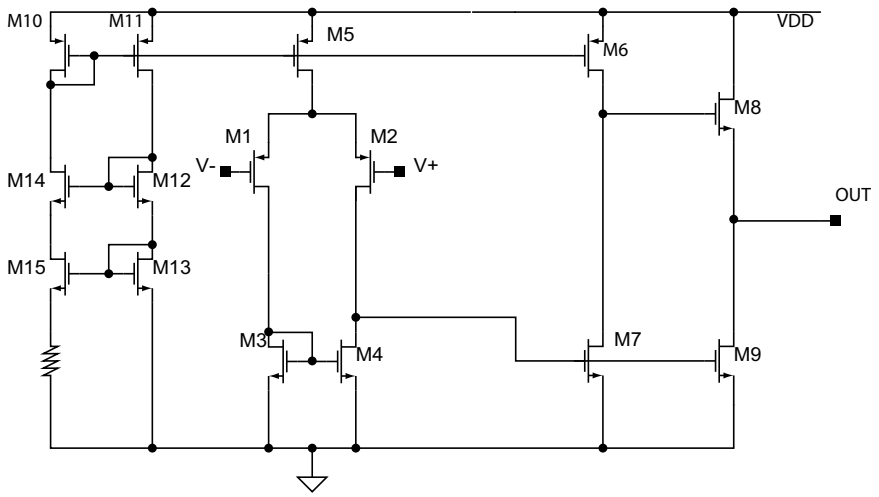


Figure 3.9: A classical two gain stage op amp

For SMC pole splitting method, a Miller capacitor C_c is placed between the input (the gate of M7) and the output (the drain of M7) of the second stage. The structure of the SMC compensated op amp is shown in Fig. 3.10.

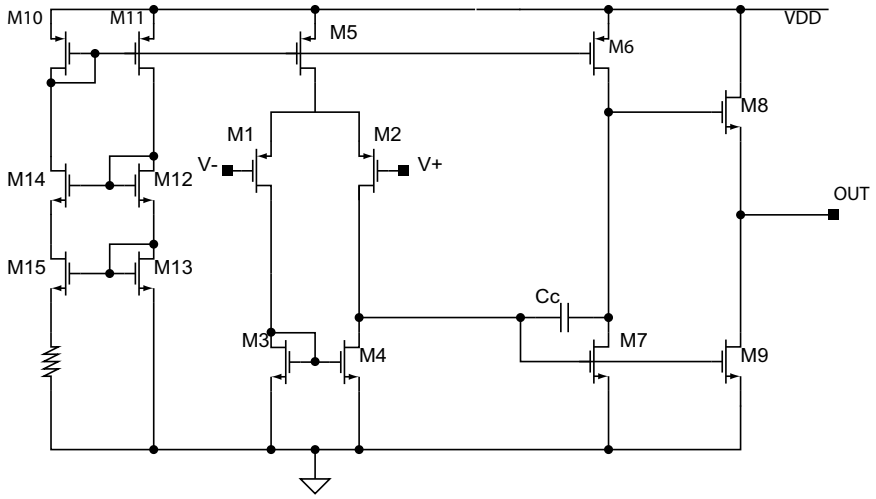


Figure 3.10: SMC compensated op amp

The feedforward compensation then replaces the Miller capacitor C_c with the feedforward stage consisting of the lead network $\frac{s}{s+\frac{1}{R_f C_f}}$, the negative wideband transconductance amplifier $-g_m$, and the feedback resistor R_b as shown in Fig. 3.11.

AMI 0.5 μm technology is applied and simulated in PSPICE. The first stage has a gain of 67.189 with bandwidth of $p_1 = 108.572$ kHz and the second stage has a gain of 81.209 with bandwidth of $p_2 = 1.0183$ MHz. The overall dc gain is 5456 V/V with supply voltages of plus and minus 2.5 V. The channel length of the transistors is chosen to be 1 μm. The output load resistor R_L is 5 $k\Omega$ and the load capacitor C_L is 20 pF. The compensation Miller capacitor C_C is 5 pF for SMC and SMRC. The lead resistor in series with the compensation capacitor for SMRC is 10 $k\Omega$. The highpass network parameters are chosen as $R_f = 30\ k\Omega$ and $C_f = 5.2098\ pF$ to satisfy $\frac{1}{R_f C_f} = p_2 = 2\pi \times 1.0183e6$. g_m is selected to be 1 mA/V and $R_b = 4.6075\ k\Omega$ based

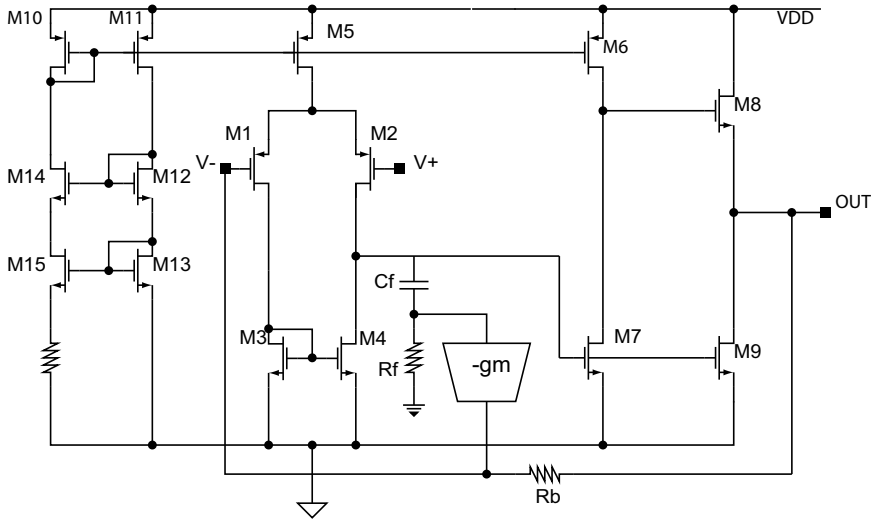


Figure 3.11: Feedforward compensated op amp

on Eq. (3.20). The three compensation methods SMC, SMRC, and Feedforward are simulated in PSPICE. The simulated results are tabulated in Table 3.3.

Table 3.3: Compensation Method Performance Comparison

Comp. Method	Ft(Hz)	PM	BW-ol	BW-cl	1% ST
SMC	144 k	80.485°	22.19	175.4 k	4.3224 μs
SMRC	143.68 k	83.067°	22.19	164.35 k	4.5487 μs
FF	37 M	79.418°	106.67 k	34.9 M	154 ns

The simulation shows that the proposed active feedforward compensation method is feasible to the existing popular op amp architecture. The performance of feedforward is superior to those of the other two pole splitting methods. With similar phase margins, the feedforward compensated op amp demonstrated larger bandwidth and faster settling time.

One possible problem related to this method is that the transient response is not as stable as the frequency response even though it has a reasonable measured phase margin. The transient response is not very consistent for input signals with

different frequencies, especially in the case of different rise and fall times. The problem might result from the non monotonically decreasing phase curve shown in Fig. 3.12. The phase goes down rapidly to $-170°$ before it goes up to $-90°$. In order for the phase margin to be a true measure of stability, the worst phase margin should not occur for gains higher than unity at all possible frequencies below the unit gain frequency.

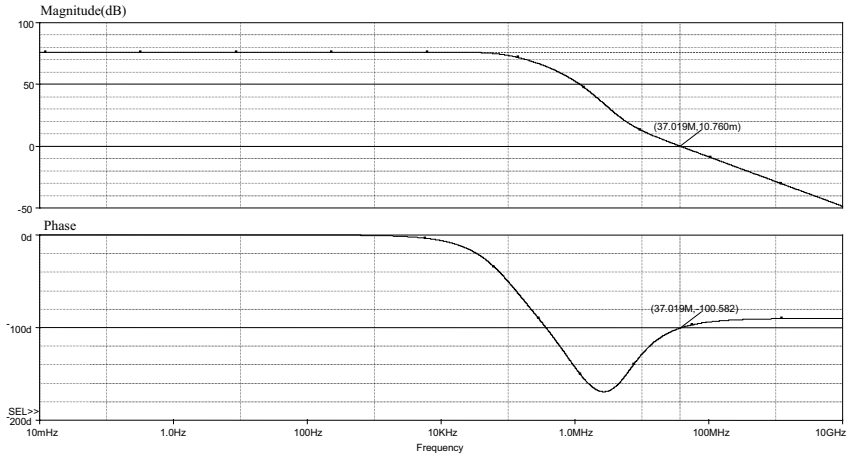


Figure 3.12: Frequency response of the feedforward model

3.7 Modified Feedforward Compensation Model Including The Lead And Lead-lag Circuits

To deal with the variable transient responses of the feedforward compensation method for different input situations, the additional phase lead networks are included to optimize this method in order to shape the phase curve and make the pattern of the transient response more robust. Fig. 3.13 shows a system level model of modified feedforward compensation strategy with lead and lead-lag circuits to improve the corresponding transient response.

The frequency response of the differential input stage is modeled by the dc gain A_{01} and the pole $p_1 = \frac{1}{R_1 C_1}$. Similarly, the frequency response of the inverting stage is modeled by the dc gain A_{02} and the pole $p_2 = \frac{1}{R_2 C_2}$. The buffer stage is used

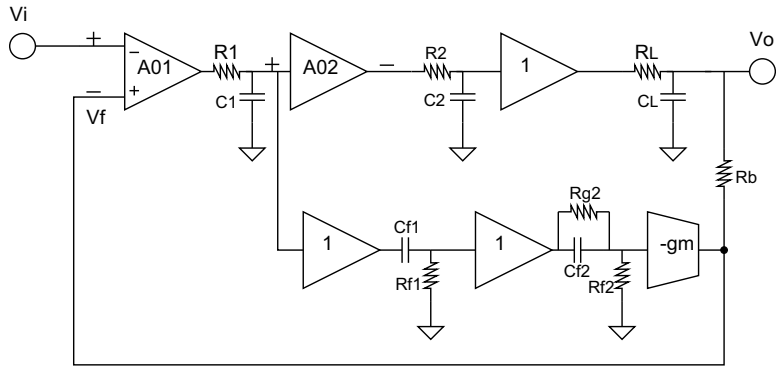


Figure 3.13: Modified feedforward compensation system model

to isolate the output of the second stage from the load stage in order to be used for the case of small resistance load or large capacitive load or both. The resulting open loop transfer function is

$$A(s) = \frac{A_{01}A_{02}}{(1+s/p_1)(1+s/p_2)(1+s/p_3)}, \tag{3.31}$$

where $p_3 = \frac{1}{R_L C_L}$. The system level model realistically represents the bench mark circuit but can be used to include or adjust any of the three dominant poles. As shown in Fig. 3.13, the feedforward compensation path consists of a negative wideband transconductance amplifier $-g_m$, a feedback resistor R_b, a lead network consisting of R_{f1} and C_{f1} with the transfer function $\frac{s}{s+\frac{1}{R_{f1}C_{f1}}}$, and a lead-lag network consisting of R_{f2}, C_{f2}, and R_{g2}. The transfer characteristic of the lead-lag circuit here is

$$H_{lead-lag}(s) \;=\; \frac{s+\frac{1}{R_{g2}C_{f2}}}{s+\frac{1}{(R_{g2}\|R_{f2})C_{f2}}}. \tag{3.32}$$

By adjusting the poles of the lead and lead-lag circuits $w_{p1} = \frac{1}{R_{f1}C_{f1}}$, $w_{p2} = \frac{1}{(R_{g2}\|R_{f2})C_{f2}}$, and the zero of the lead-lag circuit $w_{z2} = \frac{1}{R_{g2}C_{f2}}$, we can achieve better open loop phase margin of the circuit than the model shown in Fig. 3.4 and improve the closed loop transient response as well. The simulation results based on the updated feedforward compensation prove that the proposed approach functions successfully. The lead network is used to block the dc signal, give more phase lead,

and maintain the closed loop midband gain at unity. The above lead-lag circuit has $w_{z2} < w_{p2}$ based on its architecture. The modified Feedforward simulation results are tabulated in Table 3.4.

Table 3.4: Simulation Result Of Modified Feedforward Compensation with Lead-Lag

Comp. Method	Ft(Hz)	PM	Open Loop BW	Closed Loop BW	1% ST
FF	1.167 G	90°	106.92 k	1.557 M	933.6ns

Even though the settling time of the modified feedforward compensation with lead-lag is not as fast as that of the original feedforward compensation method recorded in Table 3.3, the phase curve of the modified feedforward is shaped to let the worst phase margin occur around the unity gain frequency as shown in Fig. 3.14. As a result, the transient response of the modified feedforward method is more consistent with different input signals.

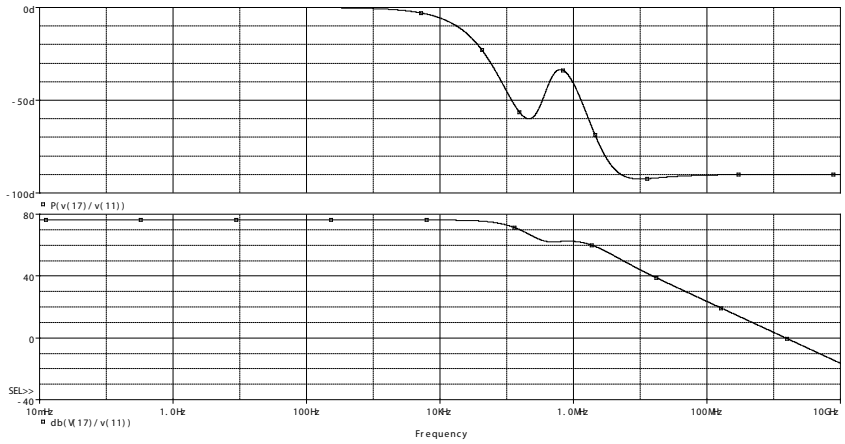


Figure 3.14: Frequency response of the modified feedforward method

3.8 Design of the g_m with the Lead-lag Circuit

Intuitively, we think a well-designed lead-lag circuit might replace the individual lead-lag circuit along with the $-g_m$ wideband transconductance circuit in Fig. 3.13. One proposed g_m architecture including one pole and one zero is presented in Fig. 3.15.

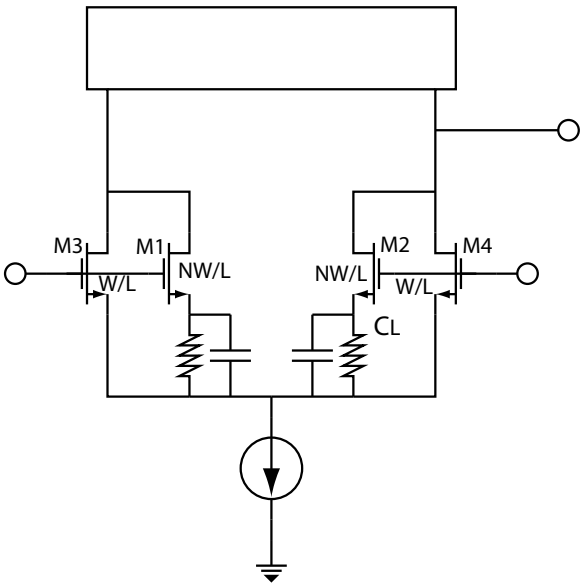


Figure 3.15: Creative g_m design

3.9 Conclusion

In this chapter, the technique of a creative feedforward compensation method of op amps is introduced and presented in detail. The proposed feedforward compensation overcomes the serious drawback of bandwidth narrowing by the widely used pole splitting method. It can improve the phase margin as well as optimize the bandwidth of the op amp. The feedforward method can be easily applied to the existing popular two gain stage op amp architectures with very little alteration. The mathematical derivation and circuit simulation demonstrate the advanced property and improved performance of this feedforward compensation technique.

A design methodology used for this innovative feedforward compensation scheme, which combines intuition, mathematical analysis, and mixed level simulation is suggested. The mixed level simulation is comprised of both the system level simulation and the device level simulation for some critical analog circuit path. This mixed simulation can verify the behavior of design ideas in an effective way as well as providing sufficient accuracy to predict the circuit performance realistically.

Chapter 4

Low Voltage Low Power Op Amp Gain Boosting Techniques

4.1 Introduction

With the growing demand for low power mixed signal integrated circuits for portable or nonportable high performance systems, analog circuit designers are challenged with making analog circuit blocks with lower power consumption with little or no performance degradation. Op amps are widely used for control and instrumentation applications where high accuracy is required. There has been a trend toward lower voltage and lower current operation to meet the needs of battery operated products and CMOS op amps are ideally suited for low power application. The classic Widlar op amp architecture, originally developed for bipolar junction transistors (BJT), has required modification for use with CMOS devices. In particular, it has proved difficult to match the open loop gain of bipolar op amps with CMOS technology [3, 4]. This is due to the inherently lower transconductance of CMOS devices as well as the gain reduction due to short channel effects that come into play for submicron CMOS processes. As a result, gain boosting schemes have been reported [5,6] to improve the gain. Multiple stage amplifiers with gain stages of more than three may be used for higher gain analog circuit designs. Nevertheless, multistage amplifiers generally are difficult to compensate.

One way to reduce the power consumption of op amp circuits is by scaling down the power supply voltage. Resulting in a reduced input common mode range and output swing. Since the threshold voltage of MOSFET does not scale down at the same rate as the reduction of the minimum transistor length with the advance

of technologies as shown in Fig. 4.1. V_{GS} is the gate-to-source voltage and V_T is the nominal threshold voltage.

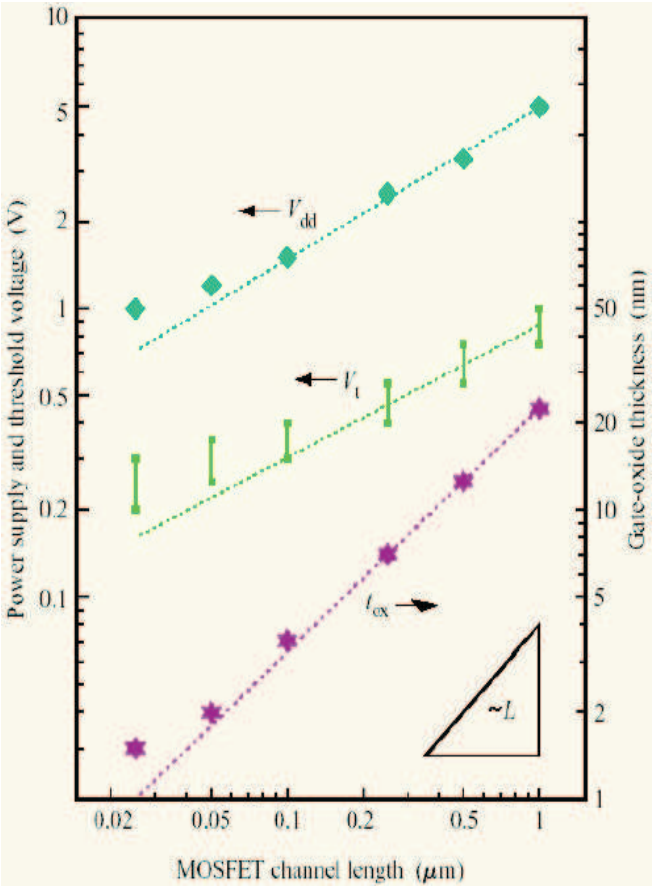


Figure 4.1: Power supply and threshold voltage versus the MOSFET channel length [1]

Reduced power supply voltage makes many existing gain boosting techniques no longer suitable for standard CMOS processes. Moreover, static power dissipation increases with the decreased threshold voltage. Scaling does not benefit analog circuits as great as it does digital circuits since the minimum size transistors are not usually selected in analog circuits because of noise and offset voltage constraints.

There are two classes of low voltage op amps in general. The first class operates with 2-3 Volt power supplies while the second class works with power supplies below 1.5 Volt. Op amps in the range of 2-3 V power supply low voltage range can still use

some existing structures with minor changes while op amps used under 1.5 V power supply low voltage range have to adapt some innovative designs to fit the extremely low voltage.

One important design aspect is the operation region of transistors. Power consumption is the highest when the MOSFET works in strong inversion while power consumption is much lower if the MOSFET works in weak inversion or subthreshold region due to the low quiescent drain current.

4.2 MOSFET Operation

MOSFETs in amplifier stages usually work in their active (saturation) regions. There are basically three operation regions of an MOS transistor within the active region; the strong inversion region, the moderate inversion region, and the weak inversion region.

When an n-type MOSFET is biased with voltages, three different situations may happen at the semiconductor surface. Assuming the source is tied to the p substrate at the zero voltage ground level, a negative voltage V_G applied to the gate will bring excess positive carriers (holes) to the interface and give rise to an accumulation of holes. This case is called the accumulation.

When a small positive voltage V_G is applied to the gate, the majority carriers (holes) near the semiconductor surface are repulsed and leave negative ions behind. This is called the depletion case since there are no free carriers available to cause the current flow.

As V_G gets larger, the positive gate voltage starts to attract minority carriers (electrons) in the p substrate to the gate surface area. The gate voltage required for the electron concentration under the gate to be equal to the majority carrier (hole) concentration in the p substrate is usually called the threshold voltage V_T. With V_G gradually increasing, when the electron concentration at the surface is larger than the intrinsic carrier concentration while the hole concentration is less than the intrinsic carrier concentration, the minority carrier (electrons) becomes majority at the surface

and the channel beneath the gate is inverted to n region. This is called the inversion case. At first, the surface is in a state of weak inversion region due to the small electron concentration. As gate voltage V_G is increased, the moderate inversion region and strong inversion region are reached.

The operation region of a MOS device as a function of $V_{eff} = V_{GS} - V_T$ is shown in Fig. 4.2. V_{GS} is the gate-to-source voltage and V_T is the nominal threshold voltage.

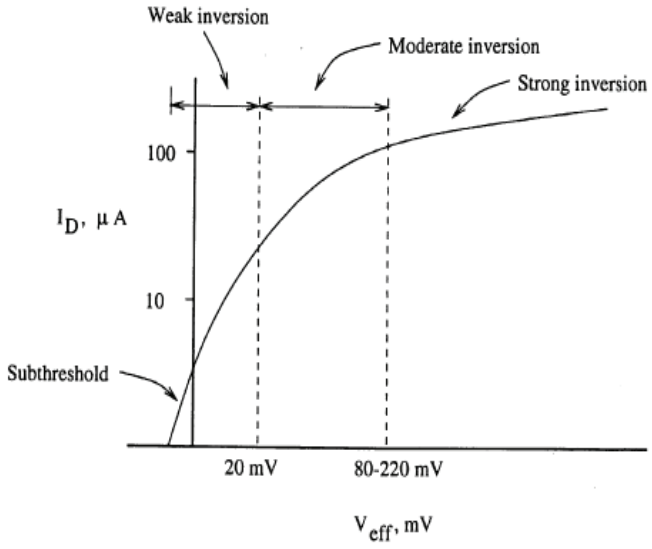


Figure 4.2: Operation regions of an MOS transistor [2]

4.2.1 Strong Inversion Region

The strong inversion region is the most frequently used among the three regions. In the strong inversion region, the commonly used drain current I_D with V_{GS} variation is represented by the square law equation

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}[V_{GS} - V_T]^2[1 + \lambda(V_{DS} - V_{eff})], \tag{4.1}$$

In this expression, μ is the surface mobility of the channel, C_{ox} is the capacitance per unit area of the gate oxide, W is the effective channel width, L is the effective channel length, λ is the channel length modulation factor, and V_{DS} is the resulting drain-to-source voltage.

The transconductance in the strong inversion region is [21]

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \sqrt{2\mu C_{ox}(W/L)I_D}. \tag{4.2}$$

The incremental drain-to-source resistance is

$$r_{ds} = \frac{1}{\lambda I_{DP}}. \tag{4.3}$$

where I_{DP} is the drain pinchoff current and is often approximated by I_D. The voltage gain A_0 of the single stage CMOS amplifier illustrated in Fig. 4.3 is given by

$$A_0 = -g_m r_{ds}. \tag{4.4}$$

In the strong inversion region, the gain varies with I_D as

$$A_0 = \frac{-K_1}{\sqrt{I_D}}. \tag{4.5}$$

This means that the gain is inversely proportional to the square root of the drain current. Lower current actually produces higher gain for strong inversion devices.

4.2.2 Moderate Inversion Region

As shown in Fig. 4.2, the MOS device starts to operate in the moderate inversion region when V_{eff} varies from a value of about 20 mV to approximately 220 mV [2]. In this region, drift and diffusion currents are similar. Increased gate-to-source voltage results in the strong inversion region when drift current dominates the diffusion current while decreased gate-to-source voltage leads to the weak inversion

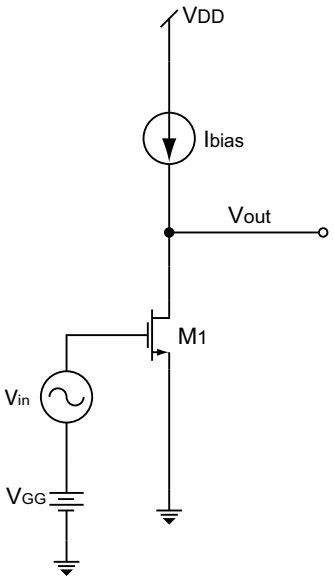


Figure 4.3: Single stage amplifier

region when diffusion current starts to dominates the drift current. There is no exact quantitative expression of the relationship between the current and V_{GS} in the moderate inversion region.

4.2.3 Weak Inversion Region

The lower end of the weak inversion region is the subthreshold region where V_{GS} is less than V_T. As V_{eff} ranges from subthreshold values up to about 20 mV, the device is in the weak inversion region. Sometimes people use weak inversion and subthreshold interchangeably. In the subthreshold region, the drain current decreases but remains finite as V_{GS} drops several tenths of a volt below V_T. The drain current decreases exponentially with V_{GS}. Subthreshold operation of the MOSFET can be used in low-voltage, low-power applications. The subthreshold state is dominated by diffusion current instead of drift current as in the case of strong inversion. The drain current as a function of the gate-to-source voltage is [6, 38]

$$I_D = \frac{W}{L} I_{D0} e^{qV_{GS}/nkT}(1 - e^{-qV_{DS}/kT}) \tag{4.6}$$

where n is the subthreshold slope factor, I_{D0} is a process-dependent parameter that is dependent also on source-to-bulk voltage and threshold voltage, k is Boltzmann's constant, T is the absolute temperature, and q is electronic charge. The subthreshold current is independent of the drain-to-source voltage once V_{DS} is higher than a few times the thermal voltage kT/q. The transconductance can be found from Eq. (4.6) and Eq. (4.2) as

$$\begin{aligned} g_m &= \frac{W}{L} I_{D0} \frac{q}{nkT} e^{qV_{GS}/nkT}(1 - e^{-qV_{DS}/kT}) \\ &= \frac{q}{nkT} I_D. \end{aligned} \tag{4.7}$$

It is clear that the transconductance is linear with the drain current in the weak inversion region. The incremental drain-to-source resistance is related to the early voltage V_A by

$$r_{ds} = \frac{V_A}{I_D}. \tag{4.8}$$

While V_A is approximately constant through the weak inversion region for a given channel length, the midband gain in the weak inversion region approaches a constant value or

$$A_0 = -g_m r_{ds} = -\frac{q}{nkT} V_A. \tag{4.9}$$

The relatively constant gain in the subthreshold region results in less signal distortion than those in the moderate and strong inversion regions as reported in [2, 39]. The weakly inverted MOSFET is very attractive for low power designs. The proposed composite cascode connection which combines strong inversion with weak inversion MOS devices will be introduced in the next chapter.

4.3 The Conventional Cascode Connection

To increase the gain of the CMOS stage, the transconductance of the stage can be improved or the output resistance seen by the first or second stage can be

enhanced. The output resistance increases in proportion to a decrease in bias current as shown in Eq. (4.3) while the transconductance increases as the square root of the increase in bias current as shown in Eq. (4.2). It is power efficient to increase the output resistance by lowering the bias current. The cascode structure is a widely used gain boosting scheme used in op amp design.

Fig. 4.4 shows a single stage amplifier using a conventional cascode connection where the common-gate stage device M2, biased by a voltage supply V_{G2}, is added to the input common-source stage M1. V_{G1}, V_{G2}, and I_{bias} are chosen to make M1 and M2 to operate in their active regions.

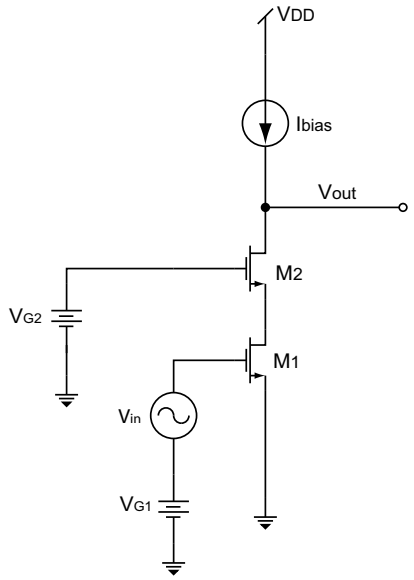


Figure 4.4: Conventional cascode amplifier

Assuming the current source I_{bias} is ideal, the output resistance is

$$r_{out} = r_{ds1} + r_{ds2} + (g_{m2} + g_{mb2})r_{ds1}r_{ds2}. \tag{4.10}$$

The midband voltage gain for the circuit of Fig. 4.4 is

$$A_0 = -[g_{m1}r_{ds1} + g_{m1}r_{ds1}(g_{m2} + g_{mb2})r_{ds2}], \tag{4.11}$$

where g_{m1} and g_{m2} are the transconductance of M1 and M2 individually, r_{ds1} and r_{ds2} denote the drain to source resistance of M1 and M2 at the bias point used, and g_{mb2} represents the transconductance that models the body effect of M2. As indicated by Eq. (4.11), it is clear that the cascode structure can achieve significantly higher voltage gain than the single stage of Fig. 4.3 by providing a higher output resistance. However, this configuration requires that the bias voltage V_{G2} for M2 be $V_T + 2V_{eff}$. The drain of M2 is set higher than V_{G2} in order to allow for some variational sinusoidal voltage swing. Thus, the use of a cascode as shown in Fig. 4.4 will require a supply voltage high enough to support the bias requirements of M1 and M2 as well as to provide headroom for the active load I_{bias}, which in practice may itself be implemented as a cascode. The input common mode level is very restricted due to structural constraints. The operation of this cascode connection has limitations for low voltage, low power applications due to the bias voltage requirement and limited output swing. To achieve an even higher gain, more cascode devices can be added in the cascode stack connection to form a "triple cascode". But this further reduces the already small output swing and the input common mode range.

4.4 Other Cascode Techniques

In order to continue applying the benefits of the high output impedance of the conventional cascode technique while alleviating the drawbacks like the very limited input common mode range, small output swing, and relatively high power supply requirements, modified cascode gain boosting techniques come into play.

4.4.1 Gain Boosted Cascode Amplifier

Fig. 4.5 shows a gain boosted cascode amplifier [17] or enhanced output impedance cascode amplifier [4]. This form of gain boosting technique is used to further increase the output impedance without using more cascode devices. The basic idea is to use a negative feedback amplifier to force the source of M2 (the drain of M1) to be at the same voltage as the bias voltage V_{G2} at the input of the feedback amplifier A_1. As a result, the drain-to-source voltage of M1 is less affected by the

voltage variation of V_{out} since the negative feedback amplifier A1 regulates the voltage and maintain the drain-to-source voltage of M1 stable.

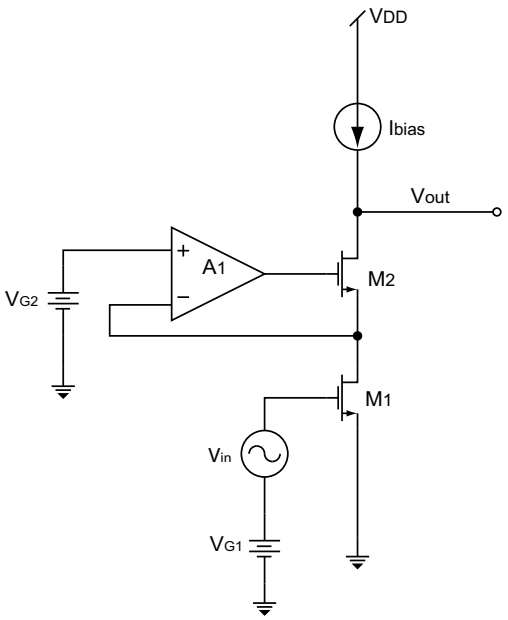


Figure 4.5: Gain boosted cascode amplifier

With small signal analysis, the output impedance is given by

$$r_{out} = r_{ds1} + r_{ds2} + g_{m2} r_{ds2} r_{ds1} (1 + A_1). \tag{4.12}$$

The form of the output impedance can be simplified as

$$r_{out} \approx A_1 g_{m2} r_{ds2} r_{ds1} \tag{4.13}$$

if A_1 is big enough. It is clear that the output resistance of this gain boosted cascode amplifier is further enhanced by A_1 compared to that of the conventional cascode amplifier. The midband voltage gain becomes

$$A_0 \approx -A_1 g_{m1} g_{m2} r_{ds2} r_{ds1}. \tag{4.14}$$

The gain boosted cascode amplifier can greatly improve the midband gain but further reduces the output swing. This structure is not suited for the second class low power supply voltage under 1.5 V. Even for the first class of 2-3 low voltage region, 3 Volt supply is a more appropriate choice due to the limited output swing. Another drawback is when the gain boosted cascode structure is used in a fully differential circuit design, it demands common mode feedback (CMFB) circuit since the output common mode level of the high output impedance circuit is very sensitive to device characteristics, mismatches, and temperature variation. Besides the drawbacks including a large number of external bias voltages and the sensitivity of the bias to process variation that the conventional cascode already has, the requirement of CMFB adds additional design complexity, higher power consumption, and extra chip area.

4.4.2 Folded Cascode Connection

To overcome the limited input common mode voltage and possibly improve the output swing of the conventional telescopic cascode connection, a structure called the "folded cascode" [4, 6, 17] can be used. Fig. 4.6 shows a simple folded cascode connected circuit.

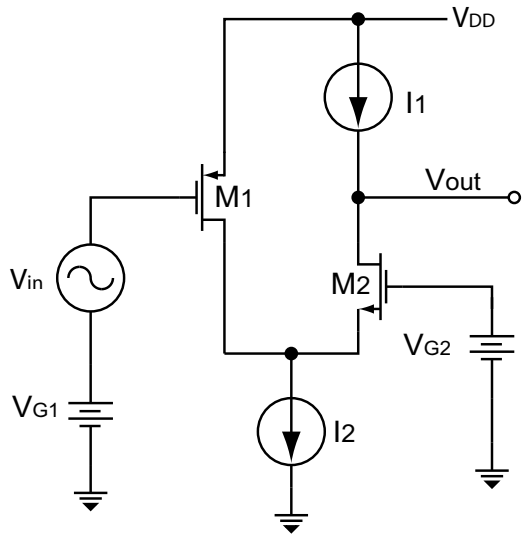


Figure 4.6: Simple folded cascode circuit

As illustrated in Fig. 4.6, the input device is supplanted with a P type MOSFET M1 to fold up the small signal current to the common gate NMOS device M2 and the output load. The main advantage of the folded structure is the freedom of choosing the bias voltage levels since it folds the two opposite type devices instead of putting one device on the top of another component.

The structure of a folded cascode op amp which employs the folded topology is shown in Fig. 4.7. This folded structure is used to improve the input common mode range. The folded cascode op amp has a push pull output stage which can sink or source current from the load. The exact match of the currents in the differential amplifier is not demanded by the folded cascode op amp since extra current can flow in or out of the current mirrors.

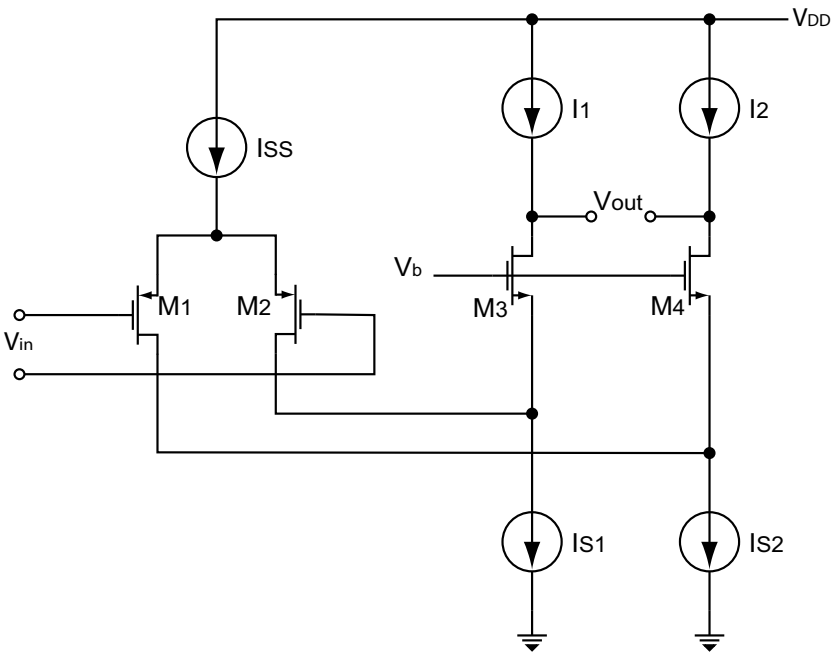


Figure 4.7: Folded cascode op amp structure

While the bias current of the conventional cascode delivers the current to both the input devices and the cascode devices since they are stacked together, the bias current I_{SS} of the folded cascode supplies only the input devices. Additional bias

currents such as I_1 and I_2 as shown in Fig. 4.7 are required to add the necessary bias current. In general, the folded cascode connection dissipates more power.

The gain of a folded cascode op amp is normally lower than that of a corresponding conventional cascode op amp due to the lower impedance of the devices in parallel. A folded cascode op amp has a pole at the folding connection which is lower compared to that node pole of the conventional cascode op amp. This is due to the larger parasitic capacitance of extra and possibly wider devices in the folded structure. Sometimes this low folding pole can self-compensate a folded cascode if the phase margin is good enough.

Calculations in [17] indicates that the output voltage swing of a folded cascode op amp is only insignificantly higher than that of a conventional cascode topology. The popularity of a folded cascode mostly comes from the flexible input common mode level and the availability of shorting the input and output together even though it consumes higher power and requires more complicated design.

4.5 Other Low Supply Voltage Techniques

As mentioned, one common way to reduce the power consumption of analog circuits is by reducing the power supply voltage. However, the circuit performance degrades at low voltages. It raises the challenge of modifying circuit structures for low voltage application since low voltage analog circuit design techniques are quite different from high voltage analog circuit design. The alteration or even redesign of the current circuit structure is necessary for low voltage operation.

Low voltage design is required for conditions when current levels are very small and supply voltages are low. Applications can be found but not limited to the biomedical area. The main restrictions of low voltage circuit design are the transistor threshold voltage and the device noise level. The down scaling of threshold voltage relies on specific device technology advancement. Higher threshold voltage has better noise margin and is less sensitive to noise while the lower threshold voltage decreases the noise margin and become more noise sensitive [40]. As a result, threshold voltage

can not be decreased below the noise floor level even with the availability of the fabrication technology to do so. A few low voltage design techniques for low power supply op amps are presented here.

4.5.1 Composite Cascode

If the conventional cascode structure is changed to bias the upper MOS device M2 in a way that has less effect on the output voltage swing, the output impedance of the connection may be increased with sufficient output swing at low supply voltage. One practice is to make both of the gates of M1 and M2 driven by the input signal and share a single bias source. This connection provides high output impedance due to source degeneration to give high output gains. This composite cascode approach, which combines the regular active devices with weak inversion devices, is promising in low voltage low power op amp design as will be introduced in detail and demonstrated in the next chapter.

4.5.2 Bulk-Driven Devices

A four terminal MOSFET transistor is usually treated as a three terminal device by tying the bulk terminal to ground or power supply V_{dd}. However, the bulk terminal can be used as the small signal input in amplifier circuits which are appropriate for the low voltage design environment. Fig. 4.8 shows a bulk-driven input stage of an op amp.

The ultimate limit of analog circuits in CMOS technology at low supply voltage comes from the threshold voltage. The turn on threshold voltage greatly inhibits the signal swing for the gate-driven MOSFETS. Instead, the bulk-driven device does not have this constraint on the threshold voltage.

The biasing current through its drain is necessary for a MOSFET to function. This drain current in a conventional gate-driven MOSFET is regulated by the gate-to-source voltage V_{GS} when the applied gate voltage surmounts the threshold voltage. In this case, bulk-source voltage V_{BS} has only a slight effect on the drain current

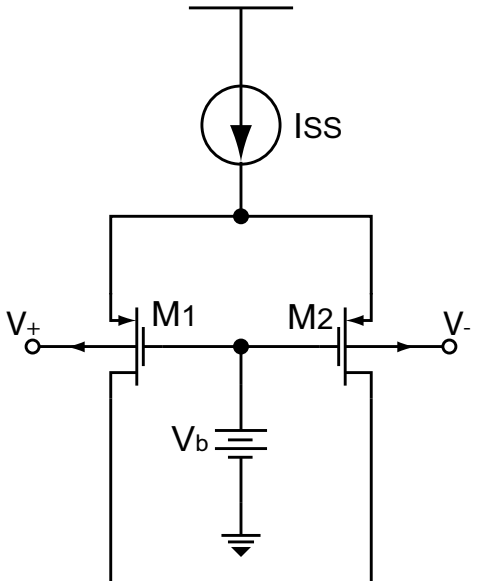


Figure 4.8: bulk-driven amplifier

which is called body effect. With the body effect or the backgate effect, the threshold voltage becomes

$$V_T = V_{T0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}), \tag{4.15}$$

where V_{T0} is the original threshold voltage without body effect, γ is the body effect coefficient with a value in the range of 0.3 to 0.4, ϕ_F is the equilibrium electrostatic potential (Fermi potential) in the semiconductor, and V_{SB} is the source bulk voltage. When $V_{SB} < 0$ or $V_{BS} > 0$, V_T is reduced and bulk source diode might be forward biased. Not only can V_T be adjusted by V_{BS} through the bulk node, the actual ac input signal can be driven through the bulk too.

In a bulk-driven MOSFET, we set V_{GS} at a bias voltage to turn on the MOSFET to have a continuous drain current and the input signal is applied at the bulk terminal. The bulk-driven MOSFET functions like a JFET. Because of the applied gate voltage, a channel exists between the source and drain of the MOSFET. The channel width is constant as long as gate bias does not change. The bulk terminal functions like the gate of a virtual JFET and modulates the channel width with the

applied voltage. The bulk-driven MOSFET has the depletion characteristics and it can work with negative, zero or slightly positive bias voltages. As a result, the constraint of V_T is totally removed in this case and these devices can work with power supply voltages under 1 V.

The bulk-driven transistor has a transconductance g_{mb} as shown below:

$$g_{mb} = \frac{\partial i_D}{\partial v_{BS}} = \frac{\gamma g_m}{2\sqrt{2\phi_F - V_{BS}}}. \tag{4.16}$$

The transconductance of a bulk-driven MOSFET is lower than that of a conventional gate-driven MOSFET, which may correspondingly decrease the gain and the bandwidth of a bulk-driven device. The small signal gain of a bulk-driven amplifier can exceed that of a standard gate-driven common source stage only when

$$V_{BS} \geq 2\phi_F - 0.25\gamma^2 \approx 0.5V, \tag{4.17}$$

where the transconductance g_{mb} of the bulk-driven device is larger than the standard gate-driven transconductance g_m. But it comes at the price of power dissipation due to the considerable current flowing in the bulk-source junction.

In [41], a 1-V op amp was designed using the bulk-driven technology to satisfy the low supply voltage condition and with rail-to-rail input and output range. This 1 V op amp has about 49 dB gain and a 1.3 MHz unity gain frequency. A phase margin of 57° is achieved while driving a 22 pF load capacitance.

The drawbacks of bulk-driven devices accompany their advantages. The polarity of the bulk-driven MOSFETs is related to process technology. There are only N-channel bulk-driven MOSFETs available for the P-well process while only P-channel MOSFETs are available for the N-well process. As a result, bulk-driven MOSFETs cannot be used in standard CMOS structures where both N and P channel MOSFETs are indispensable. Bulk-driven MOSFETs require separate wells in fabrication so as to have isolated bulk terminals. Thus, bulk-driven MOSFETs not only need more expensive processes and bigger chip area, but the matching between bulk-driven

MOSFETs in differential wells is worse than that of the conventional gate-driven devices in CMOS processes. Analog circuits which demand good matching between MOSFETs are not easy to obtain through bulk-driven devices.

4.5.3 Floating Gate MOS

A possible approach for low voltage design for the analog circuit is the floating gate technique. Floating gate MOS transistors are widely used as the storage elements in EPROM and EEPROM circuits. Floating gate MOSFETs are useful because they can store an electrical charge for extended periods of time even when the power is off. The schematic of a multiple input floating gate MOSFET is shown in Fig. 4.9.

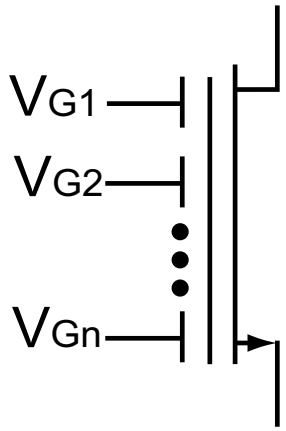


Figure 4.9: Floating gate transistor

Floating gate MOSFETs are not as widely utilized in analog circuits as in digital circuits. Floating gate devices are available in standard CMOS technology with double polysilicon due to their long existing popularity in digital circuits. Floating gate MOSFETs have the potential for low voltage analog design since the tuning of the threshold voltage is available. The gate of a floating gate MOSFET is generally floating with an electrical charge. This charge can stay constant for quite a long time due to the good insulation from the floating gate to other nodes. The floating gate is similar to the gate of a normal MOSFET but the voltage of the floating gate

is controlled by the control gates though capacitance coupling. The input common mode level can be set at an arbitrary voltage since the transistor is ac coupled through capacitance. A multi-input floating gate (MIFG) MOSFET, such as the one shown in Fig. 4.9, may be used for analog circuit design. The drain current versus gate-to-source voltage of the floating gate device is similar to that of a regular transistor.

A two input floating gate MOSFET is shown in Fig. 4.10.

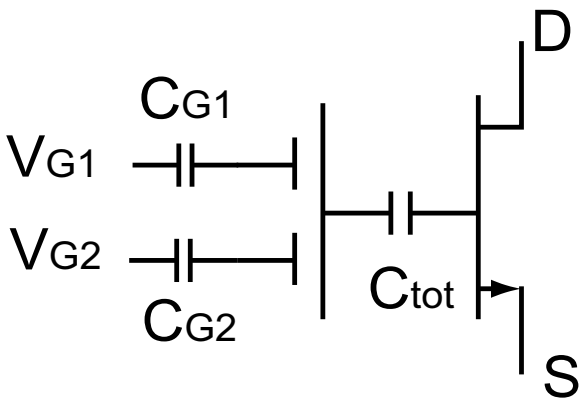


Figure 4.10: Two input floating gate transistor

The first polysilicon layer makes the floating gate over the channel while the multiple input gates are on the second polysilicon layer. For this two input gate MOSFET, a bias dc voltage V_{G2} is applied at the lower gate and the signal is applied at the upper gate. The threshold voltage with regard to the signal gate for the MOSFET is related to the threshold voltage of the floating gate $V_{T(FG)}$ as

$$V_T = \frac{V_{T(FG)} - V_{G2}k_1}{k_2}, \tag{4.18}$$

where $k_1 = C_{G1}/C_{tot}$ and $k_2 = C_{G2}/C_{tot}$. C_{G1} and C_{G2} are the capacitances between the control gates and the floating gates. C_{tot} is the sum of the capacitances between floating gate and the control gates, the capacitance between floating gate and

drain, the capacitance between floating gate and source, and the capacitance between floating gate and bulk [40].

V_T can be programmed to be less than $V_{T(FG)}$ with the appropriate selection of V_{G2}, k_1 and k_2. Thus, the MOSFET can have a modified V_T that is lower than the normal $V_{T(FG)}$. The equivalent transconductance of the combined structure $g_{m(eff)}$ is related to the transconductance seen from the floating gate $g_{m(FG)}$ as

$$g_{m(eff)} = k_2 g_{m(FG)}. \tag{4.19}$$

$g_{m(eff)}$ of the two input floating gate device is less than $g_{m(FG)}$ by a factor of k_2. The output impedance is less than that of a conventional MOSFET under the same bias condition due to the dc and ac feedback from drain to floating gate. This device is not suitable for high gain stage design. In general, the fabrication of the floating gates device costs more than regular CMOS.

Floating gate MOSFETs can be used to build op amp structures, which can operate at low voltage supplies. [42] presented a fully differential class AB/BA op amp with a 1.8 V power supply having a nominal gain of 5, rail-to-rail input and output swing, 1.6 MHz bandwidth, and 16 $V/\mu s$ slew rate while driving a 70 pF capacitive load. Research of floating gate MOSFETS used in op amp design with ultra low supply voltage below 1 V is underway by a few groups.

4.6 Conclusion

MOSFET operation is introduced and three different inversion levels are presented with the suggestion of applying weak inversion operation to low power design. A few popular cascode gain boosting techniques for op amp designs are presented with their merits and demerits. Some possible design techniques for a very low voltage environment are introduced and discussed. The choice of an appropriate technique or a combination of a few techniques can be employed for the corresponding low power high gain op amp design.

Chapter 5

Design of High Gain Op Amp Using Composite Cascode Connections

5.1 Introduction

Many gain boosting schemes have been reported [5,6] to improve the gain of an op amp. These gain enhancing methods often require complicated circuit structures and high supply voltage, and may produce a limited output voltage swing. Multiple stage amplifiers may be used for higher gain analog circuit designs. Many compensation schemes for multistage amplifiers have been investigated and reported [3–5, 7]. However, most compensation methods require more circuit area and more complex design than the dominant pole approach used in the classic op amp architecture.

Other high-gain CMOS op amps have been investigated in previous work [8–14], but most did not achieve gains higher than 100 dB. A few achieved a gain ranging from 120 dB to 130 dB. These CMOS op amp designs use up to five cascaded gain stages to achieve the high gain. The highest reported was the simulated 140 dB [10] unbuffered op amp with three cascaded gain stages. In general, high gain architectures need complex compensation to stabilize the op amp and generally require more than one compensation capacitor.

In papers [21, 40, 43], various aspects and applications using the composite cascode connection which consists of the series association of two MOS transistors have been reported. However, most variations are focused on one of the devices working in the active (saturation) region and the other device operating in the triode region. In 2004, Comer et al. [44] discussed the effects on the overall composite cascode circuit performance with one device operating in the subthreshold and the

other device operating in the active region and suggested that this approach may result in a very high gain stage for use in op amps.

This chapter discusses the design of a high gain, low power, general purpose op amp with the structural simplicity of the classical Widlar architecture. The proposed op amp structure applies composite cascode connections in both the input stage and the second stage to achieve a gain of around 120 dB with low power consumption. The op amp employs the traditional two gain stages followed by a near unity gain buffer stage. With only two gain stages, simple Miller compensation with a capacitor as small as 3.5 pF can be used. This approach overcomes some limitations of conventional CMOS cascodes by enhancing the gain without using additional bias circuits and requires only a small bias headroom voltage. A larger output voltage swing is then available using composite cascode amplifier stages than with conventional cascodes. As discussed in the former chapter, low power op amp can be designed by operating the MOS transistors in the subthreshold or weak inversion region. While the composite cascode provides high output impedance at a low bias current while setting some devices in the subthreshold region along with the other active region transistors, low power dissipation and high gain can be achieved at the same time.

5.2 The Composite Cascode Connection

In order to reduce the bias headroom voltage required for a conventional cascode, Comer et al. [21, 43, 44] proposed the composite cascode connection. The structure of the composite cascode connection is shown in Fig. 5.1. Both of the gates of M1 and M2 are driven by the input signal and share a single bias source V_{GG}.

If M2 and M1 have similar $\frac{W}{L}$ aspect ratios, M1 will operate in the triode region while M2 will operate in the active region. In this case the composite cascode works like a common-source stage, but with higher voltage gain. If M2 is chosen with a much higher aspect ratio than M1, with appropriate bias of V_{GG} and I_{bias}, M1 is placed in the strong inversion region while M2 is operating in the weak inversion region. The gain in this case can be further increased. Although the bandwidth is

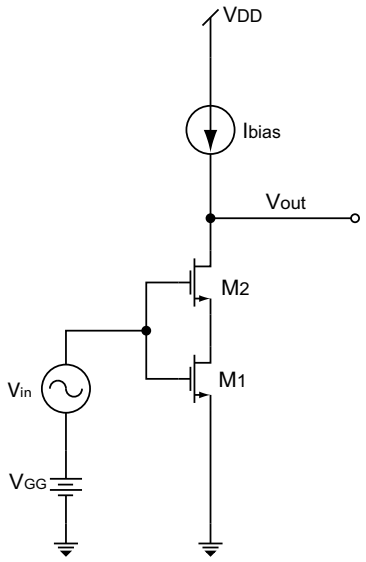


Figure 5.1: Composite cascode amplifier

lower than that of the conventional cascode due to the larger capacitance of the weak inversion device M2, this capacitance may be advantageous in the dominant pole compensation of the conventional op amp.

Assuming the current source has infinite output impedance, the output resistance is

$$r_{out} = r_{ds1} + r_{ds2} + (g_{m2} + g_{mb2}) r_{ds1} r_{ds2}. \tag{5.1}$$

It is obvious that Eq. (5.1) has the same expression as the output resistance in Eq. (4.10) of the conventional cascode. The voltage gain for the circuit of Fig. 5.1 is

$$A_0 = -[g_{m1} r_{ds1} + g_{m2} r_{ds2} + g_{m1} r_{ds1} (g_{m2} + g_{mb2}) r_{ds2}]. \tag{5.2}$$

If the current source load has a finite resistance R instead of the assumed infinite output impedance, the voltage gain then becomes

$$A_0 = -\frac{[g_{m1} r_{ds1} + g_{m2} r_{ds2} + g_{m1} r_{ds1} (g_{m2} + g_{mb2}) r_{ds2}]}{1 + \frac{1}{R}[r_{ds1} + r_{ds2} + (g_{m2} + g_{mb2}) r_{ds1} r_{ds2}]}. \tag{5.3}$$

Eq. (5.2) shows the composite cascode structure can achieve high gains similar to that of the conventional cascode stage in Fig. 4.4.

5.3 Practical Composite Cascode Circuit

Fig. 5.2 shows a practical composite cascode amplifier stage in which the ideal current source load has been replaced by PMOS devices M3 and M4.

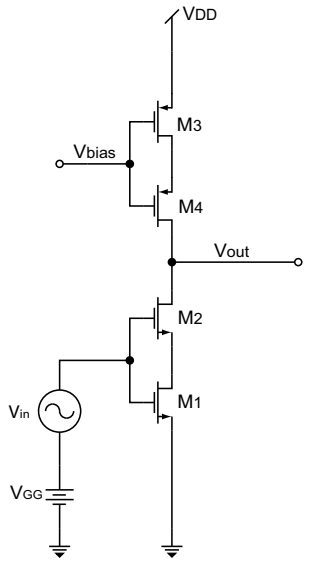


Figure 5.2: Practical composite cascode stage

Here M4 is chosen to have a larger $\frac{W}{L}$ aspect ratio than M3 similar to the ratio of M2 compared to M1. M4 is operated in the subthreshold region while M3 is in the active region. The output impedance looking into the drain of M4 is given by Eq. (5.1). If the impedance looking into the drain of M4 is equal to the impedance looking into the drain of M2, $R = [r_{ds1} + r_{ds2} + (g_{m2} + g_{mb2})r_{ds1}r_{ds2}]$, according to Eq. (5.3), the voltage gain of the composite cascode stage is then

$$A_0 = -\frac{1}{2}[g_{m1}r_{ds1} + g_{m2}r_{ds2} + g_{m1}r_{ds1}(g_{m2} + g_{mb2})r_{ds2}]. \quad (5.4)$$

This can also be written as

$$A_0 = -\frac{[g_{m1}r_{ds1} + g_{m2}r_{ds2} + g_{m1}r_{ds1}(g_{m2} + g_{mb2})r_{ds2}]}{1 + \frac{r_{ds1}+r_{ds2}+(g_{m2}+g_{mb2})r_{ds1}r_{ds2}}{r_{ds3}+r_{ds4}+(g_{m4}+g_{mb4})r_{ds3}r_{ds4}}}. \quad (5.5)$$

If M3/M4 are biased in the triode region, the gain would be lower but still greatly above that of the single stage amplifier.

5.4 Circuit Realization

The general purpose BJT op amp has traditionally been designed to have the classical Widlar architecture which consists of a high gain differential input stage, a moderately high gain second stage, and a low gain stage that acts as a buffer. The first two stages are used to provide overall voltage gain high enough for the op amps. MOS op amps are ideally suited for low power application. The classic Widlar op amp architecture, originally developed and widely used for bipolar devices, has been mimicked in CMOS devices. But it requires modification for use with CMOS devices. This is due to the inherently lower transconductance of CMOS devices as well as the gain reduction due to short channel effects that come into play for submicron CMOS processes. It has proved difficult to match the open loop gain of bipolar op amps with CMOS technology [3, 4]. The benefit of higher cutoff frequency due to smaller channel length is not needed for the first stage in pole splitting compensation methods. Relatively longer channel length devices can be used there. The use of longer channel devices also leads to higher voltage gains because of reduced channel-length modulation effects and higher output resistance. Additionally, longer lengths result in larger widths to achieve appropriate levels of channel inversion [2]. The larger gate areas of the input devices will also reduce the threshold voltage and transconductance mismatch.

5.4.1 Input Differential Composite Cascode Stage

As shown in Fig. 5.3, the first stage is the differential-to-single ended practical composite cascode stage with current mirror load.

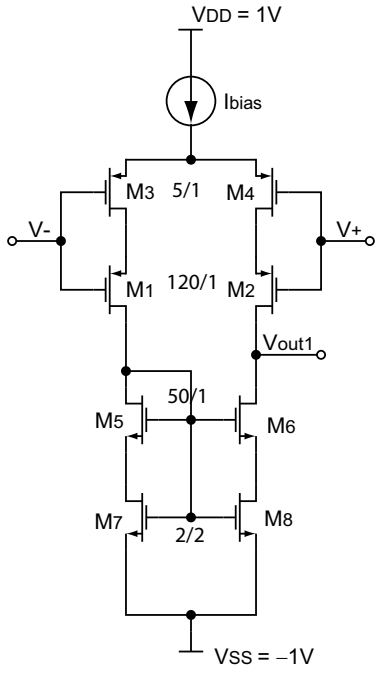


Figure 5.3: Op amp input differential composite cascode stage

The composite cascode connection in both N-channel and P-channel allows the input to swing from the positive power supply to the negative power supply. P-channel input devices provide for good power supply rejection. Moreover, the gain in the weak inversion region is relatively independent of drain current. In the composite cascode configuration, the output transistor is selected to have a much higher $\frac{W}{L}$ aspect ratio than that of the lower transistor. This allows a simple adjustment of the tail current to place the drain connected device M2 in the weak inversion region while the source connected device M1 operates in the strong inversion region. The transistors are scaled with a channel length of 1 μm, while allows better matching

than minimum length. The frequency response for the input stage is shown in Fig. 5.4. The midband gain for the chosen scaling is around 64 dB.

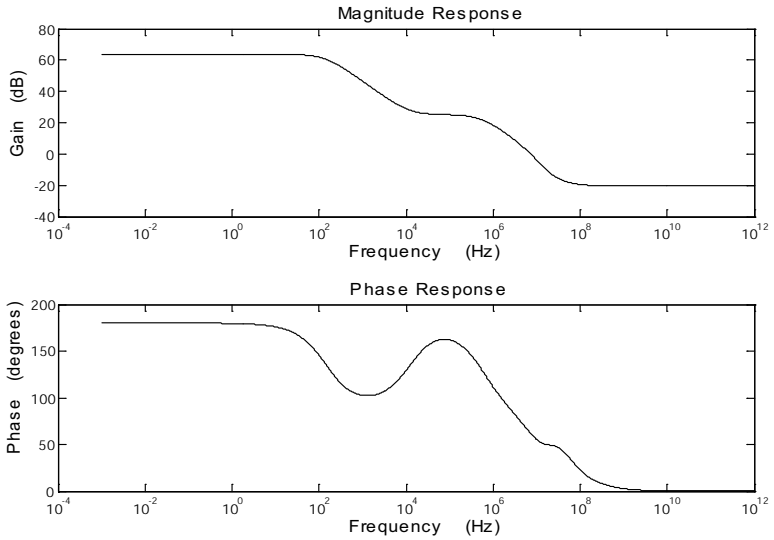


Figure 5.4: Op amp input stage frequency response

5.4.2 Composite Cascode Current Mirror

The current mirror used to provide the bias current to the input stage and the bias voltage to the second stage is shown in Fig. 5.5.

The bias current for the input differential stage is only 3.65 μA. This P type current mirror is also connected in the composite cascode structure in order to provide the robust bias current and voltage which can self adjust by tracking of the corresponding variation of the other composite cascode stages.

5.4.3 Second Composite Cascode Stage

The second stage is a common source stage implemented as a composite cascode shown in Fig. 5.6.

Different choices of the second stage architecture design may be applied to adapt to various situations as will be explained in a later section. The frequency

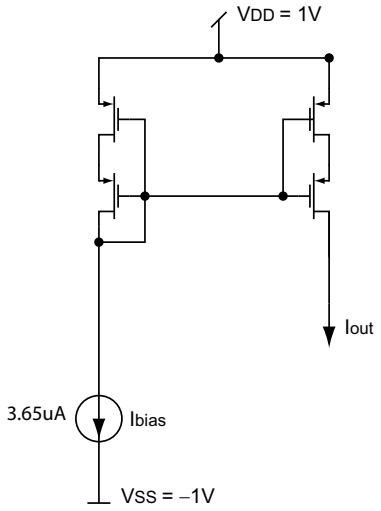


Figure 5.5: Op amp composite cascode current mirror

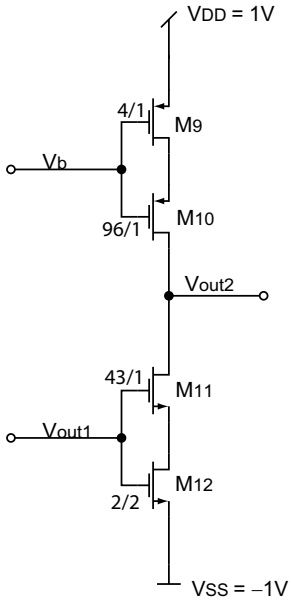


Figure 5.6: Op amp second composite cascode stage

response for the second stage is shown in Fig. 5.7. The midband gain is around 58 dB. The compensation capacitor used for pole splitting (simple miller compensation)

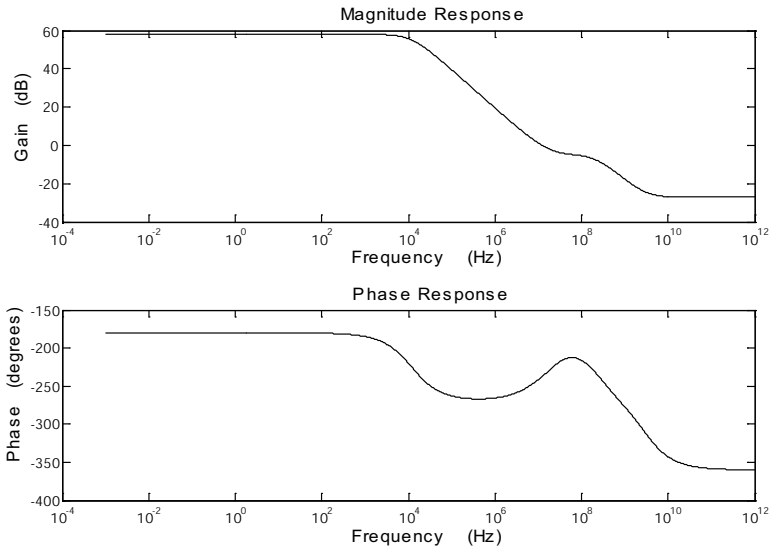


Figure 5.7: Op amp second stage frequency response

method is usually inserted between the input and output of this common source stage to apply the Miller feedback effect.

5.4.4 Output Source Follower With A Current-sink Load

The output stage is used as a buffer to drive an external load. A source follower with a current-sink load [4, 6] is used as shown in Fig. 5.8. This output buffer stage has low output impedance which allows loading by a large capacitive load or small resistive load.

The frequency response for the source follower stage is shown in Fig. 5.9. It is clear that its transfer function includes some "zeros" that improve the phase response. According to the analysis in [4], this type of source follower structure has a left half plane zero due to the parasitic capacitance C_{gs} which could generate phase lead and help achieve a more favorable phase margin. The disadvantage is that the output swing is lowered by a few tenths of a volt. Different output stages can be easily employed according to the corresponding circumstances. A rail-to-rail class

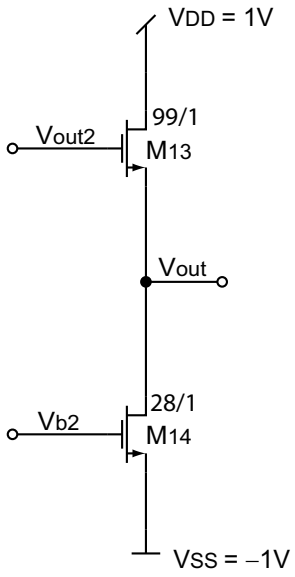


Figure 5.8: Op amp output source follower stage

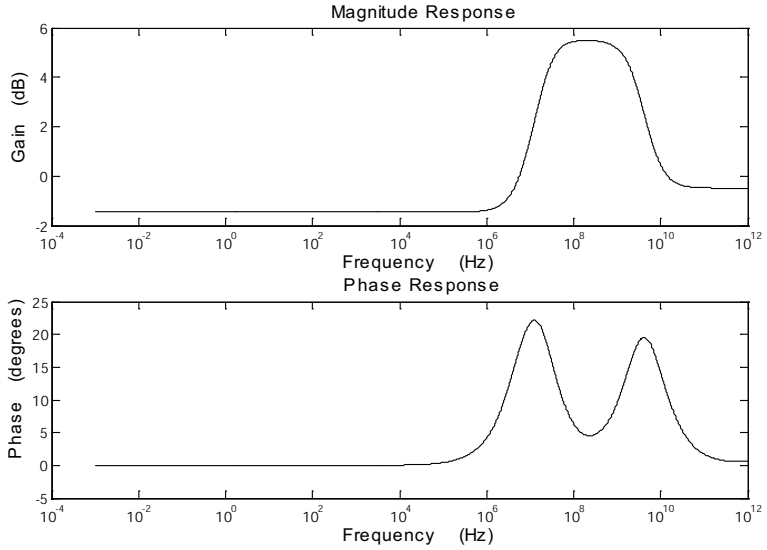


Figure 5.9: Op amp output stage frequency response

AB output stage will be introduced in a later section of this chapter. The output stage will not affect the main design topology of this composite cascode op amp.

5.4.5 Composite Cascode Op Amp in Widlar Architecture

Fig. 5.10 shows the overall schematic of a CMOS operational amplifier using composite cascode stages which implements the classical Widlar op amp structure,

with two gain stages followed by a buffer output stage as presented earlier. The entire op amp design does not use any extra bias voltage or current supplies. The only bias circuit is built inside the op amp chip to allow self adjustment.

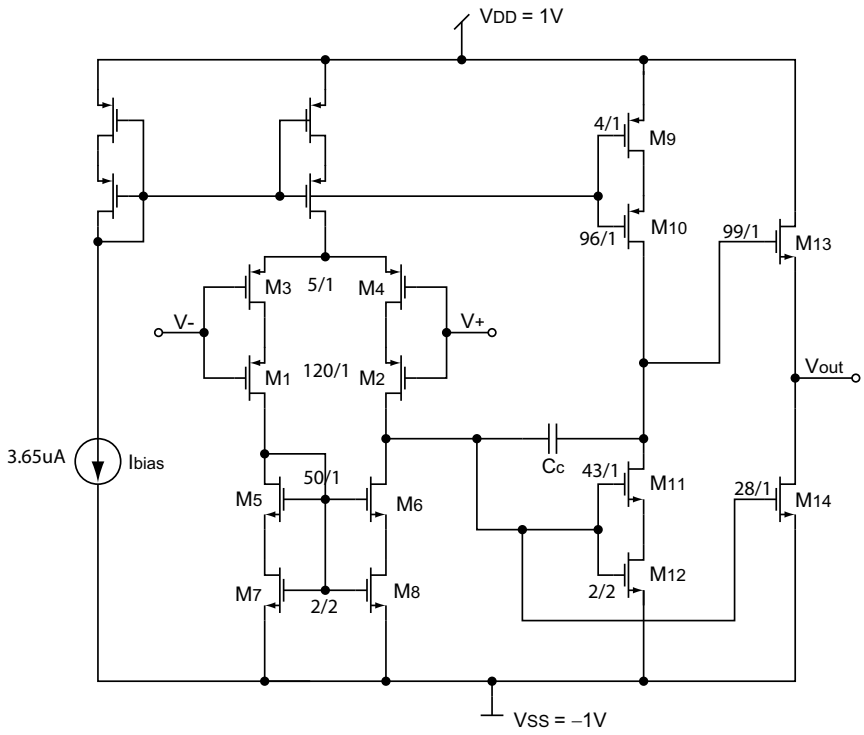


Figure 5.10: Composite cascode op amp

The DC voltage transfer curve of the composite cascode op amp is shown in Fig. 5.11, from which the common mode input range is seen to vary from -1 V to 0.7 V. The linear range is obviously the range of interest in an op amp. It denotes the voltage range over which the two inputs can be driven together even though only one input terminal of the op amp is actually connected with the input signal without causing common mode distortion.

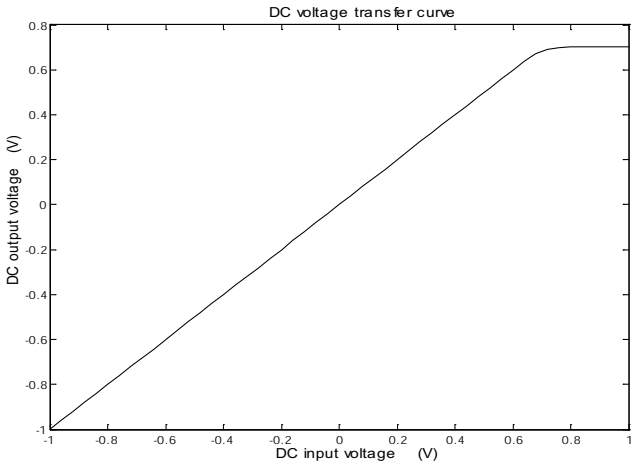


Figure 5.11: Composite cascode op amp DC transfer characteristic

5.4.6 Total Harmonic Distortion

Besides the low power dissipation and ease of compensation, this composite cascode op amp also has the advantage of reduced signal distortion over operation in the strong inversion region.

The total harmonic distortion (THD) is the ratio of the sum of the powers of all harmonic frequencies above the fundamental frequency to the power of the fundamental frequency as represented in Eq. (2.18). Fig. 5.12 shows the output waveforms for different input values.

5.5 Simple Miller Compensation (Pole Splitting)

Op amps require compensation to ensure closed loop stability. Compensation for CMOS op amps is more difficult when there is significant phase shift due to the large capacitive load. Early in 1967, Widlar designed the LM101/741 [18, 20] op amp which employed the "pole splitting" frequency compensation method [4, 20, 21, 45]. As the transistor gain of the second stage increases, the dominant pole frequency decreases and the nondominant pole location increases. In this way the two poles are being split apart and stabilize the feedback amplifiers by greatly narrowing the bandwidth. Miller compensation is popular for op amp design because of its simplicity

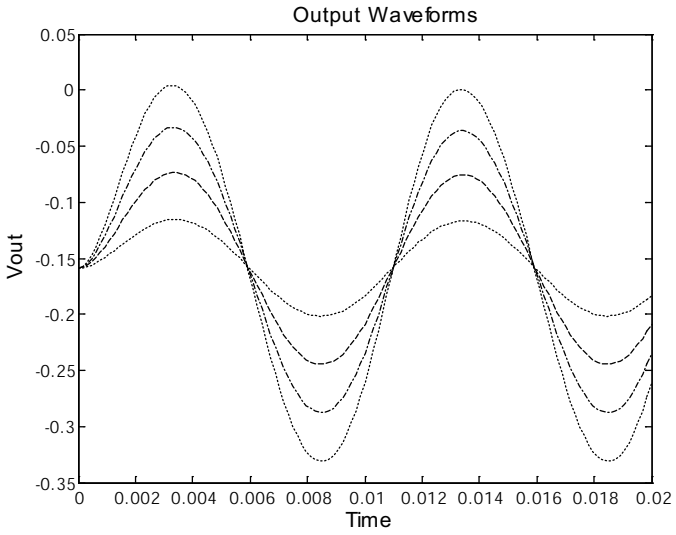


Figure 5.12: Op amp waveforms

and good stability. Though the slew rate of the amplifier is relatively decreased by the low bias current of the gain stages of the composite cascode op amp, the effect is counterbalanced by the smaller compensation capacitor. The open loop frequency response of the op amp compensated with a 3.5 pF Miller capacitor is shown in Fig. 5.13. In this case, the output load consists of a 100 pF capacitor in parallel with a 25 kΩ resistor.

5.6 Simulation and Experimental Results

The Berkeley Short-channel IGFET Model (BSIM) has been shown to be an accurate MOS transistor model in integrated circuit design. The semi-empirical model has been found to perform well for both digital and analog circuit simulations including small geometry effects. As early as 1987, Sheu et al. [46] reported good agreement between measured and model simulated results for transistors operated in both strong inversion and weak inversion regions with effective channel lengths as small as 1 μm. Research for short channel devices in the deep subthreshold region [47] showed the accuracy of short channel MOSFETs operating at currents as small as 100 pA via the BSIM model. Now, the more advanced BSIM3 model is included in CADENCE Spectre Spice Simulation which makes it applicable to modern submicron processes.

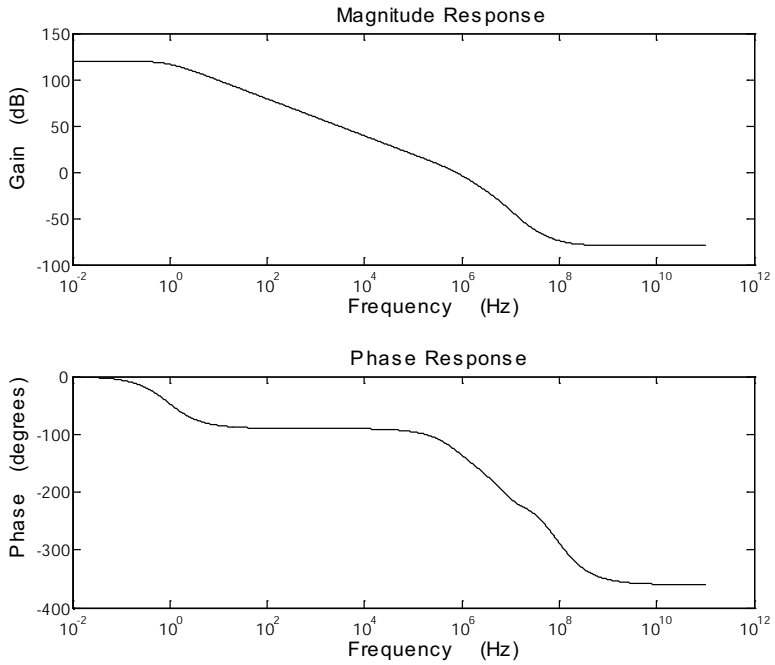


Figure 5.13: SMC compensated op amp open loop response

The proposed compact high-gain op amp is laid out in the TSMC 0.25 μm process and fabricated. CADENCE Spectre post layout simulation results along with the chip test results for this work are tabulated in Table 5.1. The slew rate and 1% settling time have been measured when the op amp is in the unity-gain feedback configuration with a 0.5 V step input. More than half of the power consumption is due to the output source follower. The input stage and second stage dissipated little power because of the low current weak inversion operating region. Using simple Miller capacitor compensation, C_c is required to be only 3.5 pF.

The micrograph of the opamp is shown in Fig. 5.14. The area of the amplifier is about 0.05 mm^2 and it could be reduced more if necessary. The simulated gain of this opamp is 120 dB. The experimental test of the open loop gain is about 117 dB. The detailed test method of the open loop gain will be presented in the next chapter.

The open loop gain of a real op amp is always finite though the gain of an ideal op amp is infinite. While open loop gain is one of the most important parameters of op amps, the other characteristics including the input offset voltage, gain

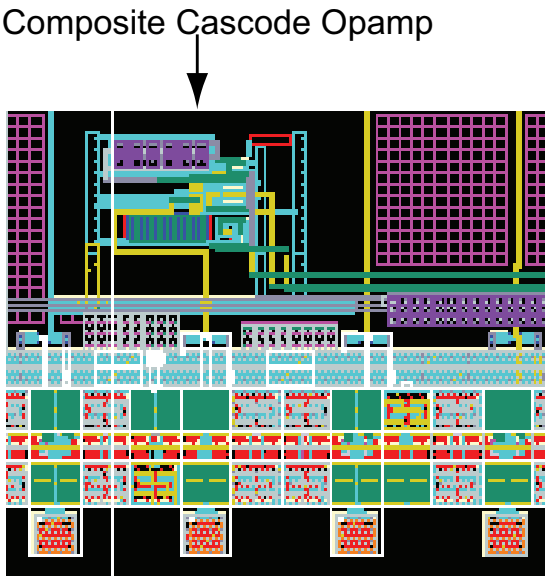


Figure 5.14: Fabricated composite cascode op amp

bandwidth product (GBW), common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), slew rate (SR), settling time (ST), phase margin (PM), and power consumption [6, 21] are all key items to represent the performance of real op amps in frequency domain and time domain. The input offset voltage is defined as the voltage required at the inputs to set the output of the op amp to zero. The low frequency op amp gain drops off at higher frequencies. As the product of the gain and bandwidth is approximately a constant, the gain of a typical op amp can trade off with the bandwidth. An op amp is usually characterized by its gain bandwidth product, which is close to the unity gain frequency. CMRR is the ratio of common mode input voltage swing to the change in input offset voltage. It is also designated as the ratio of the magnitude of the midband open loop gain to the common mode gain. PSRR is defined as the ratio of the change in power supply voltage to the change of the input offset voltage of the op amp. The slew rate is the maximum rate at which the op amp output voltage can change with an input step. The slew rate is generally determined by the rate at which the critical node inside the op amp can change voltage. Usually it is related to the current available to charge or discharge a capacitance. Settling time is defined in Chapter 3 while phase margin is defined

in Chapter 2. Power consumption is the overall power level that the op amp circuit dissipates. Low power op amp design requires micropower consumption.

For simple Miller capacitor compensation, a 3.5 pF C_c is used to produce an acceptable phase margin. The offset voltages on a sample of ten chips was found to be between 0.3 mV and 3 mV. The CMRR and PSRR are above 100 dB. The test results are quite close to the simulation results as shown in Table 5.1.

Table 5.1: Opamp Simulation Results and Test Results

	Simulation	Test
Loading	100 pF ‖ 25 kΩ	
DC Gain (dB)	120	≥ 117
GBW (MHz)	1.42	1.2
PM (°)	43	43
SR^+/SR^- (V/μs)	0.26/0.78	0.27/0.43
Ts^+/Ts^-(μs)(to 1%)	3.99/1.36	3.85/2.2
Power(μW)	110	≤ 120
Supply Voltage(V)	±1	
Capacitor (pF)	3.5	

The fabricated op amp test results show that the BSIM3 model in CADENCE Spectre Spice Simulation matches closely to the experimental results in spite of the low current weak inversion operation of the composite cascode output device. The experiment thus provides confidence in the simulation for other similar designs. A detailed chip test procedure and test methods will be presented in the following chapter.

5.7 Layout Design

This prototype design of the composite cascode op amp is implemented in the TSMC 0.25 μm process through a MOSIS research run. In analog design, matching is very important. Particularly, op amps demand very good matching for good performance with small offset and high noise rejection. The matching of analog circuits

is dependent on the size, shape, and orientation of MOS transistors [48]. In general, large transistors have more accurate matching than small transistors since the increased gate area alleviates the impact of localized variation; long channel transistors have better matching than short channel elements since longer channels decrease linewidth variation and channel length modulation. Transistors arranged in the same orientation have more precise matching than those arranged in different directions. As a result, most wider transistors in this op amp are scaled with a channel length of 1 μm. Some narrower transistors are scaled with a channel length of 2 μm to increase the active gate area for optimum matching. Symmetrical layout is necessary for analog circuits and all the stages in this op amp are laid out symmetrically and compactly. The output source follower stage with the largest power consumption is placed in a position to have even heat disperse to the input differential stage to avoid unbalanced effects. Power and ground buses are comprised of several metal layers and a wide cross section of buses is chosen to lower the resistance and keep the voltage consistent. Dummy segments are put on the ends of the resistor terminals in the bias circuit for accuracy to provide exact bias current.

Due to the issues of expense and time, my op amp design shared a test chip with another mixed signal A/D circuit. To avoid noise coupling from the digital circuitry to the delicate analog circuitry, guard rings are used to separate the sensitive analog circuits from the substrate noise coupling from the digital circuits.

5.8 Different Configurations of Various Composite Cascode Op Amp

The device sizes of the second stage could be easily adjusted to change the quiescent output voltage of the second stage for a different buffer design or to increase or decrease the gain. The total gain could be easily increased above 140 dB by adjusting the second stage device size. However, it would further lower the bandwidth and increase the settling time. The regular common source stage can also be used for relatively low gain but higher bandwidth performance. Fig. 5.15 shows the operational amplifier which implements the classical Widlar operational amplifier structure, with composite cascode differential input stage, and regular common source second stage

followed by a source follower stage. By pushing the pole of the second stage further away from the original point by using a regular common source connection instead of the gain boosting composite cascode connection, the separation of the dominant pole of the input stage from this first nondominant pole will be more desirable for compensation purpose.

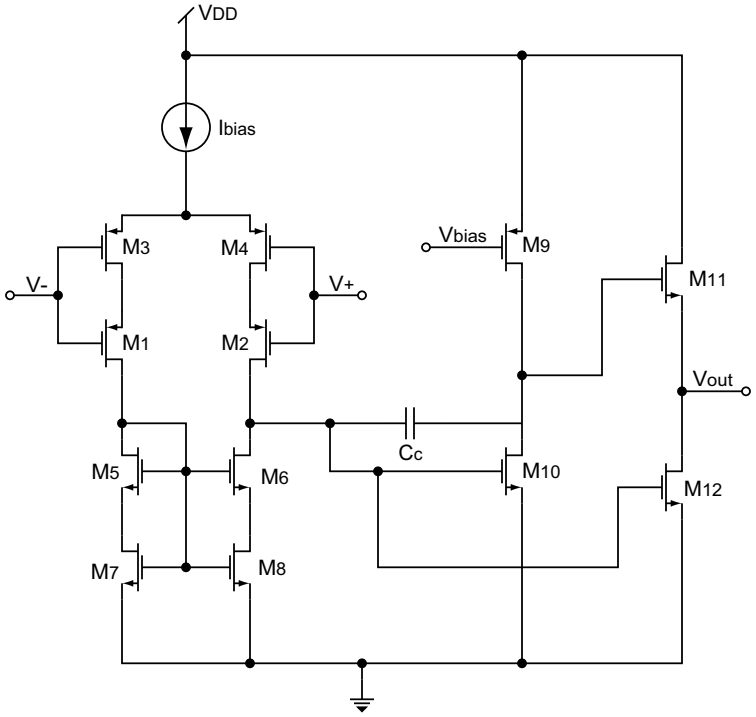


Figure 5.15: Op amp with input differential composite cascode stage and regular common source second stage

For this compact general purpose op amp, a higher or rail-to-rail output swing could be achieved by the class AB connected output buffer stage as shown in Fig. 5.16 rather than the current sink source follower stage. If the gate of M13 and the gate of M14 are directly connected to the output of the second stage, the output is a simple push pull amplifier. If voltage sources V_{GP} and V_{GN} are added between the gates and the output terminal of the second stage, higher power efficiency may be obtained by controlling the corresponding gate-to-source voltages of devices M13

and M14. The practical implementation of the voltages sources V_{GP} and V_{GN} can be realized with level shift circuits. Generally the class AB output stage requires wider devices and larger quiescent current for rail-to-rail swings, increasing the chip area.

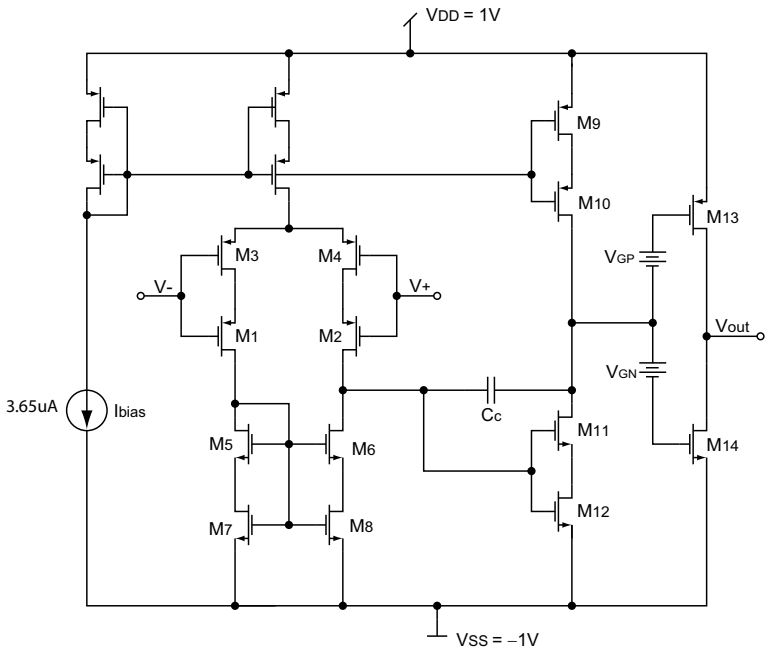


Figure 5.16: Op amp with two composite cascode gain stages and a class AB output stage

5.9 Conclusion

This work reports a low power, high gain op amp design in a 0.25 μm CMOS process using the composite cascode connection. The design follows the classic Widlar architecture. The proposed op amp produces an open loop gain above one million and shows a favorable slew rate and GBW product compared to other amplifiers driving large capacitive loads [22]. The design is fabricated as a MOSIS project chip and tested. The chip test result shows a gain of about 117 dB. In addition, the composite cascode amplifier requires a compensation capacitor of only 3.5 pF which allows a very small op amp cell. This design is intended for applications where simplicity of layout, small cell size, and low power are important. The open loop gain of this design is

comparable to bipolar op amps and exceeds all known reported CMOS designs using the classic Widlar architecture. The power supply voltage can be further reduced from 2 volt to 1.5 volt due to the freedom in biasing the subthreshold devices.

Chapter 6

Op Amp Test Procedure and Methods

6.1 Introduction

After an op amp has been designed and fabricated, the functionality test of the op amp is required to describe its performance. How to characterize op amps in frequency and time domain is a well studied topic. Simulation and experimental results to measure the open loop gain of the op amp can be found in [49–56]. The experimental measurements of the common mode rejection ratio and the power supply rejection ratio are proposed in [50,54,55]. But it becomes more difficult to measure the op amp characteristics, especially the open loop gain, as the power supplies decrease for lower voltage processes. When the multiplication of input referred noise and the open loop gain of the op amp [6, 15] exceeds the voltage level of the power supplies, it is difficult to directly measure the open loop gain of the op amp. In addition, if the signal magnitude is even smaller than the noise magnitude at the input, the output waveform would have little meaning.

The two pole model widely used in the test analysis to assess the parameters of an op amp is not accurate and may be unsuitable for gain boosting op amp designs. A more complex model with more than two poles may require tedious analysis and a large amount of calculation. Most reported op amp measurement methods require a complicated test circuit, delicate calibration, and sophisticated test instrumentation. The practical bench test of the open loop gain along with other op amp characteristics are addressed in this chapter.

The measurement of a real chip is more difficult than performing a computer simulation of the circuit. The environment in the real world is always full of noise

and interference. Special attention is needed to make sure that the test results are valid. The set up of the chip test and the debugging of the problems encountered during the test are now presented.

6.2 Power Supply Current Test and Debugging

A "functionality" test may be defined as applying an input signal to the device under test and observing the expected output. In general, the measurable parameters of the experimental design are simulated using different versions of SPICE simulators. A table of expected results could be tabulated. For example, power supply current, gain, and bandwidth for different closed loop feedback resistor ratios can be simulated, measured and compared to test results. The validity of the chip performance can then be evaluated by comparing the experimental results with the simulation results.

A specific procedure needs to be done to make sure the op amp circuit is not affected by the digital circuit on the same chip since the pure analog op amp circuit is fabricated with the A/D mixed signal circuit of another researcher on one chip. Due to the lack of pins, some of the pins are even shared between the different circuits. To make sure the test results are authentic, the A/D circuit sharing the same chip with the op amp circuit has to be turned off. One way to check whether the digital circuit has been shut down is to measure the current through the power supply and compare the current to the value given by simulation. If the two elements are close to each other, the credibility of the test board is increased.

The interconnection of the circuits is necessary for understanding the possible paths of the interference coming from the A/D circuit. Fig. 6.1 shows the placement between the op amp circuit and the A/D mixed signal circuit.

In Fig. 6.1, *gnda* denotes the analog ground while *gndd* represents the digital ground. Vcc is the analog power supply and Vdd represents the digital power supply. It is clear that the positions where the op amp circuit connects with the A/D circuit are the analog power supply Vcc and the analog ground *gnda*. Because analog ground

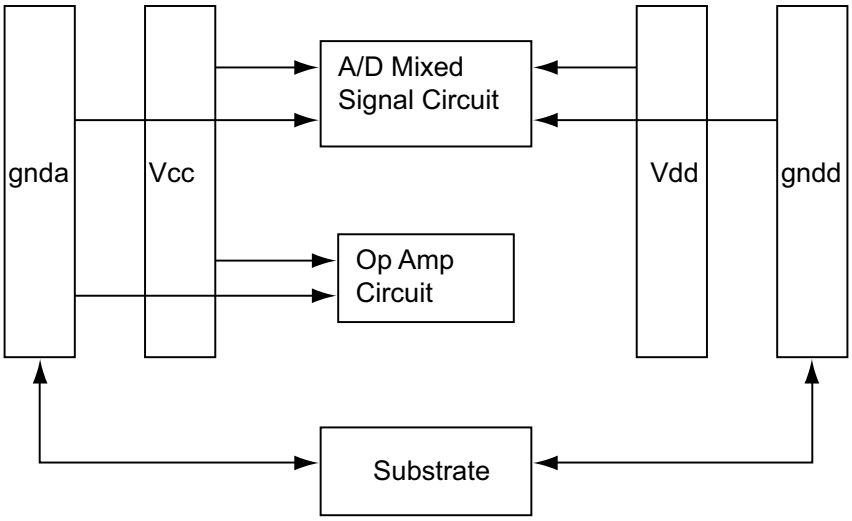


Figure 6.1: The interconnection of the chip

connects to the digital ground through the substrate, the op amp circuit is also associated to the A/D circuit through the substrate.

To see how the digital circuit affects the op amp circuit, a test circuit is set up to measure the power supply current. Fig. 6.2 is the schematic of a simple test circuit to check the possible parasitic currents. A 10 Ω resistor is placed between the negative power supply and the negative supply terminal pin of the op amp.

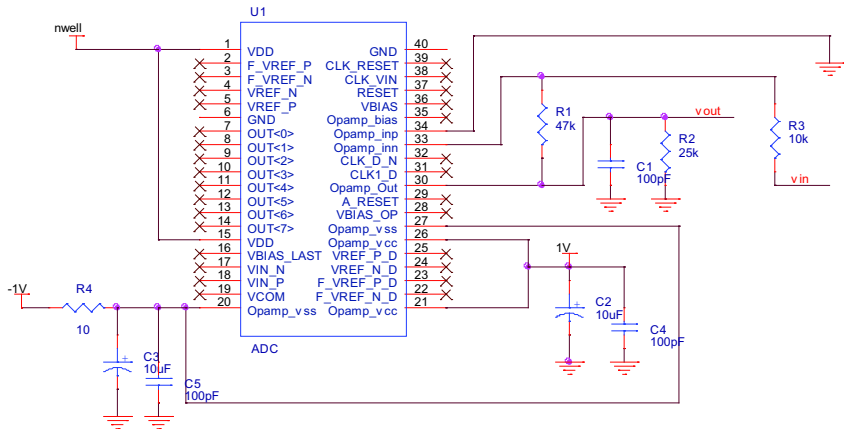


Figure 6.2: Debugging circuit setting

The pins 21 and 26 are the common analog positive supply voltage Vcc which is shared between the op amp circuit and the analog part of the mixed A/D circuit. They are tied to 1 V voltage source for the configuration of feedback op amp test. The pins 20 and 27 are the common analog negative supply voltage Vss (the P substrate of N channel device) shared between the op amp circuit and the analog part of the mixed A/D circuit. Vss is also called analog ground *gnda* in an alternative way. They are tied to -1 V source in this test circuit. The pins 6 and 40 are the digital ground of the A/D circuit. They are tied inside the chip layout to analog ground pins 20 and 27 which are used for the most negative analog supply -1 V. As a result, the analog ground is connected with the digital ground due to the common substrate in the process.

The pins 1 and 15 are the digital power supply voltage Vdd of the digital part of the mixed A/D circuit. They are tied to the nwell voltage, which changes from -1 V to 1 V during test. The current is measured by recording the voltage across the 10 Ω resistor between the -1 V dc source and the analog negative voltage terminals pins 20 and 21. By adjusting the digital supply voltage Vdd, which is also the nwell voltage, the current through the op amp circuit power supply is shown in Table 6.1. The simulated current of the op amp supply by CADENCE is around 55 μA.

Table 6.1: The test results of the current of the op amp chip

nwell voltage (Vdd)	current	if op amp functions
floating	200 μA	no
-1 V	48 mA	no
0 V	920 μA	yes
1 V	5.99 mA	yes

When the digital power supply Vdd is floating (not connected to anything), the current flowing through the 10 Ω resistor is under 200 μA (the lowest current recorded in the table). At that point, the op amp does not function. For example,

with a 100 mV sine wave input, with the feedback inverting gain at 4.7, the output waveform does not show any gain over the input. Consequently, Vdd can not be left floating.

The op amp circuit in feedback connection still does not function as an amplifier if the digital supply voltage Vdd is in the range of -1 V to -0.4 V. When Vdd gets close to - 0.3 V, the op amp circuit starts to work as a feedback amplifier with some distortion on the output waveform. The op amp circuit functions when the digital power supply Vdd is tied to the highest voltage supply 1 V as well as when Vdd is tied to the middle voltage level 0 V. When Vdd is 1 V, the current 5.99 mA is much higher than the value 920 μA measured while Vdd is set at 0 V.

After careful inspection on the layout of the whole chip, it is found that the analog op amp circuit is put on the digital part of the ESD pads used to protect the integrated circuit from electrostatic damage. The left side is the analog part of the mixed A/D circuit and the right side includes the digital part of the A/D circuit and the analog op amp circuit which should not have been surrounded by the digital ESD. The analog ESD is separated from the digital side. The ESD at the left part is connected to the analog power source and the analog ground. Instead, the ESD at the right part uses the digital power source and the digital ground. Unfortunately, the op amp circuit, which is at the bottom of the chip, is put on the digital ESD side. This explains that why the op amp could not function when Vdd is floating or connected to -1 V. Since the ESD is mainly comprised of a diode connected PMOS at the top and a diode connected NMOS at the bottom as shown in Fig. 6.3. If Vdd is set lower than the voltage level at the pad, the PMOS will be forward biased.

Even though the total current at the analog ground Vss is 5.99 mA when Vdd is tide to 1 V, most of the current might come from the digital current which is not related to the analog op amp. With the ESD circuit functions, one possible reason for this large current might come from the incomplete shut down of the A/D digital circuit. Manually turning off the digital circuit is applied to the chip under test. A sine wave with low frequency around 10 KHz is connected to the digital pin

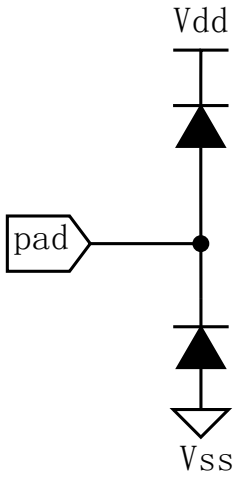


Figure 6.3: ESD circuit

Clk_vin of the A/D circuit while Vdd is kept constant at 1 V. The current at Vss was checked and found to decrease from 5.99 mA to about 160 μA. The input signal is then disconnected from the digital pin Clk_vin, the current at Vss is measured to be near 60 μA. The op amp is assumed to operate with the correct current since the measured current value is very close to the simulated value, which is 55 μA. The small difference might come from the current of the analog part of the mixed A/D circuit and the leakage current. The op amp in feedback connection is then tested and the performance is as expected. One important lesson learned here is not to put the sensitive analog circuit close to the power digital device.

6.3 Op amp Test Setup

A simple test circuit can be built by placing components on a breadboard and connecting them with jumper wires. It is convenient to get a rough estimation of the chip performance on a breadboard in a short period of time. It also saves money since the breadboard is a cheap reusable solderless device. But the noise contribution from the breadboard and wires is usually high enough to affect the behavior of the circuit experiments. The specific printed circuit board (PCB) is necessary for testing circuit designs, especially for low voltage high gain op amps which demand low noise

environment. The layout of the PCB designed for the op amp chip test is shown in Fig. 6.4.

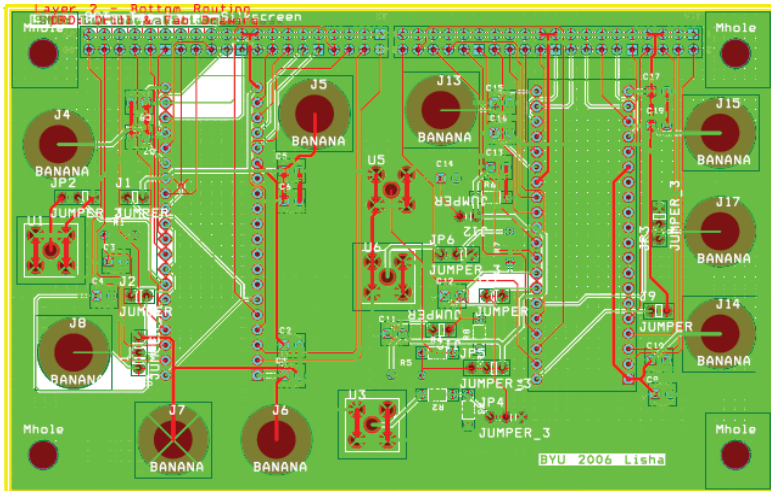


Figure 6.4: The PCB layout

Two different settings are provided on the PCB. The one on the left is the configuration set up for testing the unit feedback response. The one on the right can provide various feedback gains to measure the gain and bandwidth for the corresponding feedback factor F. Decoupling capacitors are used to reduce the fluctuation noise from the source supplies.

6.4 Op Amp Closed Loop Characteristic Test Configuration

The configuration for measuring the unit feedback response, the slew rate, the settling time, the input common-mode voltage range, and the input-offset voltage is shown is Fig. 6.5.

The input offset voltage is not only due to the small bias mismatches in design but mostly caused by device and component mismatches through fabrication. Most simulators are not capable of predicting device and component mismatches from the fabrication process. The input offset voltage is simulated to be only 37 nV by CA-

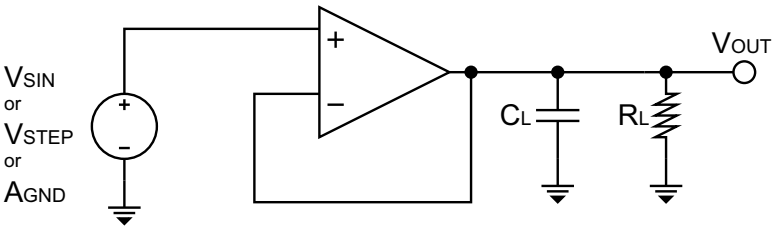


Figure 6.5: Op amp unit feedback configuration

DENCE spectre. For over 10 chips tested, the input offset voltages range from 0.3 mV to 3 mV due to the process variation.

The configuration for measuring the gain bandwidth and output voltage swing is shown in Fig. 6.6.

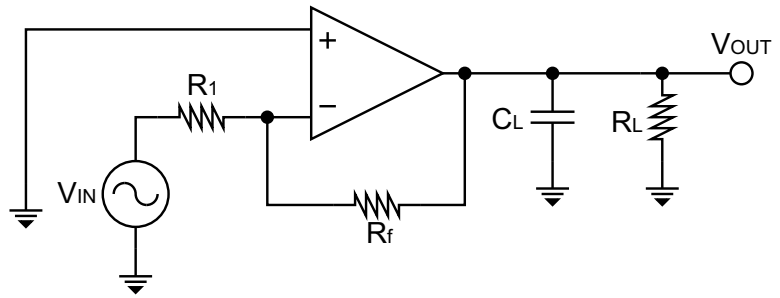


Figure 6.6: Op amp gain bandwidth configuration

The value of the resistor R_f should be large enough compared to the load resistor R_L in order not to cause significant dc current load on the output of the op amp.

6.5 Opamp Open Loop Gain Test Methods

While the closed loop properties can be easily and straightforward to test with feedback setting, measuring the open loop characteristics is much more difficult to perform. The differential gain of an op amp is quite high. A small offset voltage is generally enough to saturate the op amp to the power supply level. With the supply

voltages decreasing, even a very little input noise can drive the op amp out of the power supply limits. For the composite cascode op amp with a gain of one million at $\pm$ 1 power supplies, an input noise level as low as 1 μV is sufficient to saturate the op amp. It is hard to directly measure the open loop gain of the op amp. Suitable approaches are needed to measure the open loop gain for low voltage high gain op amp. A few test strategies are presented below along with their pros and cons.

6.5.1 Measurement Strategy One

One conventional way to check the open loop frequency response is by measuring closed loop gain phase response at various values of feedback factor F. If the measured closed loop gain phase response at different values of F could match the simulated closed loop gain phase response respectively, there is a good chance that the open loop gain phase response of the op amp under test is similar to the simulated open loop gain phase response. There might be some difference between the simulated closed loop response and the measured closed loop response due to parasitic effects and process variations. The dominant pole of the composite cascode op amp under test is only a couple of Hz after compensation by simulation. A second order op amp model can be built as shown in Eq. (3.1) if the equivalent second pole, which patterns all non-dominant higher poles into a single pole, can be found. Then, by using Eq. (2.19), the closed loop transfer function becomes

$$G_{cl}(s) = \frac{\frac{A_0}{1+A_0F}}{1+\frac{\frac{s^2}{p_1p_2}+s(\frac{1}{p_1}+\frac{1}{p_2})}{1+A_0F}}. \tag{6.1}$$

The corresponding expressions of the gain and phase of the closed loop transfer function are denoted as

$$G_{dB}(\omega) = 20\log|\frac{A_0}{1+A_0F}| - 20\log|1-\frac{\frac{\omega^2}{p_1p_2}}{1+A_0F}+j\omega\frac{(\frac{1}{p_1}+\frac{1}{p_2})}{1+A_0F}| \tag{6.2}$$

and

$$G_{phase}(\omega) = \arctan \frac{\frac{\omega(\frac{1}{p_1}+\frac{1}{p_2})}{1+A_0F}}{1-\frac{\frac{\omega^2}{p_1p_2}}{1+A_0F}}. \tag{6.3}$$

It is possible to predict the poles and the midband gain by using the experimental gain and phase of the op amp measured at different values of F. With a gain phase meter, the closed loop response can be tested and compared to the simulated response. This indirect way by employing a two pole op amp model to estimate the characteristics of the op amp is similar to the studies reported in [49,51–53,56]. Those reported measurement approaches do not fully consider the nonlinear distortion or more complete models with orders higher than two to represent the op amp behavior accurately. The two pole model works well for op amps with one low dominant pole and a second pole higher or near the unity frequency. For op amps using cascode connections or other kinds of gain boosting schemes, the second pole of the op amp will be much lower than the unity frequency. Moreover, many multistage op amps have zeros and some significant poles besides the second pole. The classical two pole model assumption does not hold for these op amps and is not capable of providing precise modeling and measurements.

In [57], more complicated models of op amps are considered and the calibration of the measurement setup [58] are presented. Most methods require a lengthy procedure of calculations, sophisticated instrumentation, and/or complicated bench setup to implement the test. In addition, most methods do not work well for CMOS devices with low power supply voltage.

To address the inaccuracy of applying the indirect modeling of feedback op amps to describe the open loop characteristics, other simple but reliable test methods of op amps using typically available bench test equipment are investigated and presented below.

6.5.2 Measurement Strategy Two

The second configuration for measuring the open loop gain is shown in Fig. 6.7.

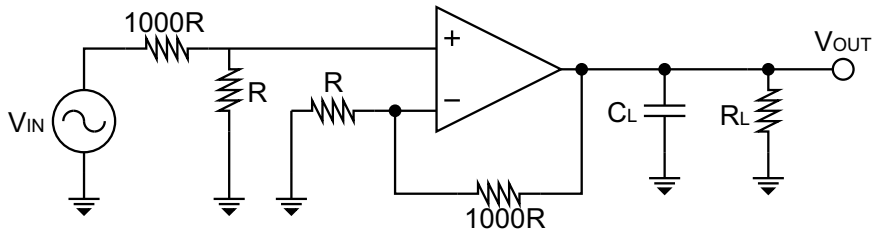


Figure 6.7: Op amp open loop gain test configuration 2

This strategy suggests measuring the open loop gain by using closed loop architecture with a voltage divider. Special care for offset cancellation needs to be applied before measurement. The offset voltage is unacceptable when a high gain op amp is under test since the offset would easily saturate the op amp. One possible solution is to use another voltage of the same magnitude and opposite polarity to cancel the offset. After mitigating the offset voltage as much as possible, the configuration shown in Fig. 6.7 is utilized to measure the open loop gain of the op amp. The voltage divider is used to attenuate the input voltage down to one thousandth or even lower magnitude while the op amp is configured with a closed loop gain around one thousand or even higher. With the measured close loop gain G and known feedback ratio F, the open loop gain could be calculated by solving equation $G = \frac{A}{1+AF}$. The closed loop gain is set between 1000 and 10000. Higher chosen closed loop gain, better error tolerance can be obtained. Clean PCB with low noise, high accuracy film resistors, and high precision signal generator that can produce low frequency signal with little distortion are necessary for this test method.

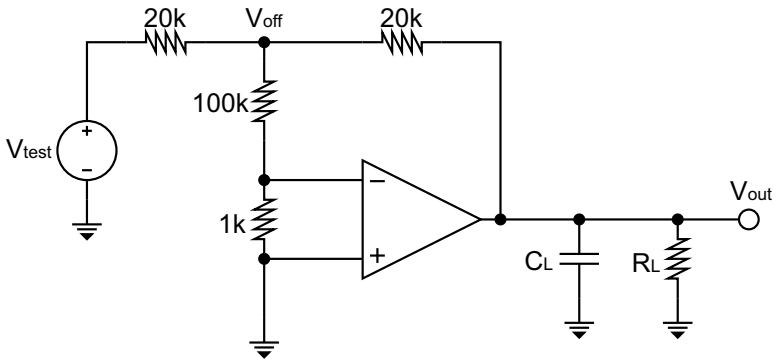


Figure 6.8: Op amp open loop gain test configuration 3

6.5.3 Measurement Strategy Three

The third configuration for measuring the open loop gain is shown in Fig. 6.8.

DC voltage V_{test} is adjusted to drive V_{out} to both the plus rail and the negative rail. V_{off} is measured at these two situations. Here V_{off} is actually the offset voltage of the op amp multiplies 100 for the setting shown in Fig. 6.8. Various values of resistors could be selected for different multiplication levels. The open loop gain of the op amp under test is then calculated by

$$\begin{aligned} A_{ol} &= \frac{\Delta y}{\Delta x} \\ &= \frac{\Delta V_{out}}{\frac{\Delta V_{off}}{100}}. \end{aligned} \tag{6.4}$$

If the measured difference of Voff at two rails is about 0.1 mV, the open loop gain of the op amp will be about 1 million. A problem of this strategy is that the noise picked up from the ESD, resistors, flicker noise, and the test board will be amplified via the op amp under test. By employing a clean PCB and more filtering, V_{off} shows less variation. This configuration could also be used to test the common mode rejection ratio and power supply reject ratio with minor adjustments on the power supply voltages. For op amps with low flicker noise, this strategy works very successfully.

6.5.4 Measurement Strategy Four

The fourth configuration for measuring the open loop gain is shown in Fig. 6.9.

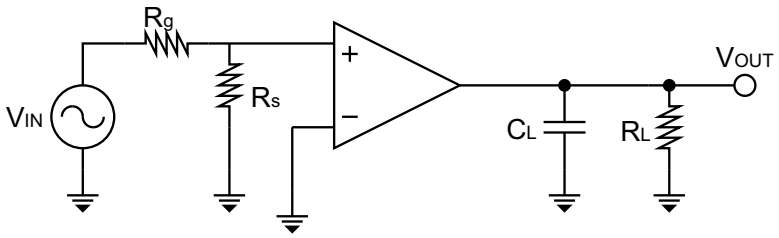


Figure 6.9: Op amp open loop gain test configuration 4

The negative terminal of op amp is connected to ground for symmetric power supplies or the common mode voltage for the single power supply. A slowly changing ramp signal with small peak voltage amplitude is applied to the positive input of the op amp. A voltage divider consisting of Rg and Rs are used to further attenuate the input signal in order to get more accurate measurement of the open loop gain without the slew rate limit effect. Comparing the slope of the output signal to that of the input ramp, the open loop gain can be calculated by

$$\begin{aligned} A_{ol} &= \frac{\Delta V_{out}}{\Delta V_{in}} \\ &= \frac{\frac{\Delta V_{out}}{\Delta x}}{\frac{\Delta V_{in}}{\Delta x}}. \end{aligned} \tag{6.5}$$

The benefit of this test strategy is that the signal level could be set higher without worrying about the output reaching the rail voltage since the slope of the active range rather than the absolute voltage amplitude is the parameter to be measured. This method is more robust to noise than the other approaches discussed.

6.6 Composite Cascode Op Amp Chip Test Results

The supplies of 1 V and -1 V are applied to the op amp chip. The power consumption of the chip is around 120 μW based on the supply current which is measured to be close to 60 μA. The offset voltages on a sample of ten chips was found to be between 0.3 mV and 3 mV. The output load of the op amp consists of a 100 pF capacitor in parallel with a 25 kΩ resistor. The CMRR and PSRR are measured to be above 100 dB. The main test results are summarized in Table 6.2.

Table 6.2: Opamp Test Results

DC Gain (dB)	≥ 117
GBW (MHz)	1.2
PM (°)	43
SR^+/SR^- (V/μs)	0.27/0.43
Ts^+/Ts^-(μs)(to 1%)	3.85/2.2
Power(μW)	≤ 120
Supply Voltage(V)	± 1

The open loop gain, the most important performance parameter of the op amp chip, has been measured with all four strategies mentioned in this chapter. Strategy one provides confidence of the test chip due to the close match between the measurement data and the simulation curves. But the exact estimation of the open loop gain could not be attained from this method because of the inaccurate transfer function modeling. Strategy two assesses the open loop gain to be above 90 dB. The lack of high precision signal generator that can produce low frequency signal with little distortion prevents the more accurate evaluation of the open loop gain. A spectrum analyzer plot shows the signal generator available in the analog lab produces a low frequency signal with significant harmonic distortion. Strategy three estimates the op amp gain to be above 100 dB. However, the more precise measurement of the gain is not possible due to the noise of the test chip, which is presented as the fluctuation of the amplified offset voltage. The result of 117 dB open loop gain is

given by strategy four because the measurement of the slope instead of the magnitude value is more robust to noise. Using a voltage divider to decrease the input signal to get an exact measurement of the open loop gain will eventually be limited by the input noise floor of the test chip. The extremely low signal noise ratio leads to the corruption of the output signal slope. The further evaluation of the op amp open loop gain as the expected 120 dB is prohibited by the considerable flicker noise of the MOSFET device. Nevertheless, the adequately close match between the op amp chip experimental results and the CADENCE Spectre Spice Simulation demonstrates that the prototype chip has achieved the expected performance in the case of low current weak inversion operation of the composite cascode output device.

6.7 Conclusion

Detailed test set up, debugging, and test methods implemented to describe the op amp performance are presented in this chapter. It discusses the increasing challenge to measure the high gain op amp characteristics when the power supplies are getting smaller. Several simple bench test methods are investigated and proposed to characterize the op amp characteristics, in particular the open loop gain. Those practical techniques do not require sophisticated instrumentation or a complicated lab setup. The requirements and the suitability of the different measurements in various situations are also evaluated.

Chapter 7

Conclusion and Future Research

Compensation methods of op amps are investigated along with their pros and cons in order for designers to have a guide to choose the approach suitable for different situations. This dissertation proposes a creative feedforward compensation method which overcomes the serious drawback of bandwidth narrowing by the widely used pole-splitting method. It can improve the phase margin as well as optimize the bandwidth of the op amp. The feedforward method can be easily applied to the existing popular two gain stage op amp architectures with very little alteration. The mathematical derivation and circuit simulation demonstrate the advanced properties and improved performance of this feedforward compensation technique.

This proposed innovative feedforward compensation method of op amps is explored by a creative mixed mode design methodology. This design approach combines intuition, mathematical analysis, and mixed level simulation. The mixed level simulation is comprised of both system level simulation and device level simulation for some critical analog circuit path. In this way, the behavior of new design ideas can be verified in an effective way as well as providing sufficient accuracy to predict the circuit performance realistically.

With the growing demand for low power mixed signal integrated circuits for portable or nonportable high performance systems, analog circuit designers are challenged with making analog circuit blocks with lower power consumption with little or no performance degradation. The classic Widlar op amp architecture, originally developed for the BJT, has required modification for use with CMOS devices. In particular, it has proved difficult to match the open loop gain of bipolar op amps with

CMOS technology. This is due to the inherently lower transconductance of CMOS devices as well as the gain reduction due to short channel effects that come into play for submicron CMOS processes. A feasible configuration of a high gain low power op amp following Widlar architecture is proposed. This op amp uses composite cascode connections for the differential input, a common source second stage, and a current mirror. By selecting the appropriate current and choosing the $\frac{W}{L}$ aspect ratios of transistors wisely, some MOS devices operate in subthreshold range while the remainder work in the active range.

A prototype of the composite cascode op amp has been laid out and fabricated in a 0.25 μm CMOS process. The fabricated op amp test results show that the BSIM3 model in CADENCE Spectre Spice Simulation matches closely to the experimental results in spite of the low current weak inversion operation of the composite cascode output device. The experiment thus provides confidence in the simulation for other similar designs.

The experimental measurement of the op amp open loop characteristics becomes more difficult as the power supply voltage decreases. When the multiplication of input referred noise and the open loop gain of the op amp exceeds the voltage level of power supplies, it is difficult to directly measure the open loop gain of the op amp. A few viable techniques are proposed to measure the op amp open loop parameters using typically available bench test equipment.

7.1 Contributions

Several significant contributions have been made to op amp compensation and high gain low power op amp design in this dissertation. The main contributions of this dissertation are summarized in this section.

7.1.1 Current Compensation Methods Investigation

Although amplifier compensation has been a well-studied topic in analog circuit design for many years, an up-to-date comparison and investigation of modern

compensation methods is periodically required to check the classical methods against modern processes. This survey summarizes some popular compensation methods of the op amp and points out their advantages and disadvantages. A guide to using different compensation methods based on the primary requirements and output load is given.

7.1.2 Feedforward Compensation Method

This proposed feedforward compensation method is fully compatible with the classical general purpose operational amplifier configuration. This architecture also has the advantage of stabilizing the op amp without reducing the bandwidth as much as most commonly used compensation methods do.

7.1.3 System-Level and Combined Device/Transfer Function Simulation Methodology

A design method which integrates intuition, mathematical derivations, system level simulations, and combined device/transfer function simulations is introduced. The proposed system-level and device-level mixed-mode simulation can give insights of creative thoughts, simplify the analysis by using ideal blocks for some circuitry while providing necessary device model properties.

7.1.4 Stability Analysis of the Feedforward Architecture

A closed loop stability criteria is derived and a design guide line for maximally flat frequency response is suggested to provide circuit stability. Mathematical derivations along with simulation results are presented to correlate the theory with the implementation.

7.1.5 MOSFET in Subthreshold Inversion Used for Low Power Op Amp Designs

Operating a MOSFET in the weak inversion region or subthreshold region is very useful for low power applications. A wise choice of the quiescent current as well

as the proper $\frac{W}{L}$ aspect ratios of the transistors can make some of the devices operate in strong inversion region while other devices operate in the subthreshold region. The appropriate selections of these values are critical for the function of the circuits. A current mirror using the composite cascode connection is also proposed to bias the circuit.

7.1.6 Architecture of A High gain Composite Cascode Operational Amplifier

A two-gain stage op amp which consists of a differential input composite cascode stage operating at a bias current of 3.65 μA and a common source composite cascode second stage provides an open loop gain around 120 dB with 110 μW power consumption. With the high output impedance and the low current of the composite cascode connections, a high gain stage is possible with small chip area and power dissipation. This high impedance load also leads to flexible and simple compensation schemes. A phase margin of 43° is achieved using conventional Miller compensation with a capacitor of only 3.5 pF while driving a 100 pF load.

The design follows the classic Widlar architecture. The proposed op amp produces an open loop gain of one million and shows a favorable slew rate and GBW product compared to other amplifiers driving large capacitive loads. This design is intended for applications where simplicity of layout, small cell size, and low power are important. The open loop gain of this design is comparable to bipolar op amps and exceeds all known reported CMOS designs using the classic Widlar architecture. The power supply voltage can be further reduced from 2 volt to 1.5 volt due to the freedom in biasing the subthreshold devices.

7.1.7 Modified Composite Cascode Operational Amplifiers for Different Applications

The proposed op amp which employs composite cascode connections for both differential input stage and second gain stage along with a source follower output stage could be easily modified to adapt to different operating conditions. The second stage

could be implemented with a regular common source stage to increase the bandwidth. The source follower stage could be replaced with a class AB output stage for rail to rail output swing.

7.1.8 Practical Test Methods of High Gain Op Amps

It is well known that it becomes more difficult to measure the op amp characteristics, especially the open loop gain, as the power supplies decrease for compatibility with modern low voltage processes. When the multiplication of input referred noise and the open loop gain of the op amp exceeds the power supply voltage, it is difficult to directly test the open loop gain of the op amp. In addition, if the signal magnitude is even smaller than the noise magnitude at the input, the output waveform would have little meaning. This work deals with the practical bench test of the open loop gain of the op amp and presents several simple but reliable test methods of op amp open loop gain using typically available bench test equipment.

7.2 Future Research

This dissertation has explored the area of op amp compensation approach, high gain low power op amp design, and practical op amp open loop gain test methods. Due to the nature of the wide research topic, there are still several topics for future work. For example, the high gain composite cascode stage was used in this work as a gain element for classic op amp design. Other applications of this stage could also be explored, especially in light of the demonstrated ability to accurately model the stage using conventional BSIM3 models.

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