Nano-scale CMOS and Low Voltage Analog to Digital Converter Design Challenges

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Abstract

This paper discusses the analog performance trend and the performance estimation of pipeline ADC in nano-scale CMOS era. The technology scaling is effective to increase the conversion rate, however it is not effective to increase the resolution, SNR, and decrease the power consumption at higher resolution. New converter design challenge is needed and one strong candidate must be the successive approximation ADC because it does not require operational amplifiers that consume power and become difficult to design with nano-scale CMOS.

1. Introduction

The prospect of analog to digital converters (ADC) has been increasing continuously along with the progress of digital systems. The performance of ADC will determine the ultimate performance of digital systems, such as data-rate, sensitivity, signal dynamic range, bit error rate, and power consumption. ADCs should be embedded into SoC, however the progress of analog performances can not be guaranteed by the technology scaling in contrast to digital performances. This paper discusses the relationship between CMOS technology scaling and the performance of ADCs and recent ADC design challenges.

2. Technology scaling and analog performance

Technology scaling has enabled the use of CMOS technology for radio frequency applications recently that has been believed the kingdom of bipolar technology.

The peak cutoff frequency of MOS transistor f_{Tmax} is approximately given by

$$f_{T\,max} \approx \frac{v_{sat}}{2\pi L}, \qquad (1)$$

where v_{sat} is a saturation career velocity and L is the channel length of MOS transistor. Cutoff frequency is inversely proportional to the channel length and will reach about 200 GHz at 65 nm node. However, the most serious present and future issue must be the operating voltage lowering. According to recent ITRS technology load map, the maximum operating voltage around 1 V will be expanded to 45 nm node future scaled devices [1]. This value is higher compared with the past ITRS technology load map's value however the realization of high SNR analog circuit is still difficult.

The SNR of the differential sample and hold circuit is

$$SNR = \frac{CV_{pp}^{2}}{4kT}, \qquad (2)$$

where C is the sampling capacitor, V_{pp} is the differential peak voltage of sinusoidal signal, k is the Boltzmann's constant, and T is the absolute temperature. Because of SNR decreases with a decrease of signal amplitude, the larger capacitances are needed to keep the same SNR at the low operating voltage and results in an increase of the power consumption or decrease of the signal bandwidth.

The head room issue where a lot of transistors cannot be piled for a low operation voltage analog circuit becomes more serious. Also MOS switches will make serious problem. CMOS switches have the source node connected to the input terminal and the on-resistance takes largest value when the signal voltage is about half operating voltage.

Another issue is the reduction of the amplifier's gain caused by the reduction of a drain resistance. Figure 1 shows that the Early voltage of NMOS transistors V_A for the several design rules versus the drain to source voltage V_{ds} when the channel length is 1.1x of minimum length. The drain resistance r_{ds} can be expressed as,

$$r_{ds} = \frac{V_A}{I_{ds}}. \qquad (3)$$

The intrinsic voltage gain G_i is,

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$$G_i = g_m \cdot r_{ds} = \frac{2V_A}{V_{eff}}, \qquad (4)$$

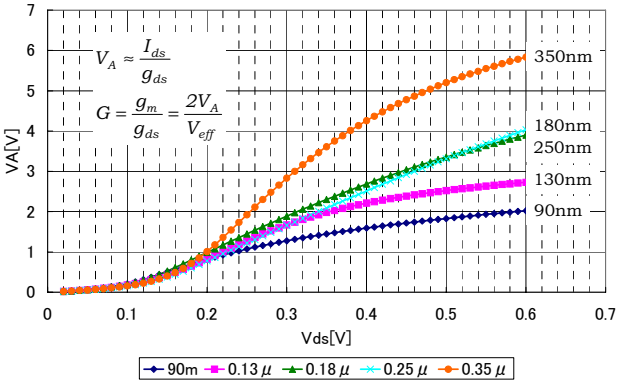

Fig. 1 V_A vs. V_{ds} for several design rules.

where g_m is the trans-conductance and V_{eff} is the effective gate voltage. Therefore higher V_A is needed to obtain higher gain. The V_A decrease with decreasing the design rule. The transistor gain of the 90 nm NMOS transistor is about 10 at most and three times lower than that of 350 nm NMOS. Then the design of the high gain amplifier with scaled CMOS process is quite tough compared with that with conventional 350 nm CMOS process.

3. Technology scaling and ADC performance

Several-hundred MHz conversion speed and 10 bit to 14 bit resolution ADC must be needed for the future cellular phone systems and the wireless LAN systems. Therefore pipeline ADC architecture, that uses comparators and accurate switched capacitor amplifiers to convert the input analog signal to the digital values with a few bits per clock in a pipeline fashion must be the strong candidate, as for.

Figure 2 shows that the conversion frequency versus the power consumption of published 10 bit, 12 bit, and 14 bit pipeline ADCs and some sigma delta ADCs. A higher resolution ADC consumes much power; however its conversion frequency is low. The maximum conversion frequency is about 200 MHz and the normalized power consumption by the conversion frequency is about 0.3 mW/MHz (FoM is 500 fJ/conv. steps) for the 10 bit pipeline ADC. Since the ADC is the most important analog core block for the future wireless systems, this paper will discuss the fundamental performance limitation and estimation with respect to the technology scaling.

A pipeline ADC consists of cascade connection of a unit amplifier and can be modeled using the parasitic input capacitance C_{pi}, the parasitic output capacitance C_{po}, and the trans-conductance g_m, as shown in Figure 3 [2].

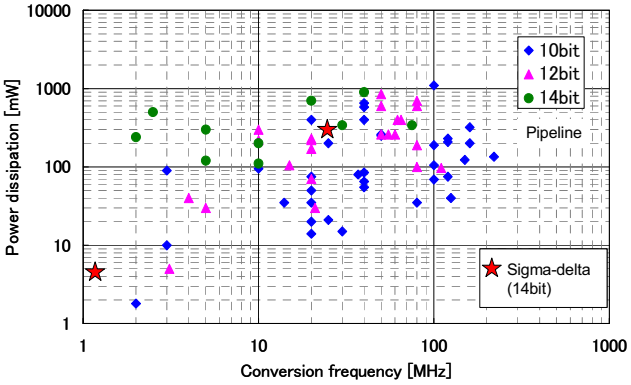

Fig. 2 power dissipation vs. conversion frequency for 10 bit, 12 bit, and 14 bit ADCs.

The closed-loop bandwidth can be derived as,

$$GBW_{\_close} = \frac{g_m}{2\pi C_o} \frac{1}{\left(2+\frac{C_{pi}}{C_o}\right)\left(1+\frac{C_{po}}{C_o}\right)+\left(1+\frac{C_{pi}}{C_o}\right)}, \qquad (5)$$

where C_o stands for signal capacitances C_s and C_f.

The conversion frequency of the ADC fc is,

$$f_c \approx \frac{3 \cdot GBW_{close}}{N}, \qquad (6)$$

where N is the resolution. Thus the higher GBW_{close} is needed for the higher conversion frequency.

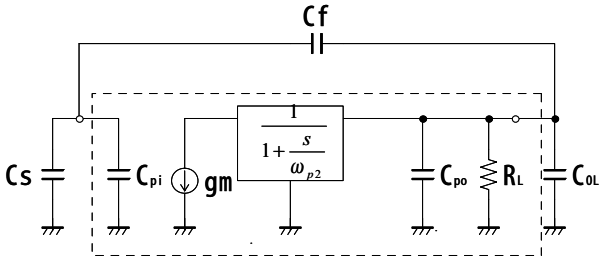

Fig. 3 Equivalent circuit model of pipeline ADC.

The parasitic input and output capacitances, C_{pi} and C_{po} depend on the used design rule and proportional to the operating current when V_{eff} keeps same value. Thus, $C_{pi} = \alpha_{pi} \cdot I_{ds}$ and $C_{po} = \alpha_{po} \cdot I_{ds}$ and equation (5)

can be modified as,

$$GBW_{\_close} = \frac{I_{ds}}{2\pi C_o V_{eff}} \frac{1}{\left(2+\frac{\alpha_{pi} I_{ds}}{C_o}\right)\left(1+\frac{\alpha_{po} I_{ds}}{C_o}\right)+\left(1+\frac{\alpha_{pi} I_{ds}}{C_o}\right)}. \quad (7)$$

The coefficients for the parasitic input and output capacitance, C_{pi} and C_{po} are decreasing with the decrease of design rule as shown in table 1, where these capacitances have been obtained by SPICE simulation for conventionally foundry processes under the assumption that the V_{eff} is 0.175V. The unit for these capacitances is fF/mA for C_{pi}, C_{po}, fF for C_o and V for V_{pp}. The coefficients become half along with one technology generation advance.

Table 1. Design rule and capacitances.

DR	C_{pi_N}	C_{pi_P}	C_{po}	C_o (10b)	V_{pp}
350	303	1034	892	20.4	5.2
250	236	662	832	43	3.6
180	115	475	340	114	2.2
130	66	249	168	215	1.6
90	24	94	95	552	1.0

Figure 4 shows estimated maximum conversion frequency from 8 to 14 bit ADCs as a function of the sink current for the input MOS transistor in the first stage operational amplifier for the several design rules such as 350 nm, 250 nm, 180 nm, 130 nm, and 90 nm.

The maximum differential signal voltage is assumed two times larger voltage that is 0.7 V subtracted from the maximum power supply voltage for each design rules.

$$C_o(pF) \geq 5.28 \times 10^{-7} \times \left(\frac{2^N}{V_{pp}}\right)^2 . \quad (8)$$

C_o is determined by needed capacitance to realize 3dB lower SNR than the ideal value.

The characteristics curve is convex and takes the highest value at the certain sink current. In the region of the current being less than this value, the conversion frequency increases with an increase of the sink current.

There are two reasons for this. At first, the g_m is proportional to the sink current, and the parasitic capacitances are smaller than the signal capacitance. At around the peak, at least one of the parasitic capacitances becomes equal to the signal capacitance. In the region of the current being larger than that value, both parasitic capacitances become larger than the signal capacitance and the conversion frequency will decrease with an increase of the sink current.

Estimated performance curves exhibit interesting results in terms of the relation ship between the performances and the design rules. For the 8 bit resolution, the case of 130 nm CMOS process is the fastest in low current operation, but the case of 90 nm CMOS process attains the highest conversion frequency. For the 10 bit resolution, the case of 350 nm CMOS process is faster than the other processes in the ultra low power region, and the finer design rule gets better for the high frequency conversion along with an increase of the sink current. The case of 350 nm CMOS process takes the best position for 12 bit or 14 bit resolutions, in terms of the high speed conversion and the low power consumption. For the lower resolution, the signal capacitance is smaller and the use of the fine design rule transistors is effective to reduce the parasitic capacitances. However to achieve the higher resolution, the signal capacitance when using the fine design rule transistors increases to keep high SNR with small signal swing. In this case, the reduction of parasitic capacitance is not effective any more.

Furthermore, the higher resolution pipeline ADC requires the higher gain of OP amp, of which value is,

$$G(dB) > 6N + 10 , \quad (9)$$

where N is the resolution. Thus 14 bit ADC needs the gain of 94 dB at least. This value is not easy to realize for 90 nm CMOS technology.

4. Design challenges for high-speed ADCs

Further performance improvement for pipeline ADC looks very difficult, in particular for high resolution ADC. Design challenges for high speed ADC has started recently. Basic idea for this new design challenge is no use of the operational amplifiers (OP. amp.)

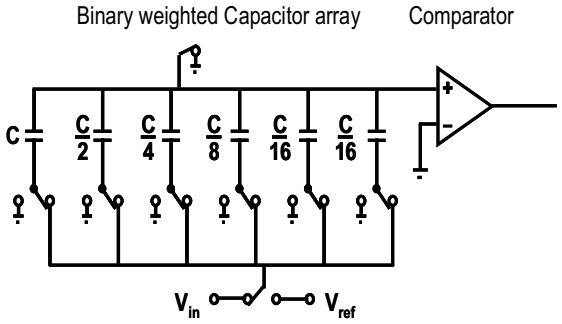

Fig. 5. Successive approximation ADC.

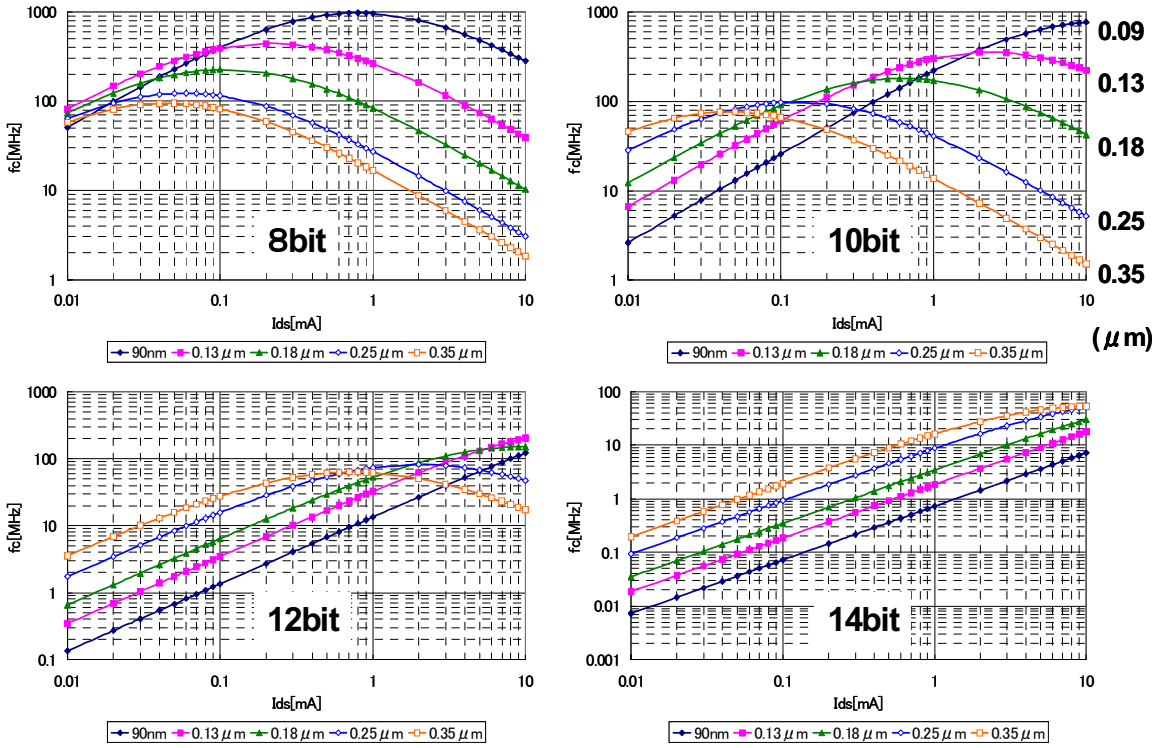

Fig. 4. Coversion frequency vs. operating current in input stage for several resolutions and design rules.

The OP. amp. is very effective to realize several analog operations, in particular, analog pipeline operation. Also, it can relax the requirement for the mismatch of comparators that is the essential part of ADCs.

However it becomes quite difficult to realize high performance OP. amp. along with technology scaling. Gain and signal dynamic range become lower and lower. Now many designers are looking for the suitable conversion architectures for nano-scale CMOS era.

One candidate is the successive approximation ADC shown in Fig. 5. Needed analog operations can be done with only capacitors, switches, and a small number of comparators. The quiescent current, which is needed for the comparator is very small or can be designed to be zero. Thus the power consumption is determined by the dynamic current like digital circuits. Signal swing can be made larger than that of OP. amp.-based design. Full swing operation is possible and results in a decrease of capacitance. Thus ultimate low power operation must be realized.

The biggest issue is the operating speed, however asynchronous operation and parallel scheme can address to this issue. Furthermore technology scaling is effective to increase the conversion frequency and decreasing power dissipation like digital circuits. 260 fJ/ conv.-steps (6 b, 600 MS/s) [3], 220 fJ/conv.-steps (6 b, 600 MS/s) [4], and 165 fJ/ conv.-steps (12 b, 100 KS/s) [5] have been reported. While It is 500 fJ/ conv.-steps for conventional 10 b pipeline ADC.

5. Summary

Technology scaling is effective to increase the conversion rate, however is not effective to increase the resolution, SNR, and to decrease the power consumption at the higher resolution. New ADC design challenge is needed and one strong candidate is the successive approximation ADC because it does not require operational amplifiers that consumes power and becomes difficult to design with nano-scale CMOS.

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