

Analog-to-Digital Converter Architectures and Choices for System Design

By Brian Black

How important are the differences between sigma-delta and successive-approximation architectures in choosing an analog-to-digital (A/D) converter? They can often be an important factor in initiating the selection of a converter for a specific application. We describe here four major circuit architectures used in A/D converter (ADC) design and outline the role they play in converter choice for various kinds of applications. The descriptions are augmented by three examples that illustrate tradeoffs and issues associated with architectural considerations.

Though not detailed or exhaustive, this overview is intended to raise issues that should be understood when considering converters of different architectures. Sources of more-detailed information on converter architectures can be found in the *References* and at Internet sites indicated at appropriate points. As one might expect in a survey of this kind, these descriptions are not comprehensive; and variations within each of the architecture families make generalizations less than fully accurate. Nevertheless, such generalizations are useful for the system designer to keep in mind when conducting a high level overview of a proposed system's requirements.

CONVERTER ARCHITECTURES

An overwhelming variety of ADCs exist on the market today, with differing resolutions, bandwidths, accuracies, architectures, packaging, power requirements, and temperature ranges, as well as hosts of specifications, covering a broad range of performance needs. And indeed, there exists a variety of applications in data-acquisition, communications, instrumentation, and interfacing for signal processing, all having a host of differing requirements.

Considering architectures, for some applications just about any architecture could work well; for others, there is a "best choice." In some cases the choice is simple because there is a clear-cut advantage to using one architecture over another. For example, pipelined converters are most popular for applications requiring a throughput rate of more than 5 MSPS with good resolution. Sigma-delta converters are usually the best choice when very high resolution (20 bits or more) is needed. But in some cases the choice is more subtle. For example, the sigma-delta AD7722 and the successive-approximations AD974 have similar resolution (16 bits) and throughput performance (200 kSPS). Yet the differences in their underlying architectures make one or the other a better choice, depending on the application.

The most popular ADC architectures available today are *successive approximations* (sometimes called SAR because a *successive-approximations (shift) register* is the key defining element), *flash* (all decisions made simultaneously), *pipelined* (with multiple flash stages), and *sigma-delta* ($\Sigma\Delta$), a charge-balancing type. All A/D converters require one or more steps involving comparison of an input signal with a reference. Figure 1 shows qualitatively how

flash, pipelined, and SAR architectures differ with respect to the number of comparators used vs. the number of comparison cycles needed to perform a conversion.

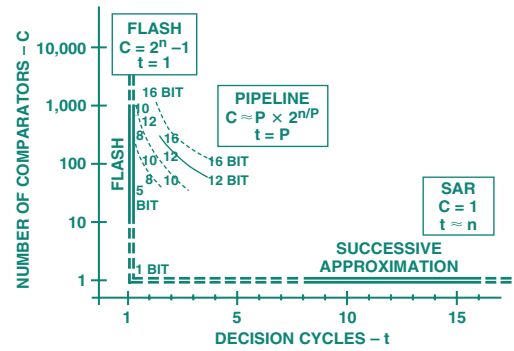


Figure 1. Tradeoff between decision cycles and comparators.

FLASH CONVERTERS

Conceptually, the *flash* architecture (illustrated in Figure 2) is quite straightforward: a set of $2^n - 1$ comparators is used to directly measure an analog signal to a resolution of n bits. For a 4-bit flash ADC, the analog input is fed into 15 comparators, each of which is biased to compare the input to a discrete transition value. These values are spaced one least-significant bit (LSB = FS/ 2^n) apart. The comparator outputs simultaneously present $2^n - 1$ discrete digital output states. If for example the input is just above 1/4 of full scale, all comparators biased to less than 1/4 full scale will output a digital "1," and the others will output a digital "0." Together, these outputs can be read much like a liquid thermometer. The final step is to level-decode the result into binary form.

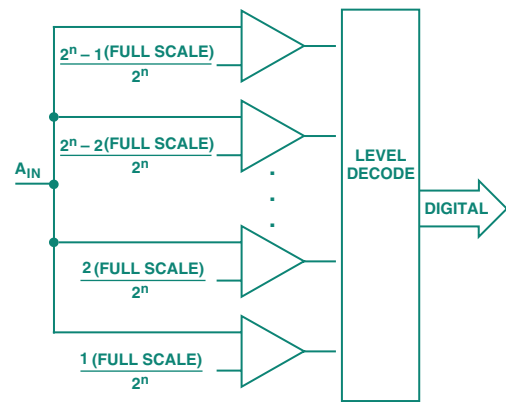


Figure 2. Basic flash architecture.

Design Considerations and Implications: The flash architecture has the advantage of being very fast, because the conversion occurs in a single ADC cycle. The disadvantage of this approach is that it requires a large number of comparators that are carefully matched and properly biased to ensure that the results are linear. Since the number of comparators needed for an n -bit resolution ADC is equal to $2^n - 1$, limits of physical integration and input loading keep the maximum resolution fairly low. For example, a 4-bit ADC requires 15 comparators, an 8-bit ADC requires 255 comparators, and a 16-bit ADC would require 65,535 comparators! For more about flash ADCs, see http://www.analog.com/support_standard_linear/seminar_material/practical_design_techniques/Section4.pdf.

PIPELINED ARCHITECTURE

The *pipelined* (or pipelined-flash) architecture effectively overcomes the limitations of the flash architecture. A pipelined converter divides the conversion task into several consecutive stages. Each of these stages, as shown in Figure 3, consists of a sample-and-hold circuit, an m -bit ADC (e.g., a flash converter), and an m -bit D/A converter (DAC). First the sample and hold circuit of the first stage acquires the signal. The m -bit flash converter then converts the sampled signal to digital data. The conversion result forms the most significant bits of the digital output. This same digital output is fed into an m -bit digital-to-analog converter, and its output is subtracted from the original sampled signal. The residual analog signal is then amplified and sent on to the next stage in the pipeline to be sampled and converted as it was in the first stage. This process is repeated through as many stages as are necessary to achieve the desired resolution. In principle, a pipelined converter with p pipeline stages, each with an m -bit flash converter, can produce a high-speed ADC with a resolution of $n = p \times m$ bits using $p \times (2^m - 1)$ comparators. For example, a 2-stage pipelined converter with 8-bit resolution requires 30 comparators, and a 4-stage 16-bit ADC requires only 60 comparators. In practice, however, a few additional bits are generated to provide for error correction. For more about pipelined ADCs, See http://www.analog.com/support/standard_linear/seminar_material/practical_design_techniques/Section4.pdf.

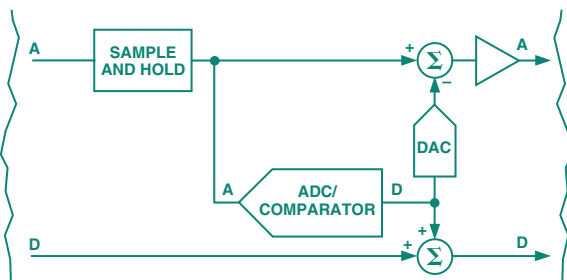


Figure 3. A single pipelined converter stage.

Design Considerations and Implications: Pipelined converters achieve higher resolutions than flash converters containing a similar number of comparators. This comes at the price of increasing the total conversion time from one cycle to p cycles. But since each stage samples and holds its input, p conversions can be underway simultaneously. The total throughput can therefore be equal to the throughput of a flash converter, i.e., one conversion per cycle. The difference is that for the pipelined converter, we have now introduced *latency* equal to p cycles. Another limitation of the pipelined architecture is that the conversion process generally requires a clock with a fixed period. Converting rapidly varying non-periodic signals on a traditional pipelined converter can be difficult because the pipeline typically runs at a periodic rate.

SUCCESSIVE APPROXIMATIONS

The successive-approximations architecture can be thought of as being orthogonal to the flash architecture. While a flash converter uses many comparators to convert in a single cycle; a SAR converter, shown in Figure 4, conceptually uses a single comparator over many cycles to make its conversion. The SAR converter works like an old-fashioned balance scale. On one side of the scale, we place the sampled unknown quantity. On the other side, we place a weight (generated by the SAR and DAC) that has the value of $1/$

2 of full-scale and compare the two values. This first weight represents the most significant bit (MSB). If the unknown quantity is larger, the $1/2$ -scale weight is retained; if the unknown quantity is smaller, it is removed. This series of steps is repeated n times, using successively smaller weights in binary progression (e.g., $1/4$, $1/8$, $1/16$, $1/32$, \dots $1/2^n$ of full scale) until the desired resolution, n , is attained. Each weight represents a binary bit, with the largest representing the most significant bit, and the smallest representing the least significant bit.

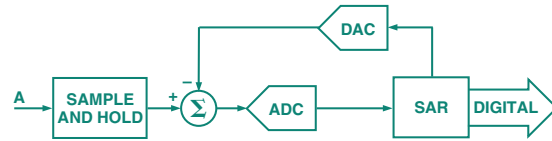


Figure 4. Successive-approximations architecture.

Design Considerations and Implications: A SAR converter can use a single comparator to realize a high resolution ADC. But it requires n comparison cycles to achieve n -bit resolution, compared to p cycles for a pipelined converter and 1 cycle for a flash converter. Since a successive-approximations converter uses a fairly simple architecture employing a single SAR, comparator, and DAC, and the conversion is not complete until all weights have been tested, only one conversion is processed during n comparison cycles. For this reason, SAR converters are more often used at lower speeds in higher-resolution applications. SAR converters are also well suited for applications that have non-periodic inputs, since conversions can be started at will. This feature makes the SAR architecture ideal for converting a series of time-independent signals. A single SAR converter and an input multiplexer are typically less expensive to implement than several sigma-delta converters. With dither noise present, SAR and pipelined converters can use averaging to increase the effective resolution of the converter: for every doubling of sample rate, the effective resolution improves by 3 dB or $1/2$ bit.

One consideration when using a SAR or pipelined converter is *aliasing*. The process of sampling a signal leads to aliasing—the frequency-domain reflection of signals about the sampling frequency. In most applications, aliasing is an unwanted effect that requires a low-pass anti-alias filter ahead of the ADC to remove high-frequency noise components, which would be aliased into the passband. However, *undersampling* can put aliasing to good use, most often in communications applications, to convert a high-frequency signal to a lower frequency. Undersampling is effective as long as the total bandwidth of a signal meets the Nyquist criterion (less than one-half the sampling rate), and the converter has sufficient acquisition and signal sampling performance at the higher frequencies where the signal resides. While fast SAR converters are capable of undersampling, the faster pipelined converters tend to be more effective at it. For more about undersampling and dither, see http://www.analog.com/support/standard_linear/seminar_material/practical_design_techniques/Section5.pdf.

SIGMA-DELTA

The sigma-delta architecture takes a fundamentally different approach than those outlined above. In its most basic form, a sigma-delta converter consists of an integrator, a comparator, and a single-bit DAC, as shown in Figure 5. The output of the DAC is subtracted from the input signal. The resulting signal is then integrated, and

the integrator output voltage is converted to a single-bit digital output (1 or 0) by the comparator. The resulting bit becomes the input to the DAC, and the DAC's output is subtracted from the ADC input signal, etc. This closed-loop process is carried out at a very high "oversampled" rate. The digital data coming from the ADC is a stream of "ones" and "zeros," and the value of the signal is proportional to the density of digital "ones" coming from the comparator. This bit stream data is then digitally filtered and decimated to result in a binary-format output. For more about sigma-delta conversion, see http://www.analog.com/support/standard_linear/seminar_material/practical_design_techniques/Section3.pdf.

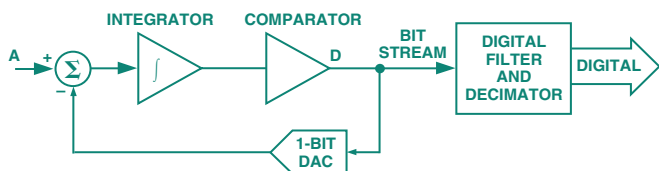


Figure 5. Sigma-delta ADC architecture.

Design Considerations and Implications: One of the most advantageous features of the sigma-delta architecture is the capability of *noise shaping*, a phenomenon by which much of the low-frequency noise is effectively pushed up to higher frequencies and out of the band of interest. As a result, the sigma-delta architecture has been very popular for designing low-bandwidth high-resolution ADCs for precision measurement. Also, since the input is sampled at a high "oversampled" rate, unlike the other architectures described in this paper, the requirement for external anti-alias filtering is greatly relaxed. A limitation of this architecture is its *latency*, which is substantially greater than that of the other types. Because of oversampling and latency, sigma-delta converters are not often used in multiplexed signal applications. To avoid interference between multiplexed signals, a delay at least equal to the decimator's total delay must occur between conversions. These characteristics can be improved in sophisticated sigma-delta ADC designs by using multiple integrator stages and/or multi-bit DACs.

APPLICATION EXAMPLES

The following three examples illustrate some of the issues described above.

Example 1: Multiple Inputs, 16-Bit Resolution

Consider an application that requires 16-bit resolution for 4 independent signals with bandwidths of dc to 15 kHz, 15 kHz, 15 kHz, and 45 kHz. The total throughput required to sample these signals under the Nyquist criterion is $(2 \times 15 + 2 \times 15 + 2 \times 15 + 2 \times 45)$ kSPS = 180 kSPS. At first glance, the SAR-type AD974, the sigma-delta AD7722, and the pipelined/sigma-delta AD9260 all have the required total throughput capability. But, as has been discussed above, the inherent latency of sigma-delta converters limits their effective throughput when they must continually acquire new signals by multiplexing. *Effective multiplexed throughput* can be defined as the total throughput of a converter when two or more independent signals are multiplexed. The following table compares the total throughput and effective throughput for each converter and indicates the number of converters of its type that would be needed to serve in this application.

Converter	Architecture	Total Throughput (16-Bit Resolution)	Effective Multiplexed Throughput	Converters Needed for Application
AD974	SAR	200 kSPS	200 kSPS	1
AD7722	Sigma-Delta	195 kSPS	2.3 kSPS	4
AD9260	Pipelined/Sigma-Delta	2500 kSPS	75 kSPS	3

Whether converting a single input or several multiplexed inputs, the AD974 achieves a throughput rate of up to 200 kSPS. Since the application requires a total throughput of 180 kSPS, the AD974's performance is sufficient. In fact, this is exactly the type of application that the AD974 was designed for: in addition to the SAR converter and reference, it also contains an integrated 4-channel multiplexer.

The AD7722 and AD9260 both face the challenges confronted by sigma-delta converters in multiplexing several inputs. The AD7722's throughput is 195 kSPS when sampling a single signal, but it drops to just 2.3 kSPS when converting multiple signals, due to the settling time which results from oversampling and filtering. To use the AD7722 in this application, four converters (one per channel) would be needed.

The AD9260 combines pipeline and sigma-delta techniques. Its throughput rate of 2.5 MSPS makes it ideal for higher throughput single channel systems. But in this application, its settling time of 13.35 ms limits its effective throughput to 75 kSPS. To use the AD9260 in this application would require at least 3 converters. Note that if the AD9260 were purely a pipelined flash converter, a single converter would have had the required throughput, assuming that the inputs are periodic.

Example 2: Single Input, 16-Bit Resolution

Consider now an application that converts a single 90-kHz bandwidth input at 16-bit resolution. In this case, all three converters from the first example would work well. Here the choice among converters would be made on other considerations, including ac and dc performance, system-level considerations (e.g., Is there a great benefit to the anti-alias performance of sigma-delta converters in this application?), latency, and cost.

Example 3: Multiple Inputs, 14-Bit Resolution

Consider an application in which 16 inputs, each with a dc to 100-kHz bandwidth, are converted with a resolution of at least 14 bits. Three converters suitable for this application include the SAR-type AD7865, the sigma-delta AD7722, and the pipelined AD9240. The total throughput required under the Nyquist criterion is $2 \times 100 \text{ kHz} \times 16 = 3.2 \text{ MSPS}$. The following table shows the throughput for each converter.

Converter	Architecture	Total Throughput (14-Bit Resolution)	Effective Multiplexed Throughput	Converters Needed for Application
AD7865	SAR	416 kSPS	416 kSPS	8
AD7722	Sigma-Delta	220 kSPS	2.3 kSPS	16
AD9240	Pipelined	10 MSPS	10 MSPS	1

Of the three converters, only the AD9240 has the throughput needed to convert all 16 channels. The AD7865 has sufficient throughput for 2 inputs per converter. To use the AD7865 in this application, 8 converters would be needed. The AD7722 would

need to be used in a converter-per-channel implementation; thus 16 converters would be required.

Summary

While not exhaustive, the following table summarizes and ranks (in a generalized sense) the relative advantages of flash, pipelined, SAR, and sigma-delta architectures. A rank of 1 in a performance category indicates that the architecture is inherently better than the others for that category. An * indicates that the architecture has the capability or characteristic listed.

Characteristic	Sigma-			
	Flash	Pipelined	SAR	Delta
Throughput	1	2	3	4
Resolution (ENOB)	4	3	2	1
Latency	1	3	2	4
Suitability for converting multiple signals per ADC	1	2	1	3
Capability to convert non-periodic multiplexed signals	1	2	1	3
Simplified anti-aliasing	*	*	*	*
Can undersample	*	*	*	*
Can increase resolution through averaging (with dither noise)	*	*	*	*

ACKNOWLEDGMENT

The author is indebted to Alain Guery and Mike Coln for providing valuable direction, and for providing the figures shown.

REFERENCES

Analog-Digital Conversion Handbook, The Engineering Staff of Analog Devices, Inc. Englewood Cliffs, NJ: Prentice Hall, 1986. ISBN 0-13-032848-0. Available from Analog Devices: Phone (781) 461-3392.

Practical Analog Design Techniques, edited by Walt Kester. Norwood, MA: Analog Devices, Inc., 1995. ISBN 0-916550-16-8. Available from Analog Devices: Phone (781) 461-3392. Also available free on the Internet as *PDF chapters*. http://www.analog.com/support/standard_linear/seminar_material/index.html

High Speed Design Techniques, edited by Walt Kester. Norwood, MA: Analog Devices, Inc., 1996. ISBN 0-916550-17-6. Available from Analog Devices: Phone (781) 461-3392. Also available free on the Internet as *PDF chapters*. http://www.analog.com/support/standard_linear/seminar_material/index.html

Linear Design Seminar, edited by Walt Kester. Norwood, MA: Analog Devices, Inc., 1995. ISBN 0-916550-15-X. Available from Analog Devices: Phone (781) 461-3392. 